Impact of Atmospheric and Space Radiation on Sensitive Electronic Devices

Lucas Matana Luza, Frédéric Wrobel, Luis Entrena, Luigi Dilillo

Title: Impact of Atmospheric and Space Radiation on Sensitive Electronic Devices

Author(s): Lucas Matana Luza, Frederic Wrobel, Luis Entrena, and Luigi Dilillo

DOI: 10.1109/ETS54262.2022.9810454

Published: 01 July 2022

Document version: Post-print version (Final draft)

Please cite the original version:
L. M. Luza, F. Wrobel, L. Entrena and L. Dilillo, "Impact of Atmospheric and Space Radiation on Sensitive Electronic Devices," 2022 IEEE European Test Symposium (ETS), 2022, pp. 1-10, doi: 10.1109/ETS54262.2022.9810454.

Impact of Atmospheric and Space Radiation on Sensitive Electronic Devices

Lucas Matana Luza*, Frederic Wrobel†, Luis Entrena‡, and Luigi Dilillo*,
*LIRMM, University of Montpellier, CNRS, Montpellier, France. {lucas.matana-luza, luigi.dilillo}@lirmm.fr
†IES, University of Montpellier, UMR-CNRS 5214, Montpellier, France. frederic.wrobel@umontpellier.fr
‡Department of Electronic Technology, Universidad Carlos III de Madrid, Leganés, Madrid, Spain.
entrena@ing.uc3m.es

Abstract

Studying the radiation effects on electronic devices is essential for avionics and space systems. The shrinking technology nodes and increasing density of devices enhance the sensitivity of electronic systems to ionizing radiation. Due to their crucial role, memories and processors are the highest contributors to soft errors in systems, making them the best candidates for studying these effects. This work introduces the radiation environment in space and atmosphere and the main effects that the different types of ionizing particles that are present in these environments may produce on electronic devices. Furthermore, mainly focusing on Single-Event Effects (SEEs), it presents approaches and tools for modeling SEEs and their impact on memories and microprocessors. Additionally, experimental results targeting a Commercial-Off-The-Shelf self-refresh Dynamic RAM are presented. These experiments are based on radiation test campaigns in particle accelerators with neutrons and protons. Finally, an overview of issues and mitigation techniques for microprocessors is exposed.

Index Terms

Radiation, environments, simulation tools, Total Ionizing Dose, Single-Event Effects, memory, processor

I. Introduction

In avionics and space systems, the study of radiation effects is crucial to ensure the high reliability of the system components and provide the required insight for important design decisions. Concerns about the radiation-induced impact on electronics became relevant from the beginning of the space era. For example, critical errors caused by cosmic ions were observed in space probes of the Pioneer and Voyager programs [1]. At avionic altitude, the population of ionizing particles (mostly neutrons and protons) has its peak in the atmosphere, making necessary the study of their impact on aeronautic electronics.

As the technology nodes get smaller and components more integrated [2], testing components for radiation-induced effects has become crucial. This procedure plays an important role in understanding the weakness of a certain technology, the failures mechanisms, and the best mitigation techniques that can be applied. Relevant radiation effects might differ when considering different technology node sizes. For instance, Single-Event Effects (SEEs) may occur by direct ionization with low energy protons [3], being an important aspect when considering smaller technology nodes.

Besides the fact that ionizing radiation may induce effects of different components, several works have shown that memories devices are one of the highest contributors to soft errors in systems [4]–[7]. Furthermore, due to their key role, microprocessors are sensitive elements of systems since they represent a relevant part of the controlling logic. Microprocessors have complex failure modes that are difficult to analyze, diagnose, and mitigate [6], [8]. This fact makes memories and microprocessors the best candidates for studying soft errors.

This work first introduces the radiation environment in space and atmosphere. The involved particles are presented as well are their main effects on electronic devices (dose and single-event effects). Then a focus is made on SEEs and the mechanisms of Single Event Transient (SET) and Single Event Upset (SEU) [9]–[11]. Monte Carlo tools are used to detail how the particles interact in the device and how they trigger a single event. The work next presents experimental results obtained through accelerated radiation test campaigns, which have been made in particle accelerator facilities that mimic the space environment.

The results presented in this paper have been obtained in the framework of the EU project RADNEXT, receiving funding from the European Union's Horizon 2020 research and innovation programme, Grant Agreement no. 101008126.

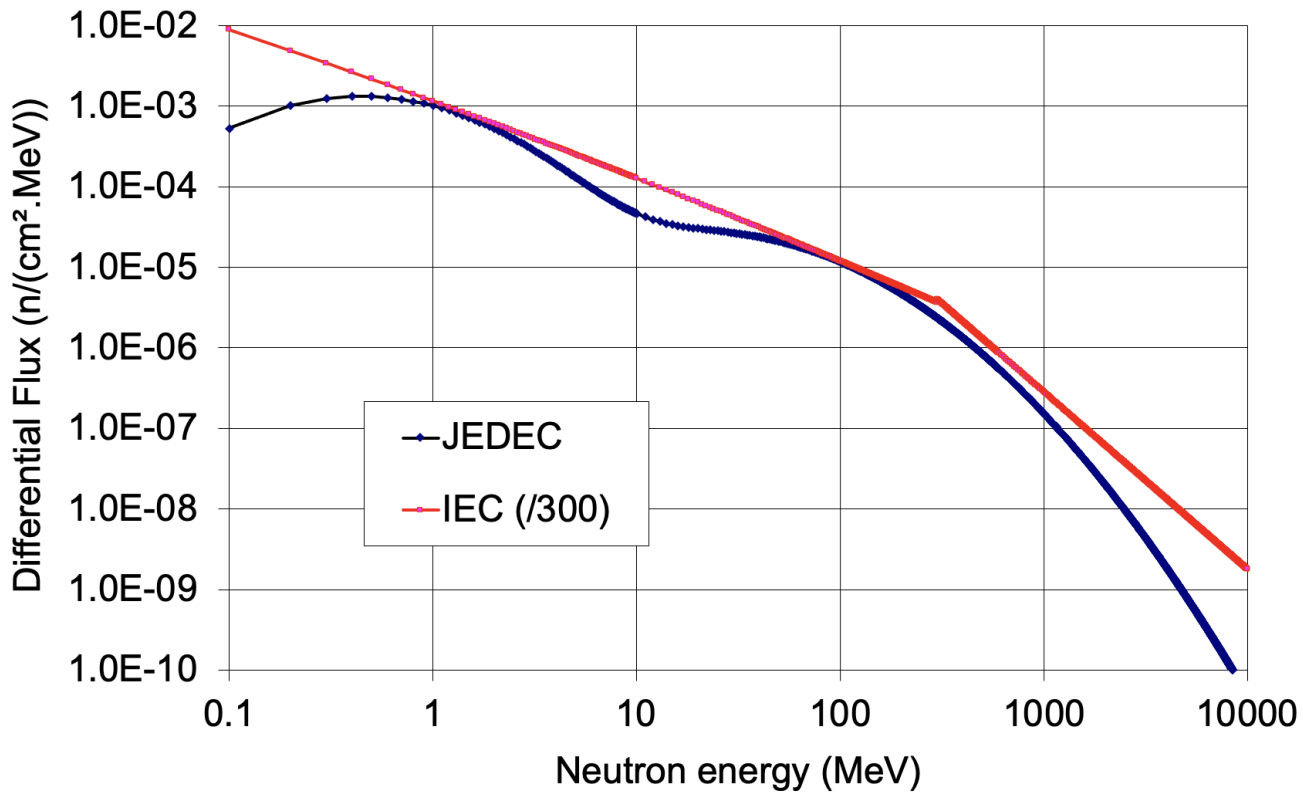

Fig. 1. Comparison of neutron flux in the atmosphere at ground level (JEDEC [15]) and at avionic altitude (IEC [16]). The spectra are very similar when using a scaling factor of 300.

II. From Natural Radiation Environments To Single Event Effect Modeling

A. Introduction to Radiation Environment

The Sun permanently emits some ionizing particles such as electrons and protons and, in a smaller contribution, heavier ions. These particles are produced during two different processes that are very different. The first one is a continuous emission due to Sun's hot corona and is called solar wind [12] while the second is sporadic and includes solar flares and coronal mass ejection [13]. Particles are traveling in Space and come in the vicinity of the Earth. Depending on their energies and direction, they can be trapped in the magnetic field. If so, they increase locally the density of particles in certain regions of the Space around Earth, which are called Radiation belts or Van Allen belts [14]. There are two main regions with high density of particles with typically $1{\cdot}10^6$ particles /cm^2/s. The first one, the inner belt, is localized at altitudes ranging from 700 to 10 000 km and is mainly composed of electrons and protons. The second region, the outer belt, is localized at an altitude between 13 000 and 60 000 km and is essentially composed of protons. In addition to these particles coming from Sun, there are also some heavy ions coming from other stars in the galaxy [13].

In space applications, these radiations belts are well known and must be considered to prevent electronic failures. For avionic and ground-level applications, the magnetic field of the Earth acts partly as a shield against the particles from Space. However, some particles are likely to cross the magnetosphere and reach the atmosphere. When it happens, the collision of a primary particle with the nucleus of an atom of Oxygen or Nitrogen triggers a cascade of nuclear reactions that produce multiple secondary particles, mainly neutrons. Because the atmosphere can attenuate the flux of particles, the neutron flux decreases with altitude, and at ground level, we still have around 13 neutrons/cm^2/h [15] (neutrons above 10 MeV). This value depends on latitude and solar activity. At avionic altitude, it is generally considered that this neutron flux is around 300 times that at ground level, as illustrated in Fig. 1.

B. Main effects on electronic devices

When particles from space (protons, electrons, and heavy ions) or from the atmosphere (mainly neutrons) interact in an electronic device, they can trigger various malfunctions that can be classified into three categories, namely

TABLE I
FAMILIES OF FAILURES VERSUS PARTICLES KIND.

Origin	Particle	TID	DDD	SEE
Galaxy	Ions			X
Sun	Protons	X	X	X
Radiation Belts	Protons	X	X	X
	Electrons	X	X	
Atmosphere	Neutrons			X
Material	Alpha radioactivity			X

Total Ionizing Dose (TID), Displacement Damage Dose (DDD) and Single Event Effects (SEE). The Total Ionizing Dose effect is due to the ionization of the medium by the incident particles and the resulting trapping of charges in dielectrics. The trapped charge increases with time as the irradiation is permanent. This trapped charge causes additional voltage, which is responsible for a drift of electric characteristics of the device.

Displacement Damage Dose is also a cumulative effect due to numerous particles that interact with the medium. Nevertheless, in the case of DDD, the incident particles can modify the crystalline structure of the material by knocking the nuclei of the atoms. This results in defects that introduce energy levels in the bandgap and parasitic currents able to cause a failure.

Single Event Effect is very different since a unique particle is able to cause a malfunction. The primary particle ionizes the medium, and the resulting electron-hole pairs drift and diffuse in the device, creating a parasitic current at the electrodes. Depending on the device sensitivity and the features of the parasitic current (shape, height, width), a malfunction may occur. Different kinds of failures exist, such as Single Event Transient, Single Event Upset, Single Event Latch-up, Single Event Functional Interruption, and many others [15].

Depending on the application and thus on the radiation environment, we may observe a specific family of failures. Table I indicates the family of failure at play for different natural environments. Let us note that SEE can occur in any natural environment. In addition, even if electrons are not the main concern for SEE, it has been demonstrated that they can also trigger SEE in very integrated technology [17].

Finally, it is worth mentioning that intrinsic radioactivity of material can produce alpha particles that are ionizing particles and can also produce failures. However, due to the low disintegration rate, only SEE at ground level (and even underground) are observable in modern applications [18].

C. Single Event Effect Modeling

In the rest of the paper, we focus on the family of SEE failures that are at play in all applications. To investigate the reliability of a given device in a given radiation environment, we can either perform testing using particles beams or perform numeric simulation. Actually, these two approaches are complementary since both of them have advantages and drawbacks. There are many ways to perform simulations that deal with multi-scale physics and will require an important CPU time if we need accuracy. Basically, the simplest methods are based on a time-independent process for which only the charge deposited in the device is at play. This is the case with very well-known models such as RPP (Rectangular Parallelepiped) and IRPP (Integral Rectangular Parallelepiped) methods [19]. The main drawback of this approach is not to account for the collection rate and thus does not consider the reaction of the circuit during the charge collection. Then, if we want to introduce time dependence, we need to consider the transport of electron-hole pairs in the device just after the passage of the particle. Even if TCAD (Technology Computer Aided Design) tools are devoted to this kind of calculation, it will actually require too much time to perform calculations in many configurations (different particles, different energies, different locations, different directions). Alternately, we can use a simplified transport model such as the drift-diffusion-collection model [20] that considers the ion tracks as the sum of many elemental tracks that are able to diffuse spherically in the semiconductor, at least far from the junctions. When the electrons pairs approach the junctions, the drift is considered, and the pairs are separated by the electric field. Consequently, a transient current is generated at the node and can be injected into a SPICE (Simulation Program with Integrated Circuit Emphasis) simulation or equivalent [21]. Finally, the effect of one ionizing particle in specific conditions is known. If we want to evaluate the real sensitivity of the device, we must perform such calculations

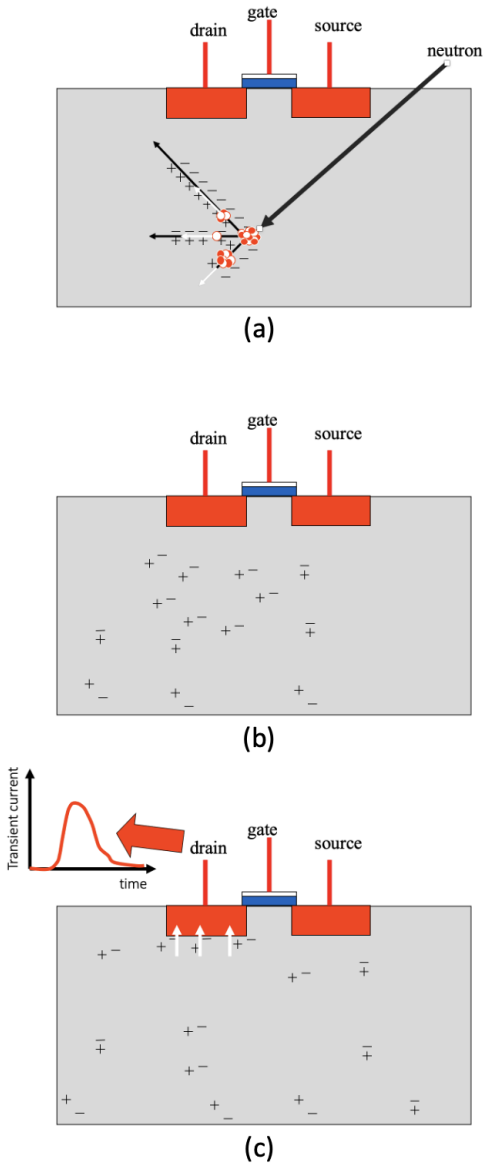

Fig. 2. Illustration of charge collection in a MOS transistor. (a) a neutron produces some ionizing particles through nuclear reactions, and electron-hole pairs are generated, (b) electron-holes pairs diffuse in the device, and (c) electron-hole pairs are separated, and a transient current is generated.

for many configurations. This is the goal of the Monte-Carlo approach that takes advantage of random numbers to mimic realistic configurations (many possibilities for energies, direction, etc.). Fig. 2 illustrates the three main steps of the process: (a) a neutron from the radiation environment in the atmosphere triggers a nuclear reaction in the semiconductor. The secondary ions that are produced create some electron-hole pairs along their tracks. (b) Far from the junctions, as the electric field is low, the electron-hole pairs diffuse through ambipolar diffusion. (c) Electron-hole pairs are separated by the electric field at the junction, and a transient parasitic current is generated at the node.

The sensitivity of the device is evaluated by using the concept of cross section symbol σ, which is simply the ratio of the number of failures *N* divided by the fluence Φ of particles:

$$\sigma = \frac{N}{\Phi} \tag{1}$$

The cross section expresses the effective area of the device that is sensitive to radiation. The main advantage of simulation is that it allows calculating the cross section for different input parameters such as kind of particles,

energies, supply voltage, transistor parameters, temperature, or even layout cell. By comparing the results of several layouts, it is then possible to evaluate which one is the most hardened to radiations.

III. Radiation-Induced Effects on Memories

Memory devices, in general, are particularly sensitive to radiation-induced effects. Targeting SEEs, the main issues are related to SELs, SEUs, and SEFIs. A particle passing through the semiconductor material can create an ionized track of free electrons-holes which can reach critical places on the device structure. It can be generated by an indirect ionization (from protons or neutrons), which occurs when an impinging particle causes a nuclear reaction that generates heavy recoils (as illustrated in Fig .2). Or direct ionization, with alpha particles, heavy ions, and low-energy protons. The mechanisms to generate such types of events have a strong dependency on memory technology.

In a DRAM (Dynamic Random Access Memory), whose technology is based on a one-transistor one-capacitor cell structure, the memory information is defined by the charge stored in the capacitor. The SEU mainly occurs by a charge collection within the memory binary cell caused by a particle strike occurring in, or close to, the storage capacitor or the access transistor [22], [23]. The cell upsets occur through a charge collection by the bias junction of a cell-access transistor, increasing the charge on the storage capacitor, and by charge transfer due to a low-resistive path created by an ionizing particle, which moves electrons from a low-voltage node to a high-voltage node [24]. Also, upsets can be caused by a charge collection in the pre-charged bit line during a memory access, introducing an imbalance in the sensing signal during or before the sensing operation [22]. In Flash memories, the bit upset occurs with the introduction of a voltage threshold shift. The charges trapped in the floating gate transistors can be discharged due to the radiation interaction, which will reduce its voltage threshold. If this shift brings the threshold value to a value lower than the one to identify the correct logic value in the cell, it will then generate a fault [25]. The mechanism that leads to these effects is not fully established. However, some of them are described in [26]. Based on SRAM devices, if the created track of electron-hole pairs reaches the reverse-biased junction of the SRAM cells, the generated transient current can flip the actual state of the cell, generating an SBU [1].

As stated above, prediction models are available for designers to assess the amounts of impinging particles in a given environment. However, these models are not completely satisfactory because they require experimental validation by exposing the system to similar conditions of an in-field application, e.g., space applications. From the radiation tests, it is possible to evaluate the electronic device by identifying the types of the generated faults and their frequency and appearance conditions. More directly related to the activities of the authors, [27] explores methods for testing memory devices and the outcome results based on two SRAM (Static Random Access Memory) laid out on a 90 nm and 65 nm technology node size. The radiation-induced effects on an SLC (Single Level Cell) NAND Flash under heavy-ions and proton irradiation were evaluated in [28], [29]. The occurrence of SELs on an MRAM (Magnetoresistive Random Access Memory) is presented in [30]. Additionally, radiation-induced SEEs in a COTS FRAM (Ferroelectric Random Access Memory) are described in [31]. Studies on these memories show that SEEs can occur in different ways, such as SBUs, Multiple Cell Upsets (MCUs), SEFIs, or SELs, and it generates different kinds of fault behaviors on the devices. Which then should be explored in detail since it may lead to unexpected behaviors when the devices are exposed to a harsh radiation environment.

In this light, the following subsection will present a summary of experimental results from the exposition of a Self-Refresh DRAM memory exposed to thermal and atmospheric-like neutron spectra and high-energy protons.

A. Experimental Results on a Self-Refresh DRAM

A Self-Refresh DRAM, also known as pSRAM (pseudo-Static RAM), is based on an array of DRAM cells that require periodic refresh operations in its memory contents. In DRAMs, the refresh operation is performed by the host, which should take care of applying such operations following timing requirements to maintain the data consistency. In a Self-Refresh device, the refresh control is performed by an on-chip logic, which will apply the refresh operation according to its timing requirements and while the memory is not actively being read or write. In this structure, since the host does not need to manage any refresh operation, the memory behaves as an SRAM device, which is composed of static cells that do not demand this kind of refresh controller [32].

The tests target a 64 Mib Self-Refresh DRAM manufactured by Infineon Technologies, the S27KS0642GABHI020. The memory is designed with a 38 nm high-speed CMOS, and it is commercially known as HyperRAM™ with a HyperBus™ interface. The self-refresh mechanism distributes single row refresh operations with an array refresh interval of 64 ms [33].

The experimental results presented in this paper as based on three separate test campaigns. The first test campaign was with thermal-neutron irradiation at the Platform for Advanced Characterization (PAC-G) facility hosted by the Institute Laue Langevin using the D50 instrument. The instrument provides a equivalent flux at 25 meV of

about 10^9 n/cm^2/s [34]. The second test campaign was carried out at the Rutherford Appleton Laboratories, UK, at the ChipIr beamline, with an atmospheric-like neutron spectrum with a flux of about 5×10^6 n/cm^2/s for energies above 10 MeV, and also a thermal component for energies lower than 0.5 eV with a flux of 4×10^5 n/cm^2/s [35], [36]. The third test campaign was carried out in the Proton Irradiation Facility (PIF), part of the Paul Scherrer Institute (PSI) in Switzerland. The primary proton energy used was 230 MeV, and to reach lower energies (150 MeV and 70 MeV), metal plates were placed in the beam path to reduce the energy of the protons and the fluxes were from 3×10^7 to 8×10^7 p/cm^2/s.

These experiments employed two types of tests in the DUT: static and dynamic. For the static test, a write operation is performed with a known data pattern to the entire DUT address space. Then, the memory is irradiated during a time interval, and subsequently, readback operations are performed to identify the faulty bits of each address. In dynamic test mode, the memory is accessed by consecutive operations following an algorithm, such as March C- (2), Dynamic Stress, Dynamic Classic, and mMats+ [37]. For example, in (2), the operations enclosed by the parenthesis are performed in the DUT in a sequential addressing order ruled by the arrows ('↑' up or '↓' down), where, in our case, '↑' means that the operations are executed from the lower address up to the highest address, and '↓' is the opposite. The operations are indicated by 'w' (write), and 'r' (read), and the following Boolean number indicates the data background (all '0', or all '1').

$$\begin{aligned} &\uparrow (w0); \\ &\{\uparrow (r0, w1); \uparrow (r1, w0); \downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0)\} \end{aligned} \tag{2}$$

This work provides a summary of outcomes related to faults induced by neutron and high-energy proton irradiation. A detailed view of all outcomes from the neutron irradiation testing can be founded in previous work from the research group [37].

The outcomes of the three tests campaigns led to the identification of SBUS, stuck bits, and SEFIs (which are shown as block errors). The simplest observed fault is the SBU, which is classified by identifying the bit upset that occurred only once during the test campaign (per DUT). In these cases, the error was not recurrent after a write operation on the bit cell.

The second type of fault is the stuck bit. A stuck bit is a bit that has reoccurring errors, which means that independently of the setting value, a read operation returns a stuck value ('1' or '0'). Several studies have shown that stuck bits may appear with intermittent behavior [38]–[40], being able to operate normally during different periods within a stuck state, and being intermittently faulty. DRAM cells present a variable retention time capability, and these effects may be enhanced by radiation-induced effects that can increase the cell leakage, thus reducing the cell retention capability and leading to stuck bits [41]. In several works, this effect is assumed to be caused by micro-dose and displacement damage effects [41]. In, e.g., [42], the stuck bits were attributed to single-particle displacement damage effects induced by single high-energy neutrons and protons.

The third type of fault was classified as block errors, which should result from a SEFI on the memory controlling logic. Block errors appeared as horizontal or vertical lines spanning a significant portion of rows (in a range of 512-word addresses on horizontal shapes) or columns (in a range of 2048-word addresses on vertical shapes). Based on this kind of event, a write operation on the addresses restored the access without a need to carry out a power cycle.

Examples of the three different faults are depicted in Fig. 3 by a bitmap representing the entire memory array. The bitmap is composed of 16384 columns and 4096 rows, and each pixel represents a bit cell. In order to improve the visibility of the faults, first, an external blue box delimits the bitmap region, and then internal blue boxes show a zoom-in portion of the bitmap, presenting block errors in the vertical and horizontal shapes, and also sparse single bits that may be an SBU or a stuck bit.

Furthermore, to evaluate the device sensitivity, based on (1), the cross sections were calculated for each source of radiation regardless of the applied test mode. In the case of SBU and stuck bit, the cross section value is normalized by the memory size (64 Mib). A summary of the results is shown in Table II.

The obtained cross sections show that the HyperRAM™ is not very sensitive to thermal neutrons, and even with the increased value with atmospheric-like neutrons and high-energy protons, the value remains very low. Furthermore, from an application point of view, a single-bit error in a word can be easily corrected with the use of error Error Detection And Correction (EDAC) schemes, and based on the calculated cross sections, the possibility to have more than one erroneous bit in a word could be considered negligible. However, one single block error can lead to more than hundreds of word addresses with errors, which would pose an issue in safety-critical applications.

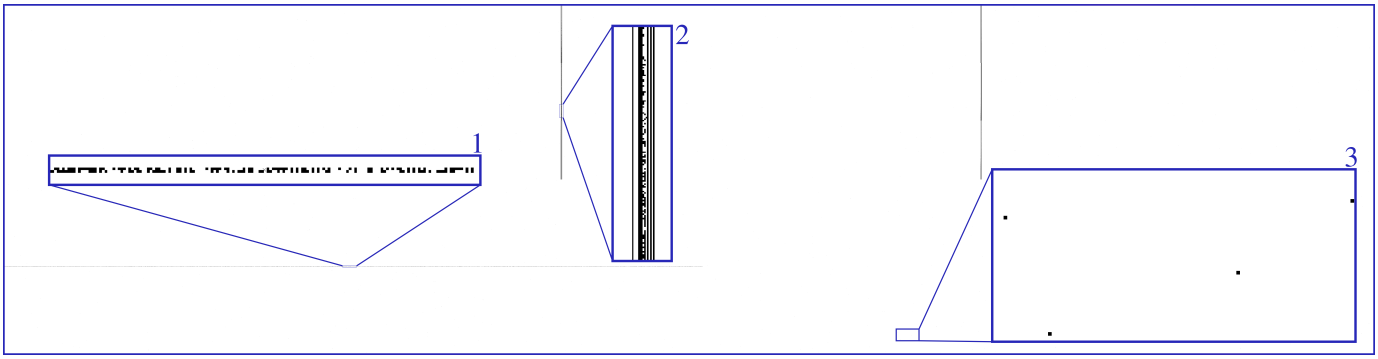

Fig. 3. Example of error types in the logical memory bitmap represented by 16384 columns per 4096 rows. The bits are represented as pixels, and each pixel with an error appears in black. Zoom-ins are added to increase the visibility of the block event and the SBU and/or stuck bit. The zoom-in box (1) presents a block event in the horizontal shape, (2) a block event in a vertical shape, and (3) SBUs and/or stuck bits randomly spread in the memory array.

TABLE II
SUMMARY OF IRRADIATION TEST RESULTS.

Radiation Source	Test Mode	σ		
		SBU (cm^2/bit)	Stuck Bit (cm^2/bit)	Block Error (cm^2)
Th-N	Dyn & Stat	$3.4 \cdot 10^{-20}$	$6.6 \cdot 10^{-20}$	$1.7 \cdot 10^{-12}$
ATM-N	Dyn & Stat	$2.8 \cdot 10^{-17}$	$1.4 \cdot 10^{-17}$	$4.4 \cdot 10^{-11}$
HEP 230 MeV	Dyn[a]	$9.2 \cdot 10^{-19}$	$3.5 \cdot 10^{-18}$	$2.7 \cdot 10^{-11}$
HEP 150 MeV	Dyn[a]	$8.2 \cdot 10^{-19}$	$2.4 \cdot 10^{-18}$	-[b]
HEP 70 MeV	Dyn[a]	$4.9 \cdot 10^{-19}$	$1.9 \cdot 10^{-18}$	-[b]

Th-N = Thermal Neutrons, ATM-N = Atmospheric-like Neutrons, HEP = High Energy Protons, Dyn = Dynamic, Stat = Static.

[a] Only the March C- (2) was executed.

[b] No block error occurred.

IV. Radiation-Induced Effects on Microprocessors

Microprocessors are ubiquitous, and spacecraft are no exception. Most systems in a spacecraft, from the attitude control system to the payloads, are embedded systems that are built around a microprocessor. These embedded systems are not functionally different from those used in commercial applications. However, the space environment imposes more stringent design constraints. Size, weight, and power (SWaP) are at a premium in spacecraft. Cost is also increasingly being added to the list of constraints, leading to SWaP-C optimization. At the same time, modern satellite applications require more computing power for remote sensing, image processing, intelligent systems, mission autonomy, etc. All these requirements must be satisfied within a high level of reliability, which is particularly threatened by radiation-induced faults.

At the atmospheric level, as mentioned earlier in the paper, radiation exposure is much lower, but it cannot be neglected. Experimental evidence has shown that neutron-induced faults can occur in safety-critical and high-performance computing applications, such as cars, airplanes, data centers, and supercomputers, among others [8], [43].

A. Radiation Effects in Microprocessors

Low sensitivity to cumulative degradation effects, such as TID, and destructive effects, such as SEL, is generally a critical requirement in space applications. Fortunately, the incidence of these effects is being reduced as technology

progresses. With the general shrinking of CMOS technology, TID resilience has been steadily improving due to the reduction of the thicknesses of SiO_2 dielectric layers [44]. Today, TID is no longer a problem in advanced digital CMOS technologies at doses typical for many space applications. Single Event Latch-Up is still a critical problem that must be evaluated, although it has also improved with the use of some technologies, such as Silicon-On-Insulator (SOI). Provided that these key radiation effects are covered, radiation-induced soft errors, such as SEU and SET, become the main reliability concern.

In a microprocessor, the most important components affected by SEUs are the memories (treated above in the paper), particularly the caches and the register file. However, a modern processor has many internal registers for different functions, including pipeline registers, shadow registers, etc. SEU effects in these internal registers are challenging to evaluate and classify because they depend on inner implementation details, which are often unknown to the application designer. Moreover, errors in the combinational logic caused by SETs are becoming an increasing concern, as they can create multiple errors in the processor registers.

Soft errors in microprocessors can produce a variety of failure modes, which are commonly classified into data errors and control-flow errors. A data error is a wrong computation result that is typically produced when an error happens in a register or memory position storing data. A control-flow error occurs when a control register, such as the program counter, is affected by an upset, resulting in the corruption of the instruction flow. Control-flow errors may produce a wide variety of effects, including wrong computation results, excessive computation time, abnormal termination, or losing control of the execution. Recovery from control-flow errors is generally tricky and may eventually require a complete reset or a power cycle. This condition involves a long recovery time to restore the system operation, and it is often identified as a SEFI.

With the complex microprocessors and systems that are commonly used today, error detection and recovery are challenging, while error correction is very expensive. Partial solutions, with a constrained impact on cost, performance, and power, are often sought. For this purpose, it is necessary to perform a systematic analysis of the soft error rate and then apply optimized protection mechanisms to the most critical processor components [45]. Architectural Vulnerability Factors (AVF) [46] express the probability that a user-visible error will occur given a bit-flip in a storage cell. Statistical fault injection is a well-known approach to determine AVFs, but it involves huge simulation or emulation efforts. In addition, fault injection is not generally considered accurate enough in the space community because it cannot take technological features into account. For this purpose, radiation test results are needed, which are seldom available and are costly to obtain.

Evaluating microprocessors under radiation is also challenging because they are complex systems and are not easy to test. Typically, the details of the implementation are unknown. Thus, identifying the cause of errors and the most critical parts that require protection is a very difficult task. Diagnosis techniques have recently been proposed that leverage the trace infrastructures [6], [47]. Through the trace interface, errors that may happen in a microprocessor running a real application under radiation testing can be detected. When an error is detected, trace information and context data are collected and analyzed to diagnose the cause of the error. With this information, it is generally possible to reconstruct the execution status at the precise moment that the error occurred and determine many interesting aspects about the cause of errors, such as the address of the last completed instruction before an error, the type of error, and the location of the error. This approach is not intrusive and can diagnose faults under realistic conditions. It can be used offline to precisely analyze the vulnerability of processor resources or online, to diagnose errors, and implement tailored recovery actions for each type of error while in operation.

An important aspect to take into account is the latency of error detection and correction. Ideally, errors should be detected and corrected as soon as possible to avoid error propagation. However, error checking or voting with fine granularity involves large area and performance penalties. On the contrary, if error checking is performed at the system level, error recovery usually involves large down times. Moreover, it is possible that latent errors remain in the system and manifest themselves at a later time with unpredictable consequences.

B. Rad-Hard Microprocessors vs. COTS Microprocessors

The choice of microprocessors in the space sector has been traditionally limited to radiation-hardened devices [48], [49]. Some devices are manufactured on dedicated radiation-hardened processes, which ensure reduced susceptibility to radiation effects. However, the cost of maintaining such special manufacturing processes just to support a small market has become prohibitive. In addition, moving to smaller technology nodes requires a huge investment that is difficult to justify for the low volume production of space applications, so such processes typically lag several generations behind state-of-the-art technologies. Alternatively, radiation hardening can be achieved by means of design techniques (RHBD) at the layout, logic, and architecture level. Examples of such techniques include special radiation-tolerant libraries with special transistor shapes, guard rings, built-in TMR latches, SET filters, etc. [50].

Whatever the choice, developing a rad-hard microprocessor is an expensive and time-consuming effort. In addition to the usual ASIC design tasks, a space microprocessor must be qualified, and this involves extensive testing in radiation facilities, among other tasks. As a result, the portfolio of available microprocessors for space is very small. Moreover, rad-hard microprocessors lag several generations behind their commercial counterparts and have high power consumption, low performance, and very high price. There is a growing market of applications in which some of those disadvantages are unacceptable, such as small satellites with tight budget constraints (NewSpace), missions that require high processing performance, or low to medium critical missions with tight power constraints. This tendency justifies the interest in the use of COTS microprocessors in space applications, provided that sufficient error detection or mitigation can be achieved [51], [52].

An alternative that is commonly considered consists of implementing a soft core in a rad-hard FPGA. Although this solution is relatively straightforward, it provides poor performance and power consumption.

Recent CNES (National Centre for Space Studies) missions, such as ANGELS and Eyesat, use commercial microprocessors successfully [53]. EyeSat is a 3U CubeSat equipped with a small space telescope (IRIS, Imager Realized for Interplanetary dust Study). Apart from the acquisition of science data, this mission has as objectives also the demonstration of new satellite technologies and readying students for careers in space engineering. According to CNES, EyeSat was developed by more than 200 students from engineering schools and universities. The satellite was launched in 2019, and all the satellite's subsystems were successfully tested in orbit, including image acquisition and downlink images of the sky and Earth. EyeSat has demonstrated new technologies, including a flight computer based on the Xilinx Zynq family. CNES ANGELS (Argos Neo on a Generic Economical and Light Satellite) objective is to develop a range of commercial satellites, with a smaller weight than 50 kilograms, for radiofrequency operational missions that will be part of the Kineis constellation. ANGELS presents a NewSpace approach using COTS components to decrease cost and design time (the satellite was developed and launched in less than 24 months).

These missions show that COTS microprocessors are successfully used in NewSpace satellites currently. However, they are not designed for working in a harsh environment, and the radiation effects in them are mostly unknown. This is a major drawback that forces to take major risks and is the cause of the high small-satellite mission failure rates [54].

Space agencies have programs to test relevant commercial microprocessors in order to determine their inherent radiation tolerance and sensitivities [55]. The list of devices of interest is not limited to conventional architectures: it includes GPUs, SoCs, embedded FPGA devices like Zynq and Versal, and even neural network devices. Testing will include TID and SEE with protons, heavy ions, and laser. The goals of these programs include identifying challenges for future radiation hardening efforts and investigating new failure modes and effects.

C. Error Mitigation Techniques

Error mitigation techniques suitable for microprocessors are traditionally divided into three basic types: hardware, software, and hybrid techniques [56].

Pure hardware techniques, such as Triple Modular Redundancy (TMR), are not feasible for COTS microprocessors, except at the system level. The main drawback of TMR, independently of the applied granularity, is the high area and power overhead. TMR approaches require triplicating the hardware and adding voters to correct errors. For error detection, duplication is sufficient. Dual-Core Lockstep (DCLS) can exploit the availability of multicore devices, but it requires hardware support for tight synchronization. More flexible COTS-based fault-tolerant architectures have been proposed, such as DMT (Duplex Multiplexed in Time) and DT2 (Dual Duplex Tolerant to Transients) [51]. These architectures use a more flexible macro-synchronization approach that relies on external modules for checking memory and I/O accesses.

Software implemented fault-tolerance (SIFT) is an attractive solution for microprocessors because it does not require hardware modifications. SIFT techniques usually take into consideration the type of observed error, i.e., data errors or control-flow errors. For data errors, the software is modified by inserting replicated instructions that operate on copies of the original data. Additional comparison or checking instructions in the program must be added to check the consistency of the replicated data with the original data. Because of the redundant computations and the data checks, a substantial performance decrease is produced, and memory requirements for both program and data are enlarged. This effect is illustrated in [57], [58].

Control-flow software fault-tolerance techniques check the integrity of the instructions and the execution order. For this type of technique, common approaches are based on Embedded Signature Monitoring (ESM) [59]. Basically, signature monitoring techniques rely on determining a signature at compilation time for certain parts or blocks of the code before execution and storing them in an appropriate memory block or register. Then, the signature is regenerated when the software is in execution and compared with the previously stored signatures that are considered golden

signatures. If there is a discrepancy between them, an error is triggered. Usually, the considered blocks are pieces of code without branches, but some variations of these techniques have been proposed in the literature [8], [59]. The comparison step can be accomplished with assertions, as in ECCA technique [60]. Again, penalties in performance and size of memory for both enlarged code and signature storage are experienced.

Although SIFT techniques have long been available, they are not much used in the space sector because of several reasons. In addition to memory and performance overheads, the contribution of their mitigation solutions can only cover the resources that can be observed through software. There are certain registers in the architecture that are critical and cannot be accessed from the programming model. In addition, testing SIFT techniques is very difficult because the observability of processor executions is poor. Fault injection is a practical solution, but it is clearly insufficient to test microprocessors because it cannot consider the technology susceptibility and the inner implementation details. In fact, most fault injection techniques usually work at the instruction level, which is rather poor. On the other hand, radiation testing is the standard validation approach for space applications, but it cannot provide details about the origins of errors.

Hybrid solutions combine hardware and software redundancy. Hardware redundancy is often introduced as an external module to accelerate the checking of redundant computations. This module can be used to simply trigger a timeout interrupt when it observes no activity on the system bus, or it can check memory accesses to validate the control and data flows [61], [62].

From a general point of view, the cost of fault-tolerant techniques can be reduced by making smart use of existing microprocessor resources. For example, we can take advantage of the increasing availability of multicore processors to implement lockstep or macro-synchronized redundant architectures. Among these resources, the trace infrastructures can provide a means to observe the microprocessor behavior in a non-intrusive manner [63]. The usefulness of the trace interface for error detection has been demonstrated under radiation for soft cores [8] and hard cores [64], with very good results. Another useful resource is the SIMD (Single Instruction Multiple Data) coprocessor, which can be used to reduce the effort of repeating data computations. In [65], an effective solution is shown that makes use of NEON SIMD coprocessor together with trace monitoring in a commercial ARM microprocessor. This technique can effectively mitigate errors with reduced area and performance overheads. This type of solution has great potential and can significantly improve with a reliability-aware design in future processors.

V. Conclusions

This work introduces the radiation environment in space and atmosphere, with the detail of the most impacting particles for aerospace electronics. The radiation-induced effects were classified, and approaches for the use of simulations tools for modeling the SEEs were presented. As a case study, memories and microprocessors were chosen as the most sensitive and representative blocks in electronic systems. An overview of SEEs in memories was presented as well as experimental results based on neutron and protons irradiation on a self-refresh DRAM, used as a meaningful example. Finally, the radiation-induced effects on microprocessors were explored, and several error mitigation techniques were presented.

References

[1] E. Petersen, *Single Event Effects in Aerospace*. Wiley-IEEE Press, Sept. 2011, DOI: 10.1002/9781118084328.

[2] G. E. Moore, “Cramming more components onto integrated circuits,” *Electronics*, vol. 38, no. 8, Apr. 1965.

[3] R. K. Lawrence, J. F. Ross, N. F. Haddad, R. A. Reed, and D. R. Albrecht, “Soft error sensitivities in 90 nm bulk CMOS SRAMs,” in *2009 IEEE Radiation Effects Data Workshop (REDW)*, Quebec, QC, Canada, Jul. 2009, pp. 71–75, DOI: 10.1109/REDW.2009.5336302.

[4] L. Dilillo, A. Bosser, A. Javanainen, and A. Virtanen, “Space radiation effects in electronics,” in *Rad-hard Semiconductor Memories*, ser. Electronic Materials and Devices. River Publishers, Nov. 2018, ch. 1, pp. 1–64.

[5] S. E. Damkjar, I. R. Mann, and D. G. Elliott, “Proton beam testing of SEU sensitivity of M430FR5989SRGCREP, EFM32GG11B820F2048, AT32UC3C0512C, and m2s010 microcontrollers in low-earth orbit,” in *2020 IEEE Radiation Effects Data Workshop (in conjunction with 2020 NSREC)*, Santa Fe, NM, USA, Dec. 2020, pp. 1–5, DOI: 10.1109/REDW51883.2020.9325842.

[6] M. Peña-Fernandez, A. Lindoso, L. Entrena, and M. Garcia-Valderas, “The use of microprocessor trace infrastructures for radiation-induced fault diagnosis,” *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, pp. 126–134, Nov. 2020, DOI: 10.1109/TNS.2019.2956204.

[7] J. Meza, Q. Wu, S. Kumar, and O. Mutlu, “Revisiting memory errors in large-scale production data centers: Analysis and modeling of new trends from the field,” in *2015 45th Annual IEEE/IFIP International Conference on Dependable Systems and Networks*, Sept. 2015, pp. 415–426, DOI: 10.1109/DSN.2015.57.

[8] A. Lindoso, L. Entrena, M. García-Valderas, and L. Parra, “A hybrid fault-tolerant LEON3 soft core processor implemented in low-end SRAM FPGA,” *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 374–381, Dec. 2017, DOI: 10.1109/TNS.2016.2636574.

[9] R. A. Reed *et al.*, “Anthology of the development of radiation transport tools as applied to single event effects,” *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1876–1911, Jun. 2013, DOI: 10.1109/TNS.2013.2262101.

[10] Y. Aguiar, F. Wrobel, J.-L. Autran, P. Leroux, F. Saigné, A. Touboul, and V. Pouget, “Analysis of the charge sharing effect in the SET sensitivity of bulk 45 nm standard cell layouts under heavy ions,” *Microelectronics Reliability*, vol. 88-90, pp. 920–924, 2018, DOI: 10.1016/j.microrel.2018.07.018.

[11] Y. Q. Aguiar, F. Wrobel, J.-L. Autran, P. Leroux, F. Saigné, V. Pouget, and A. D. Touboul, “Mitigation and predictive assessment of SET immunity of digital logic circuits for space missions,” *Aerospace*, vol. 7, no. 2, Feb. 2020, DOI: 10.3390/aerospace7020012.

[12] J. Barth, “Modeling space radiation environment,” in *NSREC Short Course*, 1997, pp. I–1.

[13] S. Bourdarie and M. Xapsos, "The near-earth space radiation environment," *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1810–1832, Sept. 2008, DOI: 10.1109/TNS.2008.2001409.

[14] C. S. Guenzer, E. A. Wolicki, and R. G. Allas, "Single event upset of dynamic RAMs by neutrons and protons," *IEEE Transactions on Nuclear Science*, vol. 26, pp. 5048–5052, Dec. 1979, DOI: 10.1109/TNS.1979.4330270.

[15] "Measurement and reporting of alpha particle and terrestrial cosmic ray-induced soft errors in semiconductor devices," JEDEC Solid State Technology Association, Sept. 2021, last accessed in March 21, 2022. Available: https://www.jedec.org/standards-documents/docs/jesd-89a.

[16] "Process management for avionics – atmospheric radiation effects – part 1: Accommodation of atmospheric radiation effects via single event effects within avionics electronic equipment," IEC/TS 62396-1, March 2006.

[17] M. P. King *et al.*, "The impact of delta-rays on single-event upsets in highly scaled SOI SRAMs," *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3169–3175, Dec. 2010, DOI: 10.1109/TNS.2010.2085019.

[18] F. Wrobel, J. Gasiot, F. Saigné, and A. D. Touboul, "Effects of atmospheric neutrons and natural contamination on advanced microelectronic memories," *Applied Physics Letters*, vol. 93, no. 064105, 2008, DOI: 10.1063/1.2971203.

[19] E. Petersen, J. Pickel, E. Smith, R. Rudeck, and J. Letaw, "Geometrical factor in SEE rate calculations," *IEEE Transactions on Nuclear Science*, vol. 40, no. 6, pp. 1888–1909, Dec. 1993, DOI: 10.1109/23.273465.

[20] T. Mérelle, H. Chabane, J.-M. Palau, K. Castellani-Coulié, F. Wrobel, B. S. F. Saigné, J. Boch, J. R. Vaille, G. Gasiot, P. Roche, M.-C. Palau, and T. Carrière, "Criterion for SEU occurrence in SRAM deduced from circuit and device simulations in case of neutron-induced SER," *IEEE Transactions on Nuclear Science*, vol. 52, no. 4, pp. 1148–1155, Aug. 2005, DOI: 10.1109/TNS.2005.852319.

[21] F. Wrobel, A. D. Touboul, L. Dilillo, and F. Saigné, "Soft error triggering criterion based on simplified electrical model of the PSRAM cell," *IEEE Transactions on Nuclear Science*, vol. 60, no. 4, pp. 2537–2541, Aug. 2013, DOI: 10.1109/TNS.2012.2235148.

[22] P. Dodd and L. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 583–602, Jun. 2003, DOI: 10.1109/TNS.2003.813129.

[23] T. May and M. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE Transactions on Electron Devices*, vol. 26, no. 1, pp. 2–9, Jan. 1979, DOI: 10.1109/T-ED.1979.19370.

[24] A. Bougerol, F. Miller, N. Guibbaud, R. Leveugle, T. Carriere, and N. Buard, "Experimental demonstration of pattern influence on dram seu and sefi radiation sensitivities," *IEEE Transactions on Nuclear Science*, vol. 58, no. 3, pp. 1032–1039, Jun. 2011, DOI: 10.1109/TNS.2011.2107528.

[25] S. Gerardin, M. Bagatin, A. Paccagnella, K. Grürmann, F. Gliem, T. R. Oldham, F. Irom, and D. N. Nguyen, "Radiation effects in flash memories," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1953–1969, Jun. 2013, DOI: 10.1109/TNS.2013.2254497.

[26] M. Bagatin, S. Gerardin, and A. Paccagnella, "Space and terrestrial radiation effects in flash memories," *Semiconductor Science and Technology*, vol. 32, no. 3, p. 033003, Feb. 2017, DOI: 10.1088/1361-6641/32/3/033003.

[27] L. Dilillo, G. Tsiligiannis, V. Gupta, A. Bosser, F. Saigne, and F. Wrobel, "Soft errors in commercial off-the-shelf static random access memories," *Semiconductor Science and Technology*, vol. 32, no. 1, p. 013006, 2016, DOI: 10.1088/1361-6641/32/1/013006.

[28] V. Gupta, "Analysis of single event radiation effects and fault mechanisms in SRAM, FRAM and NAND Flash: application to the MTCube nanosatellite project," Ph.D. dissertation, Université de Montpellier, 2017, [Online]. Available: https://ged.biu-montpellier.fr/florabium/jsp/nnt.jsp?nnt=2017MONTS087.

[29] L. M. Luza, A. Bosser, V. Gupta, A. Javanainen, A. Mohammadzadeh, and L. Dilillo, "Effects of heavy ion and proton irradiation on a SLC NAND Flash memory," in *2019 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Noordwijk, Netherlands, Oct. 2019, pp. 1–6, DOI: 10.1109/DFT.2019.8875475.

[30] A. L. Bosser, "Single-event effects from space and atmospheric radiation in memory components," Ph.D. dissertation, Université de Montpellier, 2017, [Online]. Available: https://ged.biu-montpellier.fr/florabium/jsp/nnt.jsp?nnt=2017MONTS085.

[31] A. L. Bosser, V. Gupta, A. Javanainen, G. Tsiligiannis, S. D. LaLumondiere, D. Brewe, V. Ferlet-Cavrois, H. Puchner, H. Kettunen, T. Gil, F. Wrobel, F. Saigné, A. Virtanen, and L. Dilillo, "Single-event effects in the peripheral circuitry of a commercial ferroelectric random access memory," *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 1708–1714, 2018, DOI: 10.1109/TNS.2018.2797543.

[32] N. B. Singh, D. K. Rai, and P. Singh, "Design of low power CMOS PSRAM," in *2013 International Conference on Advanced Electronic Systems (ICAES)*, Pilani, India, Sept. 2013, pp. 122–126, DOI: 10.1109/ICAES.2013.6659374.

[33] Infineon, *S27KL0642/S27KS0642 - 64-Mb HYPERRAM™ self-refresh DRAM (PSRAM), HYPERBUS™ interface, 1.8 V/3.0 V, Rev. H*, Infineon Technologies AG, Jan. 2022, accessed on: March 18, 2022. [Online]. Available: https://www.infineon.com/dgdl/Infineon-S27KL0642_S27KS0642_3.0_V_1.8_V_64_Mb_(8_MB)_HyperRAM_Self-Refresh_DRAM-DataSheet-v08_00-EN.pdf?fileId=8ac78c8c7d0d8da4017d0ee8a1c47164

[34] J. Beaucour, J. Segura-Ruiz, B. Giroud, E. Capria, E. Mitchell, C. Curfs, J. C. Royer, M. Baylac, F. Villa, and S. Rey, "Grenoble large scale facilities for advanced characterisation of microelectronics devices," in *2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Moscow, Russia, Sept. 2015, pp. 1–4, DOI: 10.1109/RADECS.2015.7365616.

[35] C. Cazzaniga and C. D. Frost, "Progress of the scientific commissioning of a fast neutron beamline for chip irradiation," *Journal of Physics: Conference Series*, vol. 1021, p. 012037, May 2018, DOI: 10.1088/1742-6596/1021/1/012037.

[36] C. Cazzaniga, M. Bagatin, S. Gerardin, A. Costantino, and C. D. Frost, "First tests of a new facility for device-level, board-level and system-level neutron irradiation of microelectronics," *IEEE Transactions on Emerging Topics in Computing*, vol. 9, no. 1, pp. 104–108, Jan.-March. 2021, DOI: 10.1109/TETC.2018.2879027.

[37] L. M. Luza, D. Söderström, H. Puchner, R. G. Alía, M. Letiche, C. Cazzaniga, A. Bosio, and L. Dilillo, "Neutron-induced effects on a self-refresh DRAM," *Microelectronics Reliability*, vol. 128, p. 114406, Jan. 2022, DOI: 10.1016/j.microrel.2021.114406.

[38] V. Goiffon, A. Jay, P. Paillet, T. Bilba, T. Deladerriere, G. Beaugendre, A. Le-Roch, A. Dion, C. Virmontois, J.-M. Belloir, and M. Gaillardin, "Radiation-induced variable retention time in dynamic random access memories," *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, pp. 234–244, Jan. 2020, DOI: 10.1109/TNS.2019.2956293.

[39] A. Rodriguez, F. Wrobel, A. Samaras, F. Bezerra, B. Vandevelde, R. Ecoffet, A. Touboul, N. Chatry, L. Dilillo, and F. Saigné, "Proton-induced single-event degradation in SDRAMs," *IEEE Transactions on Nuclear Science*, vol. 63, no. 4, pp. 2115–2121, Jul. 2016, DOI: 10.1109/TNS.2016.2551733.

[40] D. Söderström, L. M. Luza, H. Kettunen, A. Javanainen, W. Farabolini, A. Gilardi, A. Coronetti, C. Poivey, and L. Dilillo, "Electron-induced upsets and stuck bits in SDRAMs in the jovian environment," *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 716–723, May 2021, DOI: 10.1109/TNS.2021.3068186.

[41] C. Lim, H. S. Jeong, G. Bak, S. Baeg, S. Wen, and R. Wong, "Stuck bits study in DDR3 SDRAMs using 45-MeV proton beam," *IEEE Transactions on Nuclear Science*, vol. 62, no. 2, pp. 520–526, Apr. 2015, DOI: 10.1109/TNS.2015.2392851.

[42] A. M. Chugg, J. McIntosh, A. J. Burnell, P. H. Duncan, and J. Ward, "Probing the nature of intermittently stuck bits in dynamic RAM cells," *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3190–3198, Dec. 2010, DOI: 10.1109/TNS.2010.2084103.

[43] D. A. G. Gonçalves de Oliveira, L. L. Pilla, T. Santini, and P. Rech, "Evaluation and mitigation of radiation-induced soft errors in graphics processing units," *IEEE Transactions on Computers*, vol. 65, no. 3, pp. 791–804, Mar. 2016, DOI: 10.1109/TC.2015.2444855.

[44] D. M. Fleetwood, “Evolution of total ionizing dose effects in MOS devices with moore’s law scaling,” *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 14 651–1481, Aug. 2018, DOI: 10.1109/TNS.2017.2786140.
[45] S. Mukherjee, Ed., *Architecture Design for Soft Errors*. Burlington: Morgan Kaufmann, 2008, DOI: 10.1016/B978-0-12-369529-1.X5001-0.
[46] S. Mukherjee, C. Weaver, J. Emer, S. Reinhardt, and T. Austin, “A systematic methodology to compute the architectural vulnerability factors for a high-performance microprocessor,” in *Proceedings. 36th Annual IEEE/ACM International Symposium on Microarchitecture, 2003. MICRO-36.*, San Diego, CA, USA, Dec. 2003, pp. 29–40, DOI: 10.1109/MICRO.2003.1253181.
[47] M. Peña-Fernandez, A. Lindoso, L. Entrena, I. Lopes, and V. Pouget, “Microprocessor error diagnosis by trace monitoring under laser testing,” *IEEE Transactions on Nuclear Science*, vol. 68, no. 8, pp. 1651–1659, Aug. 2021, DOI: 10.1109/TNS.2021.3067554.
[48] R. Ginosar, “Survey of processors for space,” in *DASIA 2012 - DAta Systems In Aerospace*, Drubrovnik, Croatia, May 2012, p. 10, [Online]. Available: https://ui.adsabs.harvard.edu/abs/2012ESASP.701E..10G/abstract.
[49] L. Entrena, M. Portela, A. Lindoso, M. Garcia-Valderas, L. Mengibar, L. Parra, J. A. Pulido, and A. Latorre, “Flexible approaches to fault-tolerant microprocessors for space applications,” in *DASIA 2015 - DAta Systems in Aerospace*, Barcelona, Spain, May 2015, [Online]. Available: https://ui.adsabs.harvard.edu/abs/2015ESASP.732E..15E/abstract.
[50] ECSS, “Space product assurance. techniques for radiation effects mitigation in ASICs and FPGAs handbook,” ESA-ESTEC Requirements & Standards Division, Tech. Rep. ECSS-Q-HB-60-02A, 2016.
[51] M. Pignol, “DMT and DT2: two fault-tolerant architectures developed by CNES for COTS-based spacecraft supercomputers,” in *12th IEEE International On-Line Testing Symposium (IOLTS’06)*, Lake Como, Italy, Jul. 2006, pp. 10 pp.–, DOI: 10.1109/IOLTS.2006.24.
[52] K. A. LaBel and M. J. Sampson, “NEPP roadmaps, COTS, and small missions,” in *NASA Electronic Parts and Packaging (NEPP) Program’s Electronics Technology Workshop (ETW)*, Jun. 2016.
[53] F. Bezerra, D. Dangla, F. Manni, J. Mekki, D. Standarovski, R. G. Alia, M. Brugger, and S. Danzeca, “Evaluation of an alternative low cost approach for SEE assessment of a SoC,” in *2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Geneva, Switzerland, Oct. 2017, pp. 1–5, DOI: 10.1109/RADECS.2017.8696219.
[54] S. A. Jacklin, “Small-satellite mission failure rates,” NASA Ames Research Center, Tech. Rep. NASA/TM—2018–220034, 2019.
[55] S. G. E. Wyrwas, “NEPP processor enclave: Post COVID update,” in *12th Annual NASA Electronic Parts and Packaging (NEPP) Program’s Electronics Technology Workshop (ETW)*, Jun. 2021.
[56] M. Nicolaidis, *Soft Errors in Modern Electronic Systems*, 1st ed., ser. Frontiers Electronic Test. Boston, MA, US: Springer, 2011, DOI: 10.1007/978-1-4419-6993-4.
[57] P. Cheynet, B. Nicolescu, R. Velazco, M. Rebaudengo, M. Sonza Reorda, and M. Violante, “Experimentally evaluating an automatic approach for generating safety-critical software with respect to transient errors,” *IEEE Transactions on Nuclear Science*, vol. 47, no. 6, pp. 2231–2236, Dec. 2000, DOI: 10.1109/23.903758.
[58] T. Michel, R. Leveugle, and G. Saucier, “A new approach to control flow checking without program modification,” in *[1991] Digest of Papers. Fault-Tolerant Computing: The Twenty-First International Symposium*, Montreal, QC, Canada, Jun. 1991, pp. 334–341, DOI: 10.1109/FTCS.1991.146682.
[59] M. Rebaudengo, M. S. Reorda, and M. Violante, “Software-level soft-error mitigation techniques,” in *Soft Errors in Modern Electronic Systems*, M. Nicolaidis, Ed. Boston, MA: Springer US, 2011, pp. 253–285, DOI: 10.1007/978-1-4419-6993-4_9.
[60] Z. Alkhalifa, V. Nair, N. Krishnamurthy, and J. Abraham, “Design and evaluation of system-level checks for on-line control flow error detection,” *IEEE Transactions on Parallel and Distributed Systems*, vol. 10, no. 6, pp. 627–641, Jun. 1999, DOI: 10.1109/71.774911.
[61] J. R. Azambuja, M. Altieri, J. Becker, and F. L. Kastensmidt, “HETA: Hybrid error-detection technique using assertions,” *IEEE Transactions on Nuclear Science*, vol. 60, no. 4, pp. 2805–2812, Aug. 2013, DOI: 10.1109/TNS.2013.2246798.
[62] L. Parra, A. Lindoso, M. Portela-Garcia, L. Entrena, B. Du, M. S. Reorda, and L. Sterpone, “A new hybrid nonintrusive error-detection technique using dual control-flow monitoring,” *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3236–3243, Dec. 2014, DOI: 10.1109/TNS.2014.2361953.
[63] M. Portela-Garcia, M. Grosso, M. Gallardo-Campos, M. Sonza Reorda, L. Entrena, M. Garcia-Valderas, and C. Lopez-Ongil, “On the use of embedded debug features for permanent and transient fault resilience in microprocessors,” *Microprocessors and Microsystems*, vol. 36, no. 5, pp. 334–343, 2012, DOI: 10.1016/j.micpro.2012.02.013.
[64] M. Peña-Fernández, A. Serrano-Cases, A. Lindoso, S. Cuenca-Asensi, L. Entrena, Y. Morilla, P. Martín-Holgado, and A. Martínez-Álvarez, “Hybrid lockstep technique for soft error mitigation,” *IEEE Transactions on Nuclear Science*, pp. 1–1, Feb. 2022, DOI: 10.1109/TNS.2022.3149867.
[65] M. Peña-Fernandez, A. Lindoso, L. Entrena, and M. Garcia-Valderas, “Error detection and mitigation of data-intensive microprocessor applications using SIMD and trace monitoring,” *IEEE Transactions on Nuclear Science*, vol. 67, no. 7, pp. 1452–1460, Jul. 2020, DOI: 10.1109/TNS.2020.2992299.