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Technology Dependence of Stuck Bits and Single Event Upsets in 110, 72, and 63-nm SDRAMs

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Abstract

Three SDRAMs from the same manufacturer with technology node sizes 110, 72, and 63 nm, were investigated under proton irradiation and using scanning electron microscopy (SEM). The radiation-induced faults were characterized and compared between the different memory models. The devices under test (DUT) were irradiated with protons and experienced single event effects (SEE) in the form of stuck bits and single bit upsets (SBU). Analysis of the data retention times of bits which had SBU and were stuck during irradiation, showed similar patterns of retention time degradation, suggesting that the SBUs and stuck bits in all three models were likely induced by the same mechanism. Detailed data retention time analyses were also performed before and after irradiation to investigate the evolution of data retention times after irradiation, and after periods of annealing. The largest radiation-induced retention time losses were found to anneal, but the bits least affected directly after irradiation experienced decreasing data retention time as a function of annealing time. SEM imaging showed differences in the memory cell structure between the tested memory models, which were discussed in relation to the radiation sensitivity of the different DUTs.

Index Terms

Proton Irradiation, Radiation Effects, SDRAM, Single Event Effects, Stuck Bits, Technology Nodes

I. Introduction

Single energetic particles can cause different types of faults in electronic components. In synchronous dynamic random access memories (SDRAM), these radiation-induced single event effects (SEE) can be, among others, single bit upsets (SBU) and stuck bits. Different particles have been shown to cause SEE in SDRAMs. Neutrons [1], [2], protons [3], [4], electrons [5], and heavy ions [2], [6] can all induce SEE in such memories.

The basic DRAM cell structure is shown in the schematic drawing in Fig. 1. The individual cells are accessed by a word line (WL) and a bit line (BL), where the WL is used to open an access transistor, which makes it possible to sense the stored charge on the capacitor in the cell through the BL. The cell can be in one of two states: either have stored charge over a certain threshold limit, or under the limit (i.e. no stored charge). These two states can correspond to either '0' or '1' when written, depending on the programming of the device by the manufacturer.

The way the DRAM cell is constructed, the charge that is stored on the cell capacitor will leak out over time through leakage currents of the capacitor and access transistor, or other leakage paths from for instance material defects. To retain the bit information, the memory needs to be periodically refreshed by rewriting the bit values, so the cells with charge stored on the capacitor will not lose their data between write and read operations of the memory. The amount of time a cell can retain its charge so that it returns the charged state value after being written is known as the data retention time.

Stuck bits are bits that have reoccurring errors in such a way that the memory cell returns the same data when it is read (corresponding to the discharged cell state), independently of the value which was written to it. The stuck bits are often intermittently stuck [3], [5], where they are able to operate normally over extended periods of time between being in a stuck state, i.e., the retention time of the cells may vary [7]. The SDRAM cells that are stuck, have been affected by the radiation so that the data retention capability is reduced below the refresh frequency that is used, and the stored charge in these cells leaks out between refresh operations of the memory array. Changes in data retention time of the cells are a useful way to probe the cell damage that has been induced during irradiation [8].

In early studies of stuck bits induced in DRAM and SDRAM, the main discussion of the cause of the faults were towards micro-dose effects [6], [8], [9]. Later studies, and studies on newer devices, have favored a discussion around displacement damage effects from single-particles as the cause of the stuck bits [2], [3], [10], [11]. The generation of defects around the depletion region between the access transistor and the storage capacitor have been identified as particularly important for the creation of stuck bits [10], [11].

New generations of electronic components present different design features compared with their previous generations, along with a steady decrease of topological sizes. In this study, three generations of an SDRAM device from

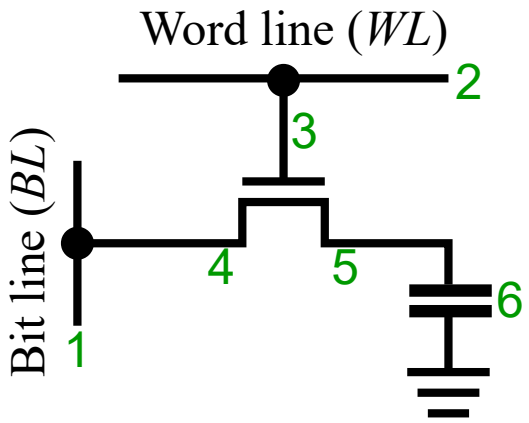


Fig. 1. Schematic view of a DRAM cell, with numbers (green) that will be used for referencing functions of the memory cell later in the paper.

TABLE I
Samples used in the experiments.

Memory model	Technology	Node size (nm)	DUT IDs PSI	DUT IDs RADEF
IS42S16320**B**	Planar	110	B1, B2	-
IS42S86400**B**	Planar	110	-	B3
IS42S16320**D**	RCAT	72	D1, D2	D3
IS42S16320**F**	RCAT	63	F1, F2	F3

the same manufacturer were studied, with technology node sizes of 110 nm, 72 nm, and 63 nm. These SDRAM models are described in Section II-A and Table I.

The memory models were subjected to high-energy proton irradiation to characterize each device response to this particle species, complementing the previously conducted studies, where they were tested with atmospheric neutrons described in [1], and with high-energy electrons, as described in [5]. SBUs and stuck bits were observed and described in both experiments, and in [5] the two fault types were suggested to originate by the same mechanism, due to the similarity in the memory cell retention time degradation for cells that had suffered SBU and those which had been stuck. The same observation was made for different DRAMs studied under neutron irradiation in [12]. This paper goes into greater detail of radiation-induced data retention time changes, and the distributions of data retention time of irradiated memory cells.

Specimen of the memories were also opened and studied under a scanning electron microscope (SEM) to determine variations in the cell structure of the different models, and to relate the memory behavior under irradiation to varying features between the tested SDRAMs. All the tested memories share the basic features depicted in Fig. 1, but with variations in the implementation.

II. Tested devices and experimental procedure

A. Devices under test

The tested components were ISSI 512 Mib SDRAMs of three different generations.
They were models IS42S86320B/IS42S86400B [13] with node size 110 nm, the 72 nm IS42S86320D [14], and the 63 nm IS42S86320F [15]. The 110 nm memory cells were constructed using planar technology, while the 72 nm and 63 nm models utilize a recessed channel array transistor (RCAT) technology [16] for the access transistors to the cell storage capacitors. Three samples of each model were tested: two at PSI and one at RADEF, as listed in Table I.

The memory arrays are composed of 512 Mib divided into four banks, and each bank has 8192 rows and 1024 columns of 16 bits for the -320**X** memory models, while the -400**B** model has 8192 rows and 2048 columns of 8 bits. Their operating frequency is up to 143 MHz and they use a 3.3 V supply voltage. The memories were packaged in 54-pin TSOP-II plastic packages, which were not opened for the irradiation tests.

The components that were tested at PSI were mounted on dedicated test boards, each board housing three devices: one sample of each node size. Apart from the devices under test (DUT), the test boards included a System-on-Chip FPGA from Microchip, a SmartFusion2 M2S025, as the main controller unit.

These test boards were designed to be used for radiation test evaluation of these components on the ground in accelerator-based testing, as well as in space, where the test board is envisioned to fly in the cubesat mission FloripaSat-2 [17], as the *Harsh Environment CubeSat Payload*.

The components tested at RADEF were controlled by Terasic DE0-CV FPGA development boards, utilizing a different test setup and test methodology than what was used in PSI. At RADEF, one DUT were connected to one controller board at a time.

B. Test procedure

1) Tests at PSI: During irradiation, static and dynamic test procedures were utilized. At PSI, a rotating schedule among the three samples on each test board was used, so that a dynamic test was running on one sample at all times, while the other two samples were performing static tests. The procedure was such, that the same pattern (either all '0' or all '1') was first written to the two memories under static test, then a dynamic test was started on the third memory, which consisted of one loop of a March C- test [18], after which the two static test patterns were read back. The procedure is seen in (1). After completion, the test was restarted, but with a different DUT under dynamic testing.

$$\begin{aligned} &S1 \uparrow (w0)\, or \uparrow (w1) \\ &S2 \uparrow (w0)\, or \uparrow (w1) \\ &D \quad \uparrow (w0); \uparrow (r0, w1); \uparrow (r1, w0); \\ &\quad \downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0); \\ &S1 \uparrow (r0)\, or \uparrow (r1) \\ &S2 \uparrow (r0)\, or \uparrow (r1) \end{aligned} \tag{1}$$

In (1), *w* signifies a write operation and *r* a read operation, while '0' and '1' specifies the data patterns all '0' and all '1'. The symbols $\uparrow$ and $\downarrow$ indicate the accessing order of the memory addresses, from the lowest address to the highest, or from the highest address to the lowest, respectively. *S1* and *S2* marks the two memories used for static testing in the current loop, using patterns alternating between all '0' and all '1', and *D* represents the memory that was tested dynamically. The full procedure in (1), including the *S1* and *S2* write and read operations were performed under irradiation.

All operations in (1) were following each other, so the length of one test loop was determined by the read and write time of the memories. To limit the time for one test loop, only the first quarter of the memories bits were used (128 Mib), which resulted in a total time for one test loop of about 3 min 30 s as detailed in (1).

The operational frequency that was used for the test in PSI was 50 MHz in order to have a stable and controlled communication with the three memories on the board, instead of the maximum frequency of the SDRAMs of 143 MHz.

Also, the refresh rate of the memory bits was reduced compared to the nominal one. The nominal value is 8192 refresh operations (one per row in the memory) every 64 ms, which corresponds to sending an auto-refresh command at a frequency of 128 kHz. Instead of this value, the auto-refresh command frequency was set to 32 kHz, with a resulting refresh operation at each bit every 256 ms. This was done to increase the radiation sensitivity of the memories to be able to collect a larger number of errors than at the normal refresh rate.

2) Tests at RADEF: The tests at the different irradiation facilities were not done for the results to be directly compared with each other, but rather to elucidate different types of behaviors, where results from the separate tests can reveal differences between the memory models.

The goals of the tests at RADEF were to investigate the effects of radiation on the SDRAMs, by monitoring the data retention time of the individual bits of the memories. To achieve this, detailed retention time characterizations were made on a portion of the memories. These characterizations were done by writing a data pattern to the memory, then disabling the automatic data refresh for a time period, after which the data refresh was enabled, and the memory was read back. A logical checkerboard pattern, AA_h, was used in this case, and the physical locations of the cells on the dies were unknown. This procedure was then repeated with a different time period with the refresh disabled. Time periods between $1.0{\cdot}10^{-2}$ s and $4.3{\cdot}10^{3}$ s with the memory refresh disabled was used in the characterizations of the devices tested at RADEF.

In the irradiation tests at RADEF, 128 kib of the memories capacity was utilized. With a checkerboard pattern, this corresponds to half of the bits (64 kib) being in their charged state and half in their discharged state. This was

verified by observing the read data pattern when close to all bits were in their upset state. To be able to still collect error events during irradiation with this small memory size, an auto-refresh command frequency of 1024 Hz was used, corresponding to a time of 8 s in between data refresh events in each bit. No errors were present in the tested 128 kib memory of the pristine DUTs at this refresh frequency.

During irradiation, the DUTs were written with a checkerboard pattern, AA_h, then read back and rewritten every minute during the full irradiation period. This procedure is described in (2), with the same nomenclature as in (1), with $t_{wait} = 60$ s, and the operations within brackets repeated.

$$\uparrow (wAA); \{\text{wait } t_{wait}; \uparrow (rAA, wAA)\} \tag{2}$$

The wait time of one minute between the read/write operations of the memory was chosen to have multiple periods of normal data refresh operations (at every 8 s in each bit) in between rewriting the data on the DUTs.

III. Irradiation test facilities

A. PIF

The irradiation tests performed at the Proton Irradiation Facility (PIF) at the Paul Scherrer Institute (PSI) in Switzerland used proton energies of 70, 151, and 230 MeV. The primary proton energy from the PROSCAN cyclotron at PSI was 230 MeV for all three cases, and to reach the lower energies, copper plates were introduced in the beam path to reduce the energy of the protons. Proton fluxes of about $3{\cdot}10^7$ to $8{\cdot}10^7$ p/cm^2/s were used, and all tests were performed in ambient room temperature and air pressure.

The beam homogeneity was checked for each energy setting by moving a small scintillator within the beam area, which was also used to calibrate in-beam ionization chambers used for flux monitoring during the irradiation runs. The reported proton fluence on the DUTs is estimated to have an uncertainty of less than 10 %.

B. RADEF

The Radiation Effects Facility (RADEF) at the University of Jyväskylä in Finland was used for irradiation with 52 MeV protons, which was the energy of the primary proton beam at the target station in air. A proton flux of about $1{\cdot}10^8$ p/cm^2/s was used for the tests at RADEF.

An in-beam ionization chamber calibrated against a Si detector at the DUT position was used to monitor the proton flux during the irradiation tests, and a fluence uncertainty of less than 10 % is assumed.

IV. Results and discussion

A. Cell imaging study

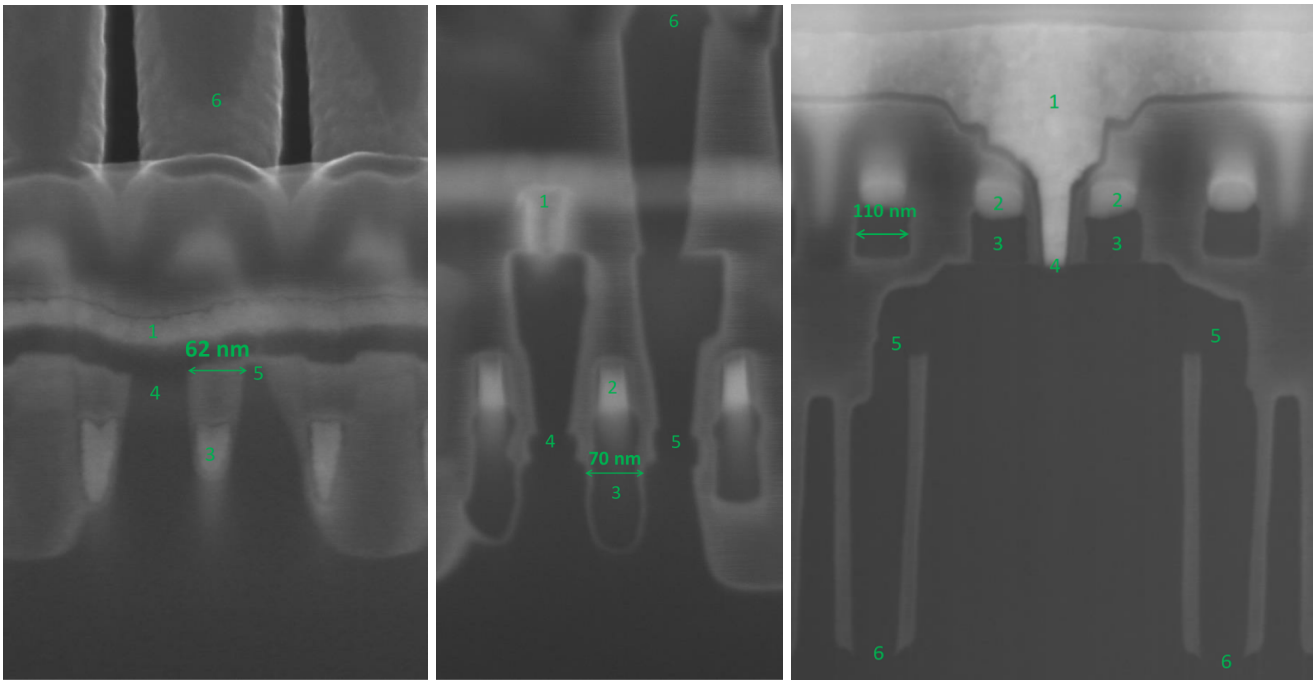
Samples of the three memory models were opened, and imaged with SEM. Cross-sectional views of the memory cells of the different models are shown in Fig. 2, with the scale of the image marked in one of the visible structures in each image. In the images, the numbers *1* to *6* marks structures corresponding to the same numbers in the schematic view seen in Fig. 1.

The devices with the smallest feature sizes are shown in Fig. 2a and Fig. 2b, depicting the memory cells of models F and D, respectively. These memories utilize the RCAT technology for the access transistor, where the gate of the access transistor is marked with number *3* in the images. Due to the RCAT structure of the access transistor, the channel forming under the gate is curved, and the effective channel length of the transistor is longer than the horizontal dimension of the gate.

SDRAM model B has a cell structure as shown in Fig. 2c, built on planar technology. The access transistor gate (*3*), controlled with a bias level on the word line (*2*), opens a straight channel connecting the stored charge in the cell (*5-6*) to the bit line contact (*4-1*). The storage capacitors for the model B are buried in the bulk of the device, below the access transistors and the word and bit lines, while for models D and F, the capacitors are tubes that instead are located above.

B. Fault modes and cross sections, PSI

During proton irradiation, SBUs and stuck bits were observed. An example of how bits with detected errors evolved during irradiation as a function of proton fluence during tests with dynamic mode is shown in Fig. 3, where the results for one tested model B memory (B2 with denominations from Table I) are shown. In the figure, only the proton fluence and errors during dynamic mode is considered, and as discussed in Section II-B1, static tests were performed interleaved with the dynamic tests. This results in an increase of stuck bits in the beginning of the dynamic cycle marked with red vertical lines, since the stuck bits induced during the static runs were observed in the first reads of the DUT in the dynamic test cycle.



(a) (b) (c)

Fig. 2. Cross-sectional microscopic images of the memory cells of SDRAM model F (a), model D (b), and model B (c). The numbers in the images refers to the different parts of the cell as shown in Fig. 1.

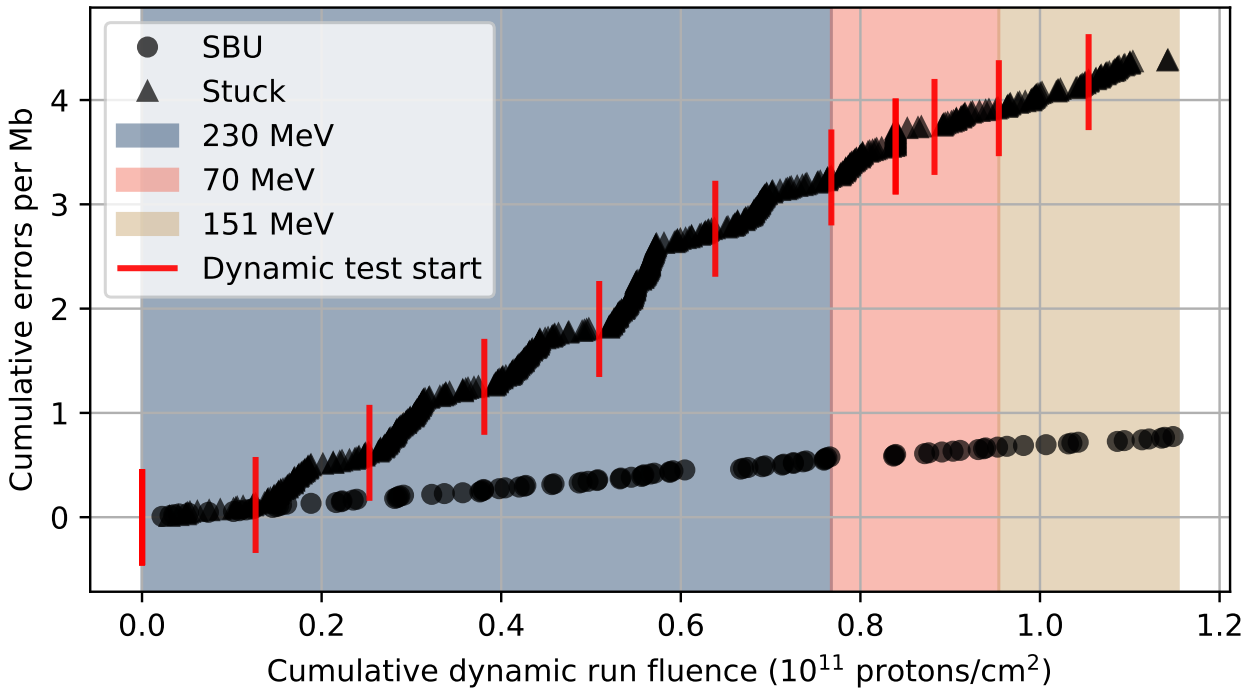


Fig. 3. Example of the error trends found in one DUT during dynamic testing. The figure shows the cumulative number of stuck bits and SBUs in DUT B2 over the fluence of protons with energies 230, 70, and 151 MeV during dynamic testing.

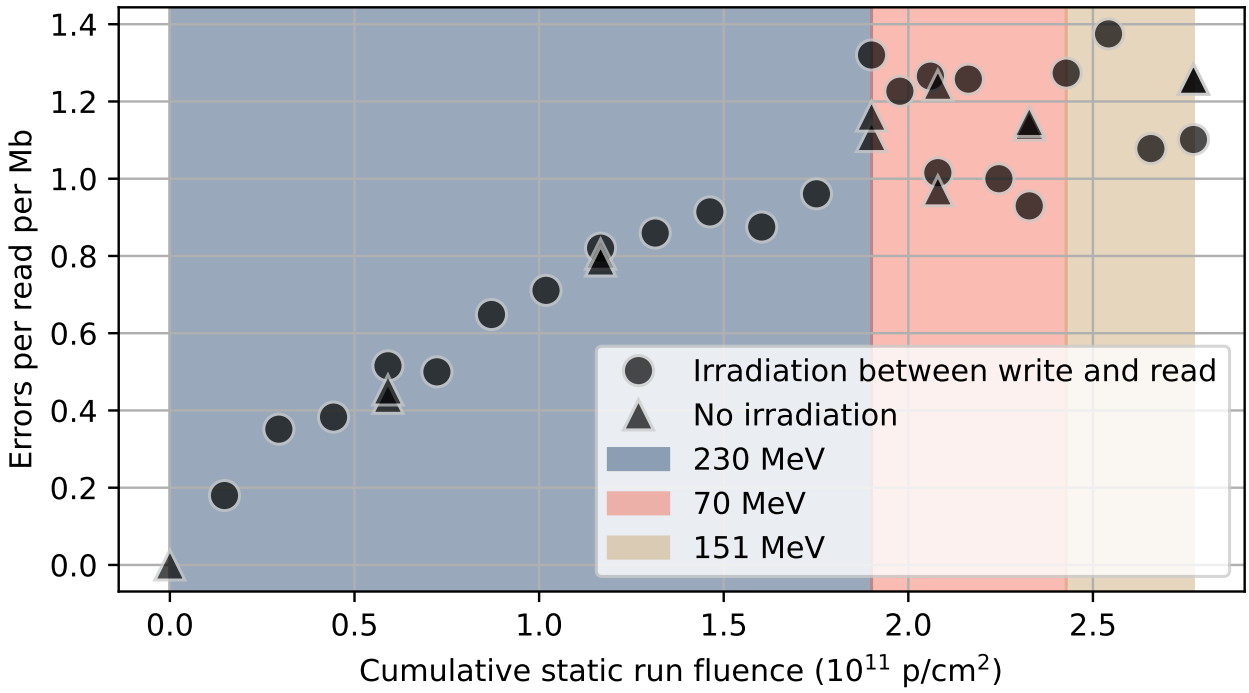


Fig. 4. Errors in a DUT during static testing. The figure shows the number of errors in DUT B2 during each static read, as a function of the acquired fluence of protons with energies 230, 70, and 151 MeV during the static tests of the DUT.

The errors found during static mode tests for the same DUT (B2) is shown are Fig. 4. Here the total amount of errors per read of the memory are presented as a function of the accumulated fluence during the static mode tests. The increasing trend of errors in this figure is due to accumulating stuck bits in the memory over the test duration. Write and read operations were performed also between irradiation runs in the DUTs, with the beam off. The returned errors during these operations are presented with a different symbol in Fig. 4. Since there was no beam on the DUT in these cases, the recorded errors are only caused by stuck bits.

In Figs. 3 and 4, regions of fluence with protons of energies 230 MeV, 70 MeV, and 151 MeV are marked. Cross sections separated in stuck bits and SBUs for the tested energies are presented in Fig. 5. Model D and F have similar cross sections to each other, while model B has a larger error cross section than the other models. The stuck bit cross sections are larger than the SBU cross sections for all memories. Fig. 3 shows this trend for DUT B2.

The bits in the memories which exhibited errors during the irradiation (stuck bits and bits with SBU), were investigated in terms of their retention time and compared with populations of bits with no observed errors. The portion of each tested bit population failing at varying wait times between write and read operations with data refresh disabled is shown in Figure 6 for the DUTs irradiated at PSI. The shown characterization was performed nine months after the irradiation, with the non-error population size fixed to 1000 bits.

The characterization was conducted by writing the targeted memory bits to their charged state, then waiting a period of time, before reading the memory portion back. The waiting time is marked as the retention time in Figure 6.

From the figure is seen that the populations of stuck bits have the worst retention time capability and fail considerably faster than the bits which had not experienced any error during irradiation. The populations of bits with SBUs also have retention time distributions shifted to lower times, but not as far as the stuck bit populations.

The most noticeable difference between the three tested models, is the larger part of the non-error populations failing for model B, compared with D and F. This is further shown and discussed in the following Sections IV-C and IV-D.

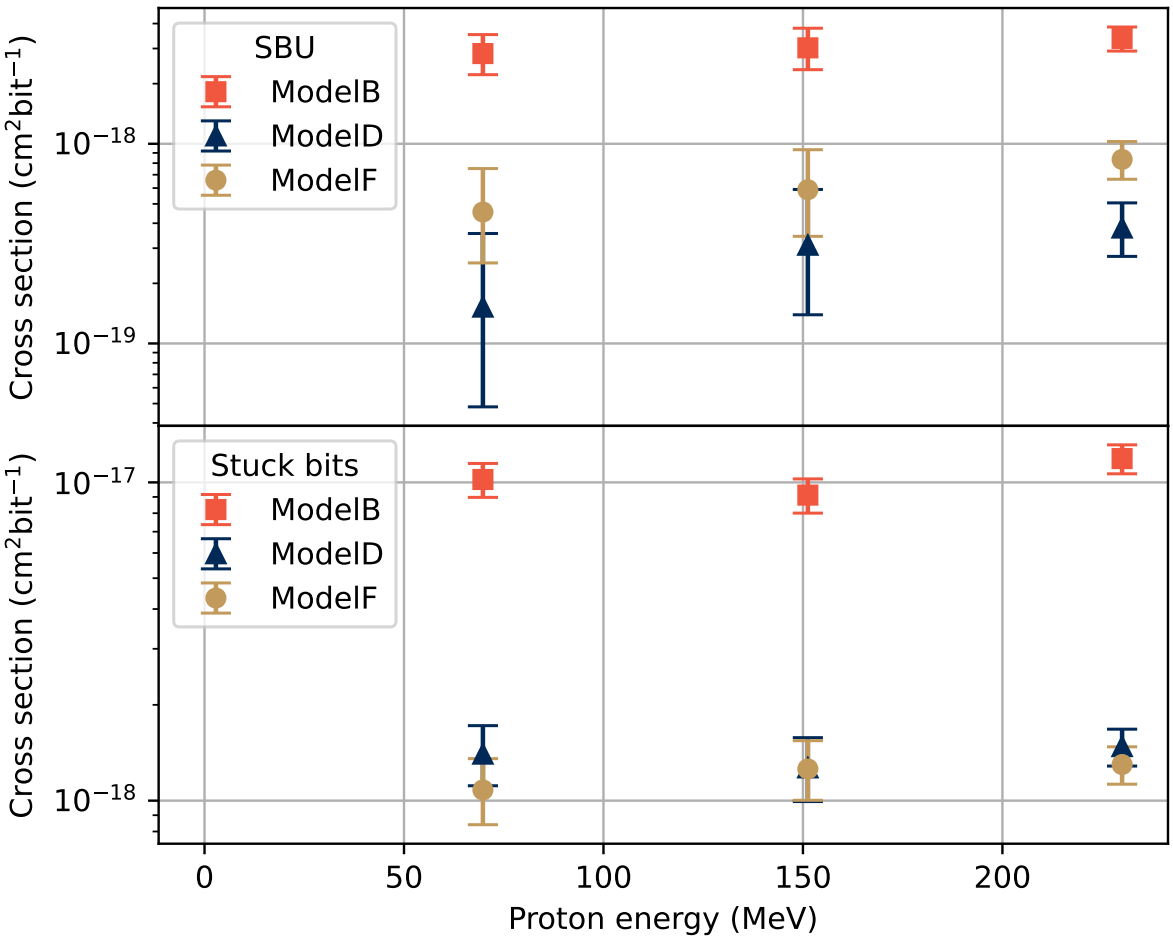


Fig. 5. Error cross sections for SBUs (top) and stuck bits (bottom) for the different memory models, for the tested 128 Mib using a data refresh interval of 256 ms. The events observed during static and dynamic tests have been combined in the figures, as well as the results from DUTs B1 and B2, D1 and D2, and F1 and F2.

C. Retention time distributions, RADEF

A detailed characterization of the memory bits retention times was performed in a 128 kib portion of one sample in each memory model. This was done before and after the irradiation tests, as described in Section II-B2. The degradation of the data retention capability of the memories due to radiation is shown in Figure 7. Here 100 % of bits failing correspond to 64 kib, since half of the used 128 kib were written to the charged state. The bits written to the discharged state will always return the discharged value (without outside stimuli).

In the figure is also shown annealing of the radiation damage one week after irradiation. The annealing was done in room temperature without any electrical connections attached to the memories apart from when it was actively characterized. The retention time distribution of the bits one week after irradiation is shown in Figure 7 with golden colored lines. After one week of annealing DUT D3 and F3 do not show much difference compared to immediately after irradiation, while DUT B3 which suffered larger radiation-induced retention time losses show a larger degree of recovery.

Further annealing steps are displayed in Figure 8. The model B SDRAM which showed the largest degree of radiation damage also shows a larger degree of retention time change after irradiation of the tested bit population. As the time of annealing increases, the most damaged cells with the shortest data retention time after irradiation

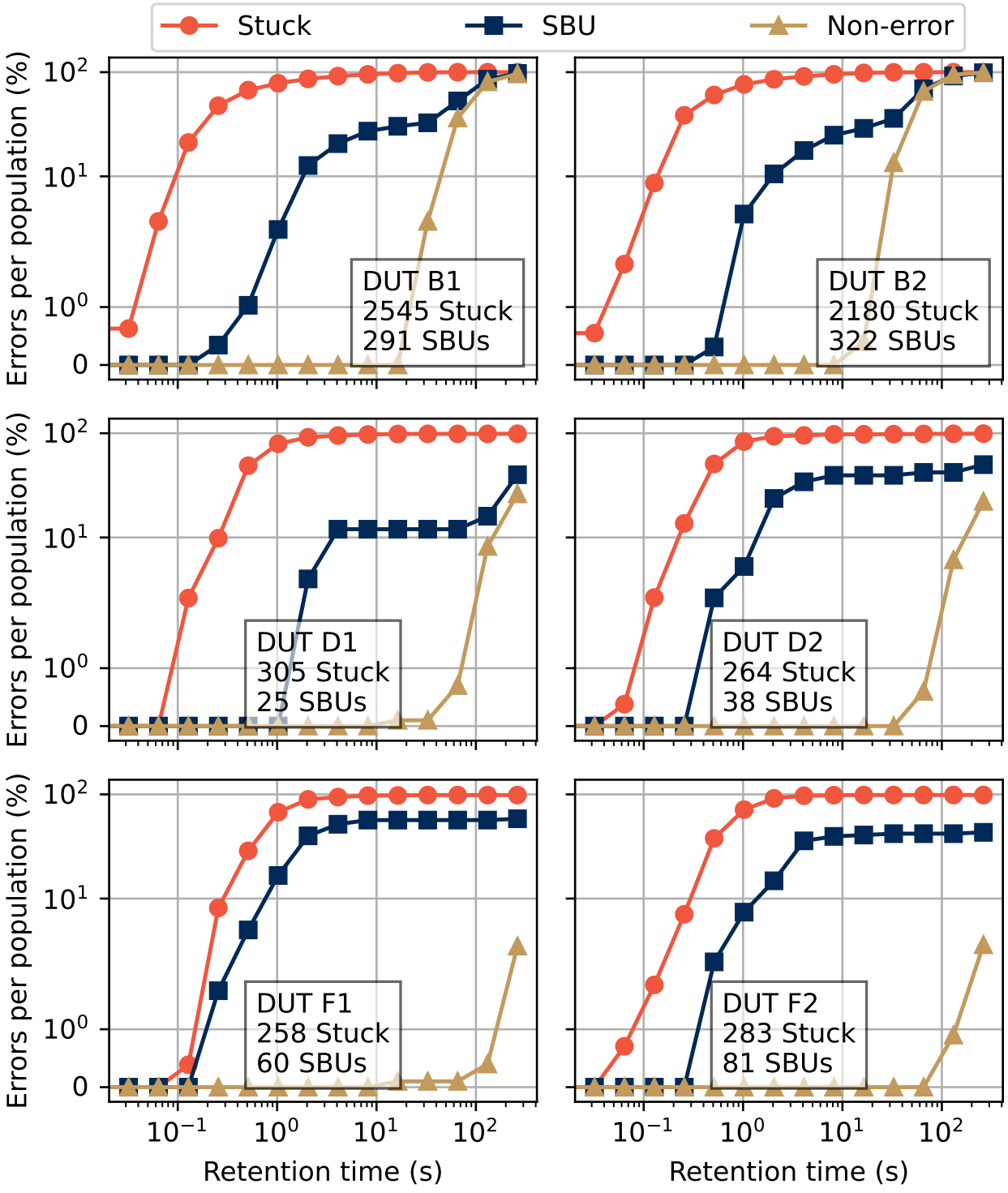


Fig. 6. Retention time distributions of three populations in the DUTs tested at PSI. The populations are: bits that were stuck during irradiation, bits with SBU, and a population of 1000 random bits without observed errors (Non-error distribution).

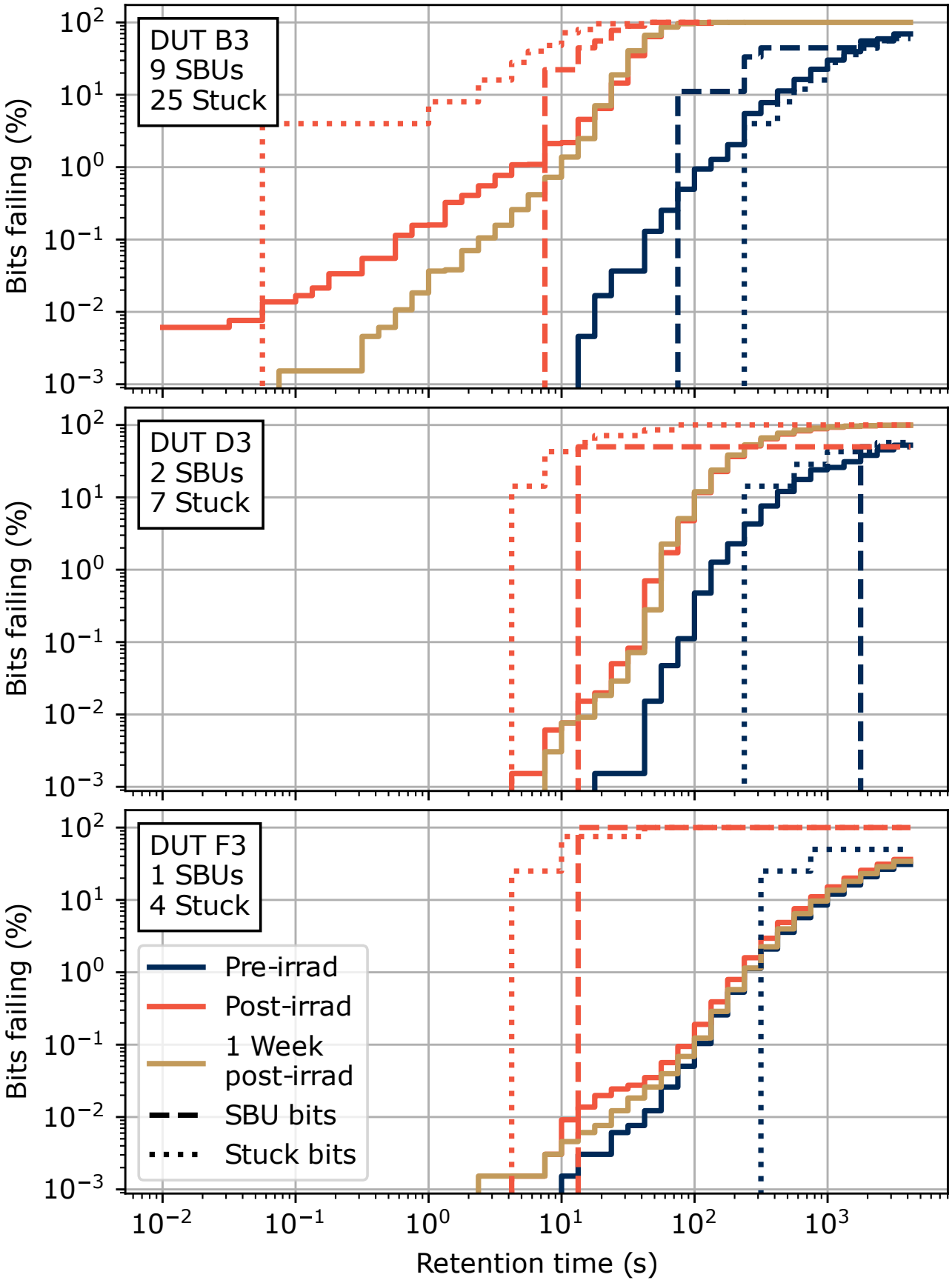


Fig. 7. Cumulative retention time distributions of 128 kib in the three different memory models (DUTs B3, D3, and F3, top to bottom) before and after irradiation, and after one week of annealing. Retention time distributions of the populations of bits with SEE during irradiation are included. All three devices were irradiated with $5{\cdot}10^{11}$ p/cm^2, and the figure legend in the bottom frame is valid for all frames of the figure.

gets longer retention times with several orders of magnitude. In the figure is also seen that the distribution shifts to a more vertical orientation, as the bits with longer retention times gets decreased data retention capabilities as the annealing time increases. A similar behavior was seen in [5] for the same memory model, and could be caused by the migration of trapped charges within the insulating oxides over time. This annealing characteristic, and the global shift of the full population of bits to shorter retention times in Fig. 7 suggest a strong effect of total ionizing dose (TID) on the observed retention times for the bits is DUTs B3 and D3 after irradiation.

The annealing effects of the model D and F DUTs were not as large as was seen for DUT B3. The same trends can however not be excluded, with the slight decrease of data retention time magnified in the inset of Figure 8 for DUT D3 at longer annealing times, and small retention time increases of the bits with the shortest retention times after irradiation.

The dashed and dotted lines in Figure 7 represent the cumulative distributions of retention times of the population of bits that had SBUs, and bits that became stuck from SEE during irradiation. The distributions are shown for these bits before and after irradiation in blue and orange respectively. Only few SEEs were observed due to the small portion of the memory that was considered, so each failing bit in the SBU and stuck bit populations cause a large jump of the dashed lines in Figure 7.

A time of 8 s between refresh events of each bit was used in the DUTs under irradiation. In Figure 7 it is seen that the bits which suffered SBUs (one single non-reoccurring error in the bit) have retention times after the irradiation only slightly larger than the time interval between refresh events during the irradiation test, while the stuck bits have data retention times reaching shorter times than the refresh time interval.

From the nature of the error modes, the expected behavior of the stuck bits would be exactly this, that they have shorter data retention times than the time between the data is refreshed, and the stored charges on the cell capacitor leak out between refresh events. The stuck bits can however anneal over time, and are often intermittently stuck [4], [5], thus the full population of observed stuck bits would not be expected to necessarily have retention times shorter than the refresh time interval.

Regarding the SBU bit populations, there is also here a shift towards shorter retention times after irradiation compared with before. This is most notably present for samples D3 and F3, where in e.g. F3 the only bit which had an SBU were not failing during the tested wait times of up to $4.3{\cdot}10^3$ s before irradiation. The large decreases of retention time for SBU bits point also here towards that stuck bits and SBUs in these types of memories are likely induced by the same mechanisms.

An exception is found for the case of DUT B3, where only one of the two observed SBUs is failing in the retention time characterizations made for Fig. 7. This is due to that the SBU bit not showing up is an error where the bit was written to the discharged state, and the read returned the state corresponding to a charge stored in the cell capacitor. All other observed SBUs has been from cells written to the charged state and returning a value corresponding to a discharged state, which is the case also for all observed stuck bits, as would be expected. The SEE mechanism causing the cell to return a value corresponding to a charged state is different from the opposite case. Examples of causes would be for instance a particle strike occurring at the time of reading the bit value that induces a charge pulse on the BL so the sensing node would interpret this as the bit being in the charged state.

In the case of DUT B3, many bits were becoming stuck due to cumulative radiation effects towards the end of the irradiation, where the accumulation of stuck bits in the memory follows a power law as a function of proton fluence to account for the multiple particle interactions which caused these bits to be stuck [3], [5]. This is shown in Figure 9, where the linear part of the figure represent the stuck bits induced by single protons, and which are used for creating the retention time distributions of SBU bits and stuck bits in Figure 7 for DUT B3. The stuck bits induced by cumulative radiation effects follow the power law part of the fit. The limit between the SEE and cumulative parts was set as $3.9{\cdot}10^{11}$ protons/cm^2.

The cumulative effects in this case is likely a combination of TID on the device, and the accumulation of multiple smaller damage clusters in the cell which together cause a large enough leakage path from the cell capacitor to cause the bit to be stuck. As discussed in relation to Fig. 8, a large part of the cumulative damage likely originate from TID, where the annealing characteristics show signs of charge migration. No clear deviations from a linear trend of induced errors as a function of proton fluence was observed for DUT models D and F, or for model B before the drastic change in error rate as seen in Fig. 9. These observed stuck bits and SBUs thus likely originate from single particle events.

D. Technology and node size dependence

The model B memory has the larger SEE cross section, as can be seen in Fig. 5, while memory models D and F have very little difference between them in terms of SEE sensitivity. Model B is the oldest device with the largest

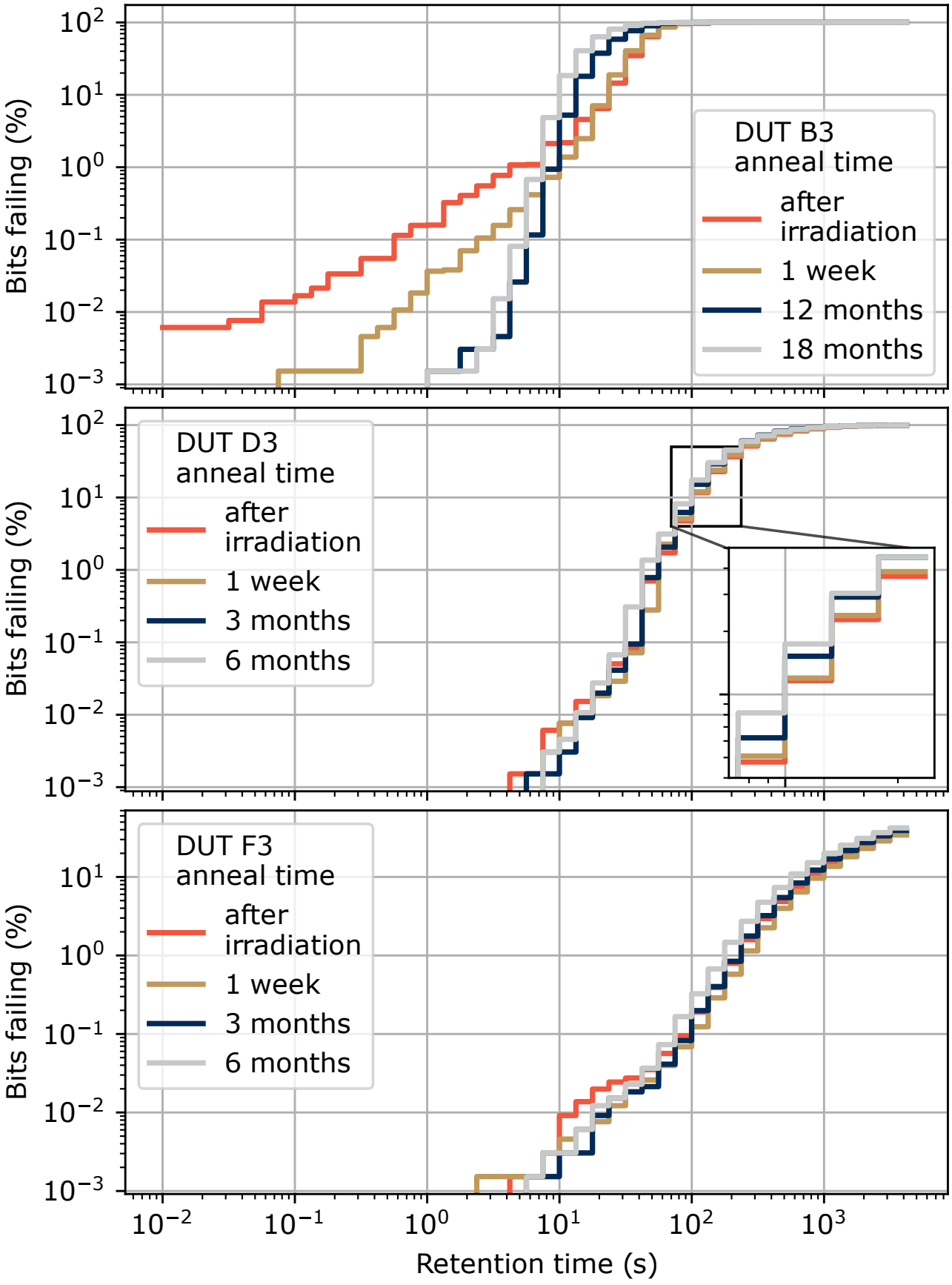


Fig. 8. Cumulative retention time distributions of 128 kib in DUTs B3, D3, and F3, top to bottom, after irradiation at different times of annealing.

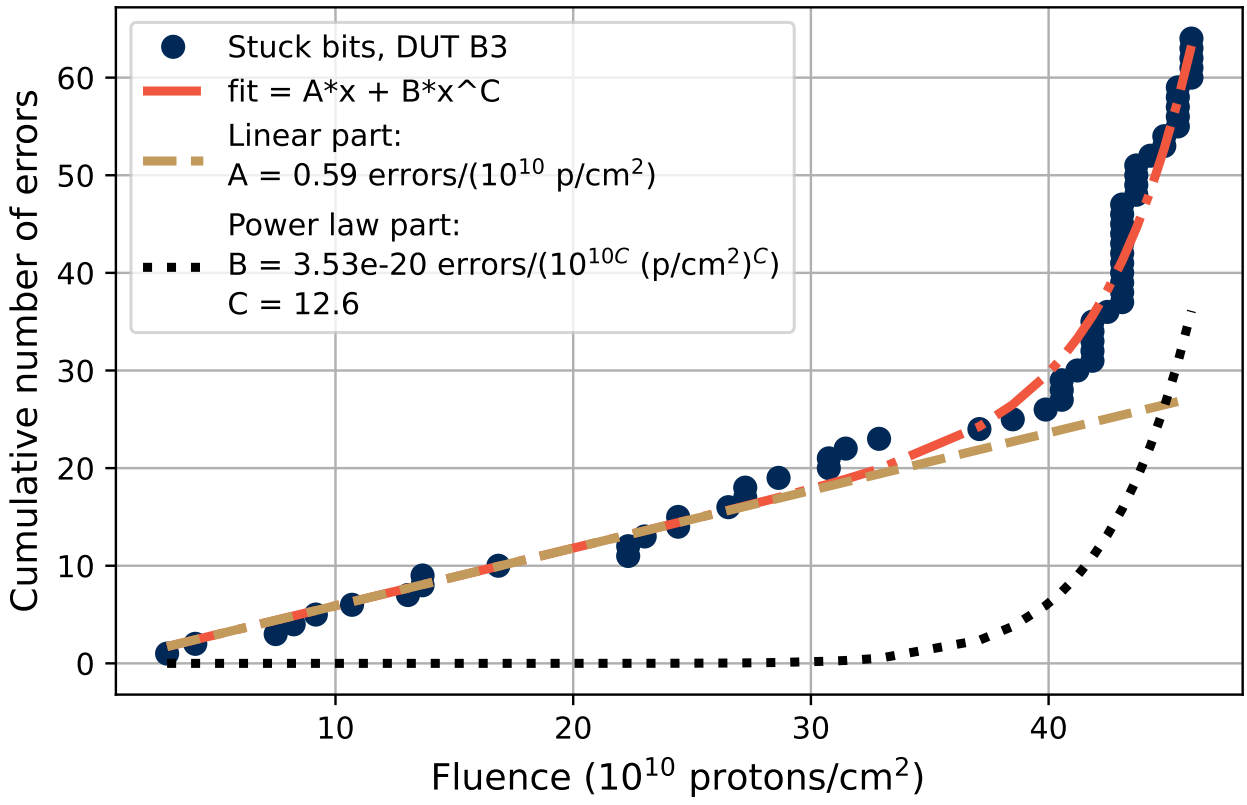


Fig. 9. Cumulative number of stuck bits as a function of proton fluence observed in the memory B3 during irradiation at RADEF. The number of accumulated stuck bits was fitted to a function $A \cdot fluence[10^{10}\text{p/cm}^2] + B \cdot fluence[10^{10}\text{p/cm}^2]^C$, where *A*, *B* and *C* are fitted constants.

technology node size, and a larger cell area might translate to a larger sensitive area, where a proton strike is able to generate an SEE in the memory cell [19].

However, shrinking of device cells technology node sizes can lead to larger bit upset cross sections. Smaller technology nodes are often associated with lower operating voltages and smaller stored charges, and lower-energy ion recoils and reaction products that are induced by the incoming protons could be able to generate SEEs in the device. Another trend when moving towards smaller memory cells and newer devices is the incorporation of new device features and material improvements, which often lead to reduced sensitivity to radiation and other parasitic effects [20].

As depicted in Fig. 2, a design change of the memory cells took place comparing model B with D and F, going from a planar cell architecture to an RCAT structure of the access transistor. This resulted in a drop of SEE bit cross section of close to 10 times for stuck bits, and 5-10 times for SBUs. The vertical structures of the cells are also very different from model B to D, so the generated secondaries by the proton radiation traversing the region of the access transistor and the storage capacitor (area *5* in Fig. 2) might differ considerably. This will affect the likelihood of creating defects and damage clusters in the area, and thus leakage paths for the stored charge of the cells to dissipate through.

The retention time distribution curves presented in Section IV-C reveal a larger collective loss of data retention capability after irradiation for DUT B3 than D3, and for D3 than F3. Looking at Fig. 2c, there is a large insulation structure present from the access transistor (*3*), down to the storage capacitor (*5-6*), isolating adjacent cells from each other. Charged particles passing through this structure can induce electron-hole pairs which might not recombine in the presence of electromagnetic fields generated from biases on close WLs or BLs resulting in charges trapped in the oxide. These trapped charges can then accumulate by the bulk silicon and insulator interfaces, interacting with the charges stored on the cell capacitor and charge carriers in the access transistor, resulting in a disturbance of the cell operation and increased leakage current in the access transistor. This effect is likely the strongest cause of

the shift to the left in Figure 7 of the full 128-kib populations.

The layout of SDRAM models D and F differ from B, as seen in Fig. 2. Around the WL contacts and on the path around the access transistor, there is a thicker insulator layer present for model D than F. This could be the cause for the larger collective loss of retention time seen for DUT D3 than F3 in Fig. 7. There the whole population of bits have shifted noticeably to lower retention times after irradiation for DUT D3, but the retention times of F3 are fairly similar for times over 10^2 s before and after irradiation.

V. Conclusions

Three generations of SDRAMs from one manufacturer were studied under high-energy proton beams, where SEUs and stuck bits were observed, and the error cross sections were compared between the different models. The different memories were opened and imaged using SEM to study the memory cell structures. It was found that the memory cells with the planar structure were more sensitive to SEE than the ones with RCAT structure in the study.

The SEEs observed in the tested memories did not occur in bits which were the weakest in terms of the measured data retention time before irradiation. However, there is a shift of data retention capability towards shorter retention times for bits which experienced either SBU or were stuck.

Both observed SEE failure modes, SBU and Stuck bits, are likely caused by the same mechanism induced by single high-energy protons. This was found due to the similar loss of data retention time observed in bits which experienced SBU and that were stuck. The bits which were stuck were found to have a larger loss of retention time than the SBU bits, pointing towards that the SBU in these SDRAMs are less severe versions of stuck bits. An exception of this is the case of an SBU observed in DUT D3, where the returned value from the bit corresponded to a charged state, even though it was written to the discharged state. All other observed errors corresponded to bits returning values corresponding to the discharged state after being written to their charged states.

The TID causing retention time losses in the tested SDRAMs seem to be closely related to the oxide present around the access transistor and stored charge in the memory cells. The three tested models showed a different response in the amount of retention time lost for the whole tested bit population, where the model with the least oxide present close to the access transistor was the least affected.

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