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Abstract— **A new method is presented to test dynamic parameters of Analogue-to-Digital Converters (ADC). A noisy and nonlinear pulse is applied as the test stimulus, which is suitable for a multi-site test environment. The dynamic parameters are predicted using a machine-learning-based approach. A training step is required in order to build the mapping function using alternate signatures and the conventional test parameters, all measured on a set of converters. As a result, for industrial testing, only a simple signature-based test is performed on the Devices-Under-Test (DUTs). The signature measurements are provided to the mapping function that is used to predict the conventional dynamic parameters. The method is validated by simulation on a 12-bit 80 Ms/s pipelined ADC with a pulse wave input signal of 3 LSB noise and 7-bit nonlinear rising and falling edges. The final results show that the estimated mean error is less than 4% of the full range of the dynamic specifications.**

Keywords-ADC;test; pulse wave;machine-learning-based

I. INTRODUCTION

Nowadays, the platform-based designs for multi-media and communication applications usually contain mixed-signal devices. An ADC is the typical mixed-signal device in these systems, being an interface between the analogue world and the digital circuits of the platform. In order to adapt the development of the systems, the speed and resolutions of the ADCs have to be increasingly higher, which raises the cost of testing significantly. For this reason, reducing the cost of the ADC testing is demanded.

In the conventional dynamic testing of ADCs, a high-quality analogue sine wave is applied as the test stimulus. The output spectrum is extracted by the well-known FFT analysis. All the dynamic parameters, like total harmonic distortion (THD), signal-to-noise ratio (SNR), signal-to-noise and distortion (SINAD) and spurious free dynamic range (SFDR), can be calculated from the output spectrum [1]. The requirement of a high quality analogue input stimulus is the main reason why reducing test cost is difficult.

Recently, much research on machine-learning-based testing for RF or mixed-signal circuits has been carried out. In [2], a high-speed ADC is tested on a low cost tester. Generating an accurate and high frequency sine wave for the dynamic test of a high-speed ADC is very expensive in a production test environment. In order to overcome this difficulty, one generates a high-frequency data source by mixing two low-frequency signals by mixers. Band-pass filters are applied to extract the desired signal, of which the frequency is the sum of the two low frequencies. However, the quality of the extracted signal is not sufficient to obtain the dynamic parameters accurately. As a result, a prediction function is generated by the multivariate adaptive regression splines (MARS) [3] and the data of training devices. Finally, by the prediction function, the values of the dynamic parameters with a certain amount of errors can be predicted from the signature results. The work in [4] focused on the loop-back test of the ADC and the Digital-to-Analogue converter (DAC). The signature results are used to predict the dynamic parameters of both the ADC and DAC in a loop-back test. The MARS algorithm is exploited to generate the mapping function as well as in reference [2]. By the mapping function, indicating the relationships of the outputs among the ADC, the DAC and the loop channel, the fault-mask problem of the loop-back test can be solved. This approach is very interesting because they avoid the need of external high-cost analogue generator. But considering only the test of an ADC there is a need of a DAC and additional circuitry to realize an analogue signature generator between the two converters. The authors in [5] propose a low-cost built-in test for RF circuits by using an envelope detector. Compared with the nominal frequency of RF circuits, a relatively low-frequency two-tone signal is applied as test stimulus. The envelope detection of the output is obtained by an on-chip envelope detector. Subsequently, its wavelet coefficients can be calculated by analyzing the output of the envelope detector with the wavelet transforms. They are then mapped to the specification space of the DUT by the mapping function. This solution is also interesting considering that it is used to test RF components that are the most expensive analogue components to test. But as for the previous solution there is a need of additional circuitry (envelope detector) to generate signature.

Considering previously cited test methods, we propose a similar machine-learning- based approach, using alternate signature to predict conventional test parameters. But for our solution, we minimize the need of additional circuitry to generate stimulus and to capture signatures. In our previous work [6], the out-of-range percentage (ORP) is exploited as the signature result to distinguish the faulty devices from the fault-free devices. Instead of a high-quality analogue sine

wave, an adapted pulse is applied to obtain the signature result, which is more appropriate to implement in a multi-site testing environment. In this paper, we propose a machine-learning-based test for ADC, estimating the accurate dynamic specifications based on the *ORP*.

II. BASIC CONCEPT OF MACHINE-LEARNING-BASED TESTING

The basic concept of the machine-learning-based testing is shown in Figure 1. As depicted in the figure, one can obtain the results of the desired parameter by signature measurements. The way to connect them is using a mapping function based on their strong correlation. In contrast with conventional testing, machine-learning-based testing obtains the results of the specifications of the DUTs in an indirect way. Instead of the specifications, the signature results are measured with unconventional test stimuli or post-processing methods. The key issue in machine-learning based-testing is that the signature results must have a strong correlation with the specifications. In such a case, a mapping function can be built by the training of test data. Once the mapping function is built, the specifications can be estimated from the signature results.
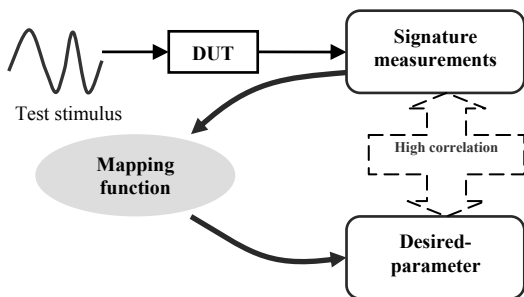

Figure 1: Basic concept of machine-learning-based testing [2]

Usually, MARS is selected to build the mapping function, being popularized in 1991 by Friedman [3]. One can consider it as an extension model from the linear regression model with more flexibility. The main purpose of the MARS analysis is to predict a dependent variable from a set of independent predictor variables. It builds the model described as in [3]:

$$\hat{f}(x) = c_0 + \sum_{i=1}^{k} c_i B_i(x) \qquad (1)$$

, where x is the predictor variable, $B_i(x)$ represents the basic function and c_i represents constant coefficient. It is a weighted sum of the basic function. The MARS algorithm selects a set of the basic functions to maximize an overall least squares goodness-of-fit criterion [4].

III. PROPOSED TEST METHOD

The overview of our machine-learning-based test method is shown in Figure 2. First, a set of ADCs is selected as the training set. The test data is used for building the mapping function. For an accurate prediction of the

specifications, it is recommended that the training set can cover all corner cases.

Second, each device in the training set has to be tested twice via the signature-based testing and the conventional specification testing.

Third, after collecting both of signature as well as the specification results, a mapping function can be built by the MARS algorithm. This function can map the signature results to the specification space.

Subsequently, only the signature-based testing is applied to the DUTs. Once the signature results are obtained, the estimated specifications can be calculated by the mapping function built before. The details of the whole process will be presented later.
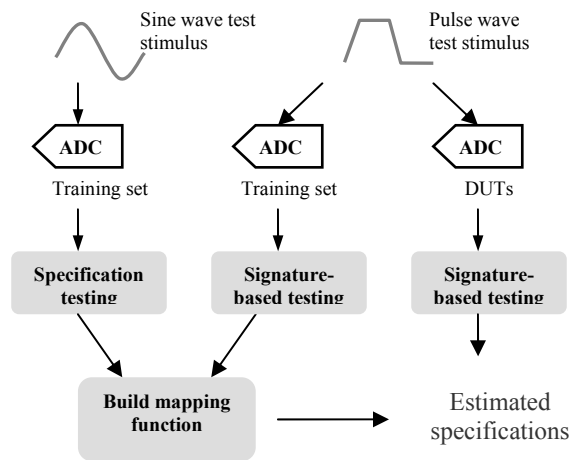

Figure 2: Overview of the proposed test method

In our approach, a pulse wave with noise and non-linear edges is applied as the realistic test stimulus for all the DUTs. Obviously, such a low-quality pulse wave is easier and more inexpensive to generate than a high-quality analogue sine wave as used for conventional testing. Nowadays more and more ADCs are integrated into a platform-based design, which often contains also the digital parts like memories and multiple-processor cores. When using a pulse wave as the test input signal, an appropriate setting of the rising and falling edges is crucial for testing an ADC correctly. If the rising or falling edge is too steep, the sampled digital output will be only the digital codes representing the high and low levels of the pulse wave. Obviously, it contains no useful test information of the ADC under test. According to the Nyquist theory [1], the rising or falling time of the input pulse wave should be at least larger than the reciprocal of the sampling frequency of the ADC.

A. Conventional specification testing of the training set

The desired conventional dynamic specifications, SFDR, THD, SINAD and SNR are measured by the conventional test method using an analogue sine wave.

B. Signature-based testing for the training set

The flow of the signature testing is shown in Figure 3. In our previous work [2], we proposed signature testing to

filter out the faulty devices from the fault-free devices by the signature *ORP*. This is an analysis in the time domain, which is simpler than the FFT analysis in conventional testing. The basic idea is using *ORP* to define the similarity between the outputs of the golden devices (fault-free devices defined by the specification testing) and the DUTs. Based on the degree of similarity, the faulty devices can be distinguished. In this work, the signature testing included in the machine-learning-based testing is based on the signature *ORP* but with some differences, as now it is used as a variable to predict the actual specifications. In the original work, a certain amount of the golden devices are used as reference devices, which have to be fault-free. In this work, the training devices are used as the reference devices. However, they do not have to be all fault-free. The specific steps are explained as follows:

Step 1: Assume the specification parameter *Spec* (for example, the THD) is the required one to be predicted by the signature results later. All the values of *Spec* of the training set can then be sorted in ascending or descending order. After that, an array of *Spec* can be obtained: *Spec (1), Spec (2)...Spec (i)...Spec (n)*. The parameter *n* is total number of the ADCs in the training set. The corresponding training device of each *Spec (i)* can be assumed as *train (i)*.

Step 2: Divide all the elements in the array *Spec* evenly into a number of ranges. If there are *m* ranges as shown in Figure 3, then these ranges will be:

$$[Spec(1), Spec(1+\lfloor n/m\rfloor)],$$
$$[Spec(1+2*\lfloor n/m\rfloor), Spec(1+3*\lfloor n/m\rfloor)]...$$

Step 3: As shown in Figure 3, the pulse waves with the same period, amplitude, rising and falling edges are applied to all the ADCs in the training set. By applying the time modulo plot [7] to the output, the number of periods of pulse waves can be transferred to only one period waveform without losing any test information. This technique shows the output waveform in a more clear and simple way for later analysis [6]. For each device, an array of the output amplitude can then be obtained as:

 Am (1), Am (2), Am (3)... Am (n)

Each element *Am (i)* represents the amplitude of one sampling point on the output curve.

Step 4: For each range defined in step 2, the maximum amplitude Am_{max} *(i)* and minimum amplitudes Am_{min} *(i)* of each sampling point can be determined. They are obtained by comparing the output amplitude of the corresponding devices of each range. The acceptable amplitude range of the ith sampling point of one certain range can then be defined as [Am_{min} *(i)*, Am_{max} *(i)*].

Step 5: Verify if each amplitude element *Am (i)* of one ADC in the training set is within the range [Am_{min} *(i)*, Am_{max} *(i)*]. If it is within the range, the deviation from the range *ΔAm (i)* is defined as zero. Otherwise, it is defined as:

$$\Delta Am\ (i) = Am\ (i) - Am_{max}\ (i) \tag{2}$$

,when *Am (i)* is larger than Am_{max} *(i)*.

$$\Delta Am\ (i) = Am_{min}\ (i) - Am\ (i) \tag{3}$$

,when *Am (i)* is smaller than Am_{min} *(i)*.

Step 6: After finishing collecting the deviation of all the sampling points for one certain range, the *ORP* of one ADC can be calculated as [2]:

$$ORP = \frac{\sum_{i=1}^{N}\Delta Am(i)}{\sum_{i=1}^{N}Am_{max}(i) - \sum_{i=1}^{N}Am_{min}(i)} \tag{4}$$

If there are *m* ranges in total, then *m* different *ORP*s can be obtained as:
ORP (1), ORP (2) ... ORP (m)
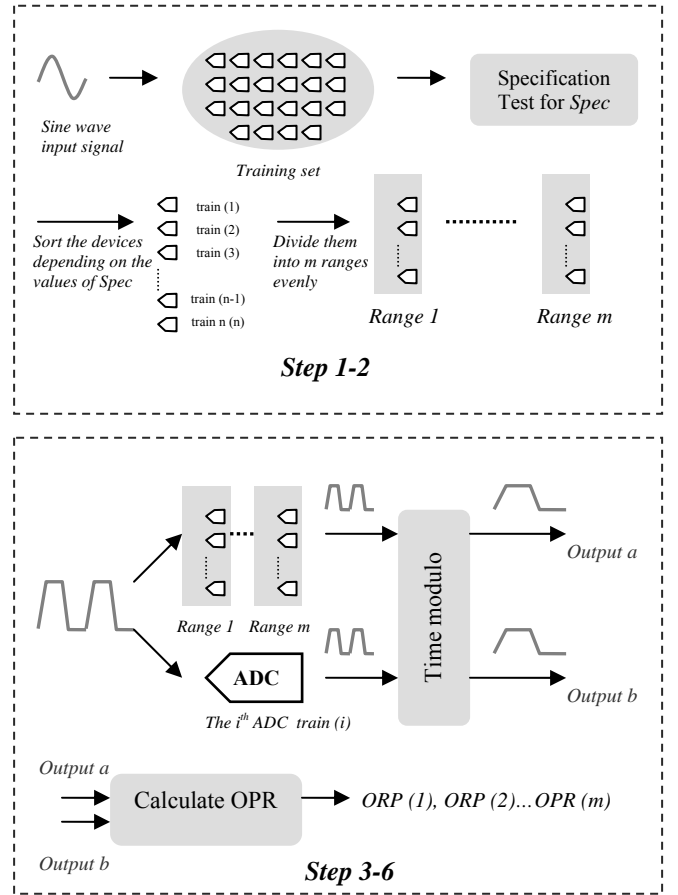

Step 1-2

Step 3-6

Figure 3: Test flow of the signature-based testing of the training set

C. Build Mapping Function

In this method, we use the MARS algorithm to build up a mapping function. As shown in Figure 2, the inputs of the algorithm are the specifications and the signature *ORP* of the training set. Later on, a mapping function that can map the ORP to the dynamic specifications can be extracted.

D. Signature-based Testing for the DUTs

When calculating the *ORP* of the DUTs, the same methodology as the training set is exploited. The test input signal has the same parameters as the signature testing of

the training set. In contrast to the signature testing of the training devices, only the steps 3, 5 and 6 are carried out on the DUTs. The acceptable ranges of the amplitudes for calculating the *ORP* are still the ones obtained from the training set.

E. Estimate the specifications of the DUTs

At the end, one can just substitute the variables of the mapping function with the *ORP* values of the DUTs. The results of the mapping function will be the estimated values of the corresponding specifications.

IV. DEVICE-UNDER-TEST MODELLING

In order to validate our method, an on-chip 12-bit 80 Ms/s pipelined ADC has been selected as the target device. It is modeled at the behavioural level using Labview. The pipelined ADC is a very popular choice in high-speed and high-resolution applications [8]. The key advantage of the pipelined ADC is the high conversion rate, high resolution, well dynamic performance and low power consumption. The architecture of this 12-bit ADC is shown in Figure 4, on which the Labview model of the ADC is based. It consists of ten stages. The first two stages are 2.5 bits, the seven stages in the middle are 1.5 bits and the last stage is 2 bits. The first stage is only a coarse conversion. In the second stage, the difference signal between the original input and the first stage output is converted. In this way, the input signal is converted stage by stage. At the end, the results of every stage are combined to achieve a high-resolution output. The basic architecture of each stage is identical, which is denoted by the dashed line in Figure 4. Its major parts are a residue amplifier, an analogue adder, a 1.5-bit ADC and a 1.5-bit DAC. Usually the ADC in the sub-stage is implemented by a flash ADC. As the resolution of a sub-stage is very low, only a few comparators are required to build up the flash ADC. The amplifier, adder and DAC blocks are implemented by a multiplying DAC (MDAC) [9].
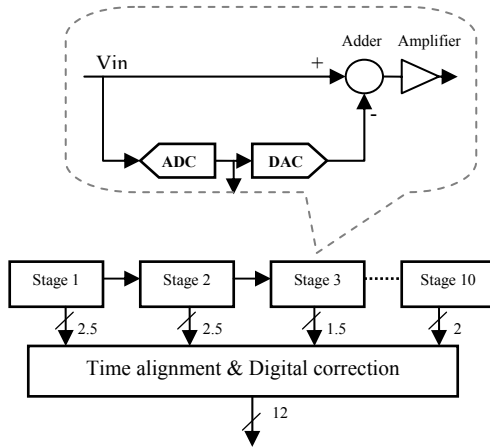

Figure 4: The basic architecture of the 12-bit pipelined ADC

In the Labview model of the 12-bit pipelined ADC, there are several key parameters that can affect the performance of the ADC:

1) The reference voltages of the comparators in the flash ADC of each sub-stage
2) The values of the capacitors in the MDAC of each sub-stage
3) The gain of the residue amplifier in the MDAC of each sub-stage

These parameters will be changed depending on the process variations in the fabrication. For this reason, independent Gaussian noise sources are added to all these key parameters respectively. As a result, the values of these parameters are generated randomly to emulate the devices with the process variations.

V. SIMULATION OF THE PROPOSED METHOD

A. Simulation setup

In the simulation of the proposed method, 2000 training sets are used to build mapping functions and 1500 test sets to evaluate the method. They are generated randomly by adding Gaussian noise to the key parameters of the ADC model. The specification is tested by a perfect sine wave of frequency f_{in}=38 MHz, a sampling frequency f_s=80 MHz and the number of samples is N=4096.

For the pulse-wave input signal of the signature-based test, the rising and falling edges are modeled with 7-bit non-linearity as suggested in [10]:

$$x(t) = v_{os} + \eta[t + 0.04*(t^2 - t)] + n(t) \qquad (5)$$

, where v_{os} is the offset voltage, η is the slope and $n(t)$ denotes the noise. The part $0.04*(t^2 - t)$ corresponds to the 7-bit nonlinear property of the signal. For the entire pulse wave, a Gaussian white noise has been added. All the simulations have been performed with an adapted pulse wave of input frequency f_{in}=38 MHz, rising or falling time T_r / T_f = 6 ns, a sampling frequency of f_s=80 MHz, and the number of samples is N=4096.

The MARS algorithm is implemented by using existing software. It has two functions:
1) Build the mapping function by the specifications and the signature results from the training data.
2) Predict the specifications of the DUTs by the signature results and the mapping function built in 1).

In signature testing, the number of ranges *m* determines how many variables are in the mapping function. In order to see its impact on the estimated specifications, different values of *m* have been applied in the simulations.

B. Simulation results and analysis

Four dynamic parameters SINAD, THD, SFDR and SNR are predicted in the simulation. A pulse wave of 7-bit nonlinear edges and a noise with a standard deviation σ = 0.8 LSB has been applied. Their simulation results are shown in Figures 5, 6, 7 and 8 respectively. As shown in the figures, all the predicted values are calculated by the mapping function with 30 variables. The x-axis denotes the actual values of the dynamic parameters while the y-axis denotes either the actual or estimated values. The straight lines plot the actual values of the specifications and the stars

plot the corresponding estimated values. From the figures, one can observe that the predicted values are quite close to the actual values.
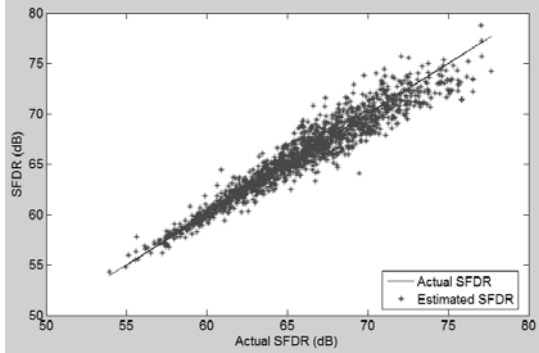

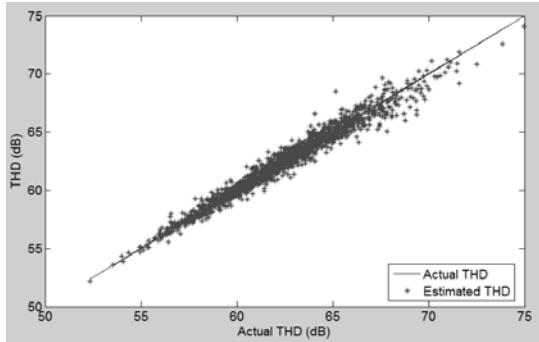Figure 5: SFDR simulation results with the mapping function of 30 variables

Figure 6: THD simulation results with the mapping function of 30 variables
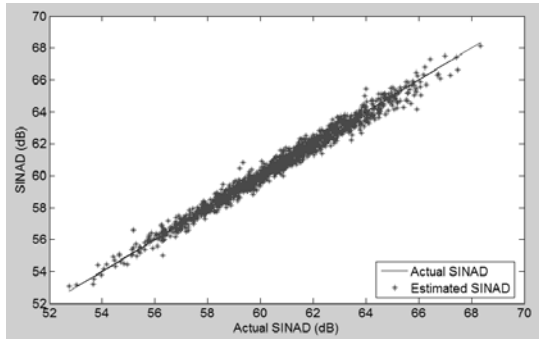

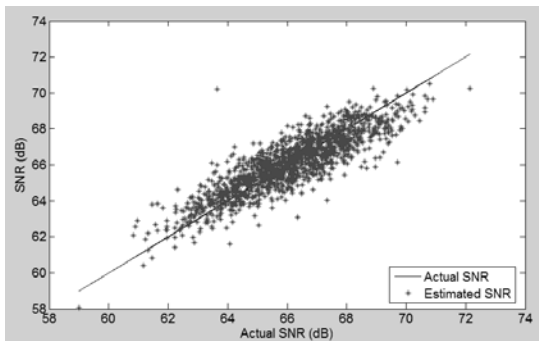Figure 7: SINAD simulation results with the mapping function of 30 variables

Figure 8: SNR simulation results with the mapping function of 30 variables

In order evaluate the results in a better way, the error is defined as the deviation between the actual values and the estimated values. In the production test of mixed-signal circuits, the correlation defines the ability of obtaining the same results when testing the same device with different hardware or software. However, in reality it is very hard to obtain completely identical results. In general, it is sufficiently accurate to make sure the deviation of the results is less than one-tenth of the full range between the minimum test limit and maximum test limit [1]. According to this requirement, if the error is smaller than one-tenth of the full range of the specification, the estimated result is acceptable. Otherwise, we define the case, of which the error is larger than one-tenth of the full range, as an outlier.

In Table 1, the mean error, the maximum error and the number of outlier cases are presented. They are all obtained by a pulse wave stimulus with 7-bit nonlinear edges and a noise of $\sigma = 0.8$ LSB. From Table 1, one can observe that when there are 30 variables in the mapping function, the estimated results are most accurate. In the signature testing, one tried to divide the training sets by a different number of ranges. By increasing the number of ranges, the more *ORP*s are calculated for each device. Therefore, the number of variables of the mapping function increases as well. In this way, the model built by MARS can fit to the relationship between the specifications and the signature in a better way. When the number of variables increases to over 30, it does not improve the results too much. Moreover, it increases the time of building mapping function. For these reasons, 30 variables were chosen to build the mapping function at the end.

TABLE 1: THE ERRORS AND OUTLIERS IN THE ESTIMATED RESULTS WITH DIFFERENT NUMBER OF VARIABLES IN THE MAPPING FUNCTION

Input pulse wave of 7-bit nonlinear edges and a noise with σ = 0.8				
		2 variables	15 variables	30 variables
SFDR	Mean error (dB)	1.70	0.78	0.68
	Max error (dB)	3.97	5.60	5.30
	Number of outlier	131	6	11
THD	Mean error (dB)	1.12	0.43	0.38
	Max error (dB)	1.88	1.29	3.33
	Number of outlier	192	4	1
SINAD	Mean error (dB)	0.68	0.31	0.23
	Max error (dB)	2.13	1.96	1.80
	Number of outlier	73	9	2
SNR	Mean error (dB)	1.22	0.78	0.66
	Max error (dB)	7.84	6.75	6.58
	Number of outlier	629	270	120

As shown in Table 1, the mean errors obtained by 30 variables are 0.68, 0.38, 0.23 and 0.66 dB for the SFDR, THD, SINAD and SNR respectively. The ratios between their mean errors to the full range of the specifications are 2.4%, 1.6%, 1.4% and 4.6%. In another words, the results are completely within the requirement that the error should be smaller than one-tenth of the full range of the specifications. The maximum errors can not satisfy the requirement, which are 19%, 14%, 10% and 40% of the full specification ranges. All these outliers can cause yield loss in production testing. For the SNR, the number of outliers is considerable as 120 out of 1500 DUTs. However, the number of outliers of the SFDR, THD and SINAD is relatively very small to 1500 DUTs as shown in Table 1. The ratio between their outliers to the total number of the DUTs is not larger than 0.8%, which is small compared with nominal values of yield loss.

TABLE 2: The Errors and Outliers in the Estimated Results with Different Standard Deviation of the Noise of the Input Signal

Input pulse wave of 7-bit nonlinear edges, 30 variables in the mapping function				
		σ= 0.2 LSB	σ= 1.6 LSB	σ= 3 LSB
SFDR	Mean error (dB)	0.67	0.69	1
	Number of outlier	10	4	45
THD	Mean error (dB)	0.38	0.49	0.77
	Number of outlier	5	4	18
SINAD	Mean error (dB)	0.24	0.35	0.66
	Number of outlier	3	0	25
SNR	Mean error (dB)	0.72	0.88	1.07
	Number of outlier	315	352	522

In Table 2, the estimated results with different standard deviation σ of the noise of the input signal are presented. From the table, one can observe that the mean errors become larger as the standard deviation of the noise increases. However, they are all within 10% of the full range of the specifications. The number of the outliers from the SFDR, THD and SINAD are still relatively small when increasing the noise. For the SNR, the number of outliers is too large to be accepted, although the mean error can satisfy the requirement. Among all the dynamic parameters, the SNR always has the worst prediction. The noise is a very random error source. In our signature testing, a set of devices are used as the references to calculate the *ORP*, which has the random noise error as well as the DUTs. As a result, the *ORP* can reflect the noise error in a certain degree but not sufficiently accurate. The SINAD, which includes the noise information as the SNR as well, can have an accurate estimated result. It is because that the values of the harmonics are relatively dominant to the noise in the

calculation of the SINAD. In our case, the mean value of the harmonics is 5dB larger than the noise.

In order to evaluate the time required for the data-processing, both the FFT analysis and the proposed signature test algorithm have been carried out in the Matlab programs on the same computer. Their computation time is 0.076s and 0.01s respectively. The data-processing of the signature testing consumes much less time.

VI. Conclusions

In this work, a machine-learning-based testing of the ADCs is proposed, which predicts the dynamic specifications from the signature *ORP*. In order to build the mapping function for prediction, both the specification testing and the signature testing are carried out on a training set. Nevertheless, only the signature-based testing is required for the DUTs, of which the data-processing consumes less computation time than the conventional FFT analysis. In the signature testing, a noisy and nonlinear pulse wave is applied as the test stimulus. It is much easier and more inexpensive to generate than a high-quality analogue sine wave used in conventional specification testing, especially when the ADCs are integrated into a platform-based design. Therefore, it is suitable to be implemented in a multi-site environment, which can reduce the test time efficiently. In order to validate our method, a 12-bit pipelined ADC modeled in Labview has been selected as the test vehicle. Finally, the results show that a pulse wave input stimulus with 7-bit nonlinear edges and an additive noise of a 3 LSB standard deviation can obtain accurate estimations of the SFDR, THD and SINAD. Although there are still some outliers in the results, their number is not larger than 3% of the total number of DUTs.

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