A Novel BIST Engine for CMOS Image Sensors

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Abstract—*This paper presents a novel test solution directly embedded inside CMOS Image Sensors (CIS) to sort out PASS and FAIL dies during production test. The solution aims at reducing test time, which can represent up to 30% of the final product cost. By simplifying the way optical tests are usually applied with an ATE, the proposed fast and low cost Built-In Self-Test (BIST) solution overcomes the drawbacks of long test time and huge amount of test data storage. Roughly half of the tests usually performed with an ATE can be embedded and applied using the BIST. Results have shown that our solution reduces test time by about 30% without impacting the defect coverage and adding only 0.25% of the total sensor area. The proposed solution outperforms existing solutions in terms of area overhead and test time saving, thus encouraging its future implementation in an industrial production flow.*

1. Introduction

CMOS **I**mage **S**ensors (CISs) are widely used in many electronic devices for various industrial applications, such as smartphones, autonomous vehicles, night vision systems, medical imaging equipments, etc. Although the **C**harge **C**oupled **D**evice (CDD) technology was initially dominant due to superior sensitivity and picture quality, various improvements in CISs have led them to surpass CCD sensors in shipment volume since about 15 years [1].

Industrial practices for CIS testing aim at verifying and ensuring that a CIS will be able to operate correctly during in-field application. They are mainly based on using external test approaches based on the use of an ATE (Automatic Test Equipment). Unfortunately, these practices have a significant impact on the final cost of the product since the test cost for a complex IC (Integrated Circuit) like a CIS may represent up to 30% of the final product cost, which is now considered as prohibitive [2].

The strategy to reduce the significant CIS test time consists of using the proposed BIST (Built-In Self Test) solution to screen out local defects (defective pixels) and to use ATE-based tests to target global defects. The BIST solution reuses the way pixels are scanned in conventional image processing algorithms (convolution and median filtering) applied with an ATE.

Validation of the solution has been done through software emulation experiments performed on output images coming from 2,400 CIS, showing that test time can be reduced by roughly **30%** without impacting the defect coverage when compared to a full ATE-based test solution. Moreover, the silicon area estimated to implement the BIST engine is about 0.25% of the total area of a CIS.

The paper presents the novel BIST solution and is organized as follows. The next section presents the background of the study, the third one deals with our BIST solution, and the fourth section is dedicated to the results.

2. Background of the Study

2.1. CIS Overview

Thanks to his optical and electrical blocks, a CIS is able to transform the light information into electrical information through the following conversion flow. The light arrives directly on a micro lens located on top of each pixel, arranged in an array, so as to do not miss any light rays and to focus them on the photosensitive element inside the pixel. This element converts photons in electrons owing to the photoelectric effect. To deal with the color aspect, a color filter organized in a Bayer pattern (Red, Green and Blue) is located on the pixel array. Analog pixel value from the photoelement is converted into a digital value thanks to Analog to Digital Converter (ADC) before to be treated (calibration, correction, …etc) inside the Image Signal Processor (ISP).

The output image of a CIS is obtained from the "row by row" reading of the pixel array. Each arithmetical pixel value in the image is an interpretation of the light level seen by a human eye, i.e. the higher the pixel value, the lighter is the pixel in the output image.

2.2. CIS Testing

The test of a CIS is divided in two main parts: electrical and optical tests. This paper interest is in optical tests which are performed on output images from the CIS under test. Optical algorithms are based on image processing techniques like convolution or median filtering methods which are done in two-dimensions and launched on an ATE. To do so, the CIS is put in two conditions: dark and light conditions with several parameters' variation. These conditions are defined in order to catch and classify defects, that can be one or several defective pixels. The defect categories represent physical defects that can occur inside the pixel array.

Two partial-test solutions have been proposed in the literature to save optical test time. Authors in [3] discuss the generation of a voltage stimuli (pulse) on the anode of the photodiode to simulate the light illumination. The work presented in [4] deals with the detection of defective lines (readout or addressing lines) thanks to the impedance extraction.

3. New Built-In Self-Test Solution

The proposed BIST solution has been implemented in Verilog language. The general BIST architecture is depicted in Fig.1 where each digital block are represented.

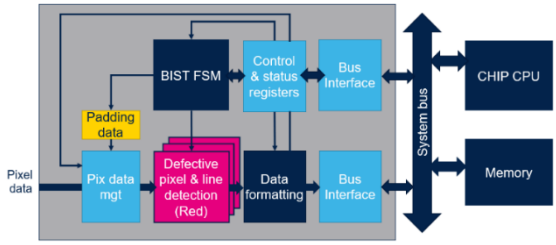

Figure 1. General BIST architecture

To test the pixel array, the BIST engine needs to access each arithmetic pixel value inside the array. The array is streamed row by row at the pixel rate thanks to a sequencer block already existing in the CIS.

In order to test all pixels in a CIS array, the block *Pixel data mgt* guides pixel of the same type (Red, Green, Blue) in dedicated accumulators located inside the *Defective pixel & line detection* block to **pipeline** the detection on several pixel types.

Then, the arithmetic value of the pixel is compared with two thresholds computed from a local average. The local average is computed in **one-dimension** because the area dedicated to the hardware BIST need to be limited as much as possible. By **transforming** two-dimensional computations into one-dimensional computations realized inside the sensor, test complexity and test data storage requirements are limited, and test time is saved.

If the pixel value is outside the defined range, the pixel is defective and its data (type, value and coordinates) are encoded by the *Data formatting* block before to be stored in the memory for the next phase. Otherwise, these data are not saved.

Once all the pixels of the array have been evaluated by the BIST, the data of each defective pixels stored inside a memory is read by a software program on the external CPU which is able to count and classify defects in the pixel array of the CIS under test.

4. Results

A dataset composed of output images (dark and light images) coming from 2,400 CIS originating from the same packet were used in the experiments. This packet is divided into PASS and FAIL sensors identified by former ATE-based tests. The BIST solution has a **99.95%** correlation with this classification with only one CIS misclassified by the BIST.

Regarding the coverage of optical algorithms usually performed on ATE, a deep analysis allows to estimate that more than **50%** of these algorithms can be embedded inside the CIS under test, thus leading to a reduction of approximately **30%** of the test time for each sensor.

Unlike the works existing in the literature, the proposed BIST solution is able to detect all potential local defects in the pixel array and not only a part of them. Moreover, the area taken by the BIST architecture has been estimated in terms of additionnal logic gates. It represents roughly only **0.25 %** of the sensor total area.

5. Conclusion

In this paper, we have presented a novel BIST solution for CIS testing. It is based on the detection of defects in dark or light output images from a CIS under test. These detection information are used to define whether images are good or bad and, finally, if the CIS is PASS or FAIL. A software emulation of the BIST engine has been done to validate our solution. Experiments carried out on images coming from 2,400 CIS have shown that our proposed solution adequately classify CIS into PASS and FAIL categories in 99.95% of cases. In addition to be useful for testing CIS, this type of embedded test solution is also valuable for diagnosis purpose, since the coordinates of defective pixels stored inside the memory are easily reachable.

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