A Novel Test Flow for Approximate Digital Circuits

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A. General context and introduction

Despite significant energy efficiency improvements in the semiconductor industry, computer systems keep consuming more and more energy [1]. Many widely used applications – such as Recognition, Mining and Synthesis (RMS) applications – are increasingly deployed in mobile devices and on Internet of Things (IoT) nodes. Therefore, it is necessary to improve the next-generation silicon devices and architectures on which these applications will run. The *inherent resiliency property* of RMS applications has been thoroughly investigated over the last few years [1]–[3]. This interesting property leads applications to be tolerant to errors – as long as their results remain close enough to the expected ones.

Approximate Computing (AxC) [1], [2] is an emerging computing paradigm, which takes advantage of the inherent resiliency property. AxC is based on the intuitive observation that selectively relaxing non-critical specifications of computing systems may lead to improve them in terms of power consumption, run time, and/or chip area. AxC has been applied to the whole digital system stack, from hardware to applications [1], [2].

This thesis focuses on Approximate Integrated Circuits (AxICs). AxICs stem from the application of AxC at hardware level. A widely used method to design those circuits is functional approximation of conventional integrated circuits [4]. This thesis focuses specifically on the testing aspects of functionally approximate circuits. Indeed, since approximation changes the functional behavior of circuits, techniques to test them must be revisited. As a matter of fact, extending the basic testing concepts to AxICs is not straightforward. In particular, during the test of a conventional circuit, any change in its functional output signals with respect to the expected values leads to labeling the circuit as faulty, and discarding it. When moving to approximate circuits, the presence of a fault may lead the circuit to behave differently than expected, yet still in an acceptable manner. In this case the circuit should not be discarded. Mastering these mechanisms may lead to increase the production process yield.

To deal with such aspects, this thesis presents a whole new test flow, named *Approximation-Aware (AxA) test flow*, composed of three main steps: (i) AxA fault classification, (ii) AxA test pattern generation and (iii) AxA test set application. The *fault classification* divides faults producing catastrophic effects on the circuit behavior from those producing acceptable effects. The *test pattern generation* produces test stimuli able to cover all the catastrophic faults and, at the same time, to leave acceptable faults undetected, as much as possible. Finally, the *test set application* labels AxICs under test as catastrophically faulty, acceptably faulty, or fault-free. Only AxICs falling into the first group will be discarded, thus minimizing overtesting (i.e., minimizing AxICs discarded due to acceptable faults).

B. AxA fault classification

The first step of the AxA testing is the *fault classification*. It aims at separating acceptable faults from catastrophic ones. Moreover, fault classification establishes the *expected yield increase* of the AxA testing w.r.t. conventional test. Measuring the output deviations of AxICs is a crucial task for a successful classification. Different error metrics have been proposed in the literature to measure AxIC output deviations [5]. This thesis shows that the classification task complexity drastically changes depending on the considered error metric. We show that some metrics – referred to as *Single Condition Test (SCT) metrics* – entail a smaller effort for the fault classification compared to metrics based on the calculation of a mean – referred to as *Mean Error (ME) metrics*.

This thesis presents two fault classification techniques [6], [7] to address respectively SCT and ME metrics. Both techniques are based on the idea of masking acceptable fault effects by using a filter. Specifically, both the netlists of the AxIC under test and of the original precise circuit are embedded in a *classifying architecture*, along with the filter. For a given fault, the so-obtained architecture produces an anomaly only if the fault leads to catastrophic output deviations. In this way, by using conventional test approaches, it is finally possible to distinguish catastrophic faults from acceptable ones. The classifying architecture is never manufactured. It is only used in simulation to classify faults. Furthermore, the technique proposed in [6] entailed drastically reduced times compared to other state-of-the-art techniques [8], [9].

C. AxA test pattern generation

The second step of the AxA testing is the *test pattern generation*. In the context of AxICs, test patterns must cover all catastrophic faults and as few as possible acceptable ones. Respecting both these conditions is crucial to discard AxICs affected by catastrophic defects and, at the same time, to avoid discarding those affected by acceptable defects. Since state-of-the-art techniques [8], [9] do not focus on minimizing detected acceptable faults, this thesis presents **the first** technique to suitably address the AxA test pattern generation [10].

This novel technique relies on a new engine capable of finding, among a set of input vectors, the smallest subset covering all the catastrophic faults and minimizing the acceptable fault coverage. Specifically, the engine generates an input vector set $\mathcal{S}$ and measures its catastrophic fault coverage as well as its acceptable fault coverage. Hence, it finds within $\mathcal{S}$ the optimal subset $\mathcal{V}$ which attains the required goals. To accomplish this task, the engine formulates and resolves an *Integer Linear Programming*

(ILP) optimization problem, whose solution is the final *ax-aware test set*.

Experimental outcomes achieved with the proposed technique showed an improvement spanning from 16% to 49% compared to state-of-the-art techniques. Although the achieved results are quite good, the ideal outcomes (i.e., 100% covered catastrophic faults and 0% covered acceptable faults) are still quite far from being attained. Therefore, further efforts are needed to effectively test AxICs.

D. AxA test set application

To push further the test outcomes, the third step of AxA testing, the *test pattern generation*, comes into play. In this regard, this thesis presents **the first** AxA test set application technique [11]. Since often it is not possible to avoid detecting acceptable faults, the basic idea is to verify, after the test application, whether the detected fault was acceptable or not. The proposed technique is based on the well-know signature analysis concept, successfully applied to built-in self-test (BIST) architectures in the seventies [12] and still used in modern BIST architectures. BIST approach compacts test responses together into a signature, which is used to verify whether the Unit Under Test (UUT) is faulty or not. In detail, when the test mode is activated, test patterns are applied to UUT and a signature is generated. Then, the latter is compared with the golden signature, which was generated by the fault-free circuit and stored within the BIST architecture. If the two signatures are identical, the circuit is considered fault-free. Otherwise, a malfunction is detected. Basically, the proposed technique is divided into two steps:

At design time, we perform a fault simulation by using test patterns and the AxIC's faults. For each acceptable fault, we compact simulation responses into a signature, thus ending up having multiple *acceptable-fault signatures*.

At test time, AxIC test responses are compacted into a signature and compared with all the acceptable-fault signatures. If there is at least one match, then the AxIC is considered acceptable. Otherwise, the circuit is rejected.

The proposed technique is intended to be used for external test, i.e., test are applied by using an Automatic Test Equipment (ATE). Of course, it can be also adapted to a BIST context.

Results obtained with the proposed technique were really good. Indeed, they showed yield gain results very close to the expected ones (i.e., 99.84% of the expectations, on average). In terms of covered faults, the technique delivered 100% covered catastrophic faults and 0.16% covered acceptable faults on average, that are quite close to the ideal ones (i.e., 100% covered catastrophic faults and 0% covered acceptable faults).

E. Conclusion and perspectives

In the last two decades, approximate computing has been employed to realize a new class of integrated circuits, i.e. approximate integrated circuits or AxICs. The introduction of this new class of circuits entailed new challenges and opportunities to test them. Indeed, in AxIC context, the concept of faulty circuit changes. Faults can be either acceptable (i.e., causing acceptable output deviations) or catastrophic (i.e., causing catastrophic output deviations). Catastrophic deviations lead the AxIC to be discarded. However, if the deviations stay in the acceptable region, then the AxIC must not be discarded. Therefore, in this context, test procedures have to be able to distinguish catastrophically faulty AxICs from acceptably faulty ones. Ultimately, this leads to increase the production yield.

The contribution of this thesis is to introduce a whole new test flow, the Approximation-Aware (AxA) test flow, able to fully fulfill the purpose. Specifically, this thesis provided the following progresses in the research field and produced related scientific publications: (i) separating catastrophic faults from the acceptable ones in a drastically faster way compared to the state of the art [6], [7]; (ii) presenting the first approach to produce test sets detecting all the catastrophic faults and as few acceptable ones as possible [10]; (iii) presenting the first approach to distinguish catastrophically faulty AxIC from acceptably faults ones, by observing test responses [11]. Experimental results showed that the synergy of all the proposed techniques led us to achieve relevant outcomes, i.e., 100% catastrophically faulty AxICs were discarded and almost all (99.84%) acceptably faulty AxICs were accepted, thus increasing the production yield.

The techniques presented in this thesis can be adapted to any kind of domain needing the selective test of fault subsets in integrated circuits. For instance, according to the ISO26262 automotive standard terminology, faults that cannot produce any failures in the operational conditions of embedded processor cores are called *"safe faults application dependent"*. Using the techniques proposed in this thesis would help suitably treating these faults in order to reduce over-testing effects, which, in turns, increases the yield and thus the profit of semiconductor companies.

REFERENCES

[1] Q. Xu *et al.*, "Approximate computing: A survey," *IEEE Design Test*, vol. 33, no. 1, pp. 8–22, Feb 2016.

[2] S. Mittal, "A survey of techniques for approximate computing," *ACM Comput. Surv.*, vol. 48, no. 4, pp. 62:1–62:33, Mar. 2016.

[3] V. K. Chippa *et al.*, "Analysis and characterization of inherent application resilience for approximate computing," in *2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC)*, May 2013, pp. 1–9.

[4] S. Rehman *et al.*, *Heterogeneous Approximate Multipliers: Architectures and Design Methodologies*. Springer International Publishing, 2019, pp. 45–66.

[5] J. Liang *et al.*, "New metrics for the reliability of approximate and probabilistic adders," *IEEE Transactions on Computers*, vol. 62, no. 9, pp. 1760–1771, Sept 2013.

[6] M. Traiola *et al.*, "Testing approximate digital circuits: Challenges and opportunities," in *2018 IEEE 19th Latin-American Test Symposium (LATS)*, March 2018, pp. 1–6.

[7] ——, "Investigation of mean-error metrics for testing approximate integrated circuits," in *2018 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Oct 2018, pp. 1–6.

[8] A. Chandrasekharan *et al.*, "Approximation-aware testing for approximate circuits," in *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan 2018, pp. 239–244.

[9] A. Gebregiorgis *et al.*, "Test pattern generation for approximate circuits based on boolean satisfiability," in *2019 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2019, pp. 1028–1033.

[10] M. Traiola *et al.*, "A test pattern generation technique for approximate circuits based on an ilp-formulated pattern selection procedure," *IEEE Transactions on Nanotechnology*, pp. 1–1, 2019.

[11] ——, "Maximizing yield for approximate integrated circuits," in *2020 Design, Automation Test in Europe Conference Exhibition (DATE) (to appear)*, 2020.

[12] R. A. Frohwerk, "Signature analysis: a new digital field service method," 1977.