Preliminary Defect Analysis of 8T SRAM Cells Used for In-Memory Computing

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***Abstract*—In-Memory-Computing (IMC) paradigm has been proposed as an alternative to overcome the memory wall faced by conventional von Neumann computing architectures. IMC architectures proposed today are built either from volatile or non-volatile basic memory cells, but a common feature is that all of them are prone to manufacturing defects in the same way as conventional memories. In this paper, we propose to analyze the behavior of an IMC 8T SRAM cell in presence of defects located in the read port of the cell. A model of a basic IMC memory array has been set up to simulate the behavior of the cell in the two modes of operation: memory mode and computing mode. Resistive short defects were injected into the read port and then analyzed. Preliminary results show that these defects can severely impact the behavior of the 8T SRAM in memory mode as well as computing mode. The final goal of this study is to develop effective test algorithms for these defects.**

Keywords—8T SRAM cell, In-Memory Computing, test, resistive defect.

I. INTRODUCTION

Most modern computer systems are based on the von Neumann architecture, which is characterized by memory storage decoupled from the processing cores. However, the efficiency of data-intensive applications such as artificial intelligence, cryptography, search engines, etc. is now severely impacted by the von Neumann bottleneck [1]. This problem is caused by frequent and large data transfers between memory units and processing cores, resulting in high energy consumption and overall throughput limitation. To overcome these performance and power penalties, many efforts have been done to develop new architectural paradigms.

One of the most promising alternatives is to use In-Memory Computing (IMC) architectures [2][3]. Beyond their classical storage function, these memory architectures aim at integrating extra logic in the memory array and in the periphery to circumvent the von Neumann bottleneck problem. By this way, computations and operations can be performed directly inside the memory.

Electrical defect characterization is a preliminary step to identify testability conditions of a defective cell. In [4], the authors analyzed the faulty behavior of an 8T SRAM cell caused by open defects (full and resistive) affecting the terminal nodes of the read port transistors. However, this was done under the assumption that the cell works correctly with respect to the write operation and that only the read operation can cause an erroneous read.

In this paper, we propose an analysis of the IMC 8T SRAM cell w.r.t all resistive short-circuit defects that may occur into the read port of the cell. Defects on the remaining part (six transistors) behave in the same manner as defects in the conventional 6T SRAM cell, and hence have been widely investigated in the literature [5]. From the results of this analysis, our goal is to develop new test algorithms to detect defects specific to IMC memories. These algorithms will be used in conjunction with conventional SRAM test algorithms to achieve complete fault coverage in 8T SRAM IMC architectures.

II. SRAM-BASED IN-MEMORY COMPUTING

IMC architectures allow computations to be performed directly in the memory instead of offloading the data to an external computing node. They can operate in two modes: memory mode and computing mode. In memory mode, the memory performs a read or write operation on an addressed word. In computing mode, the memory executes a calculation from at least two addressed words.

To characterize the electrical behavior of the 8T SRAM cell in both modes of operation, the model shown in Fig. 1, which consists of two 8T SRAM cells, was considered.

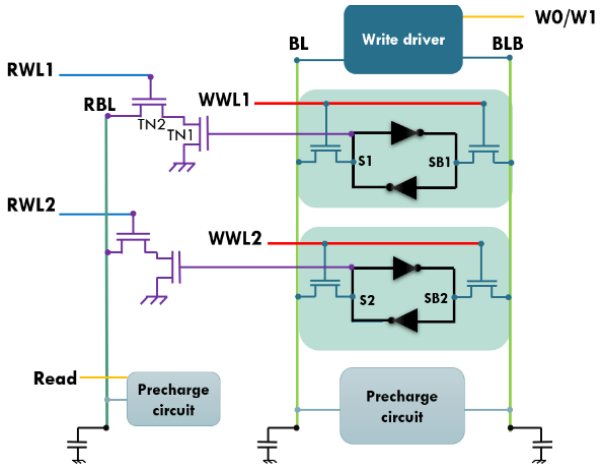

Fig. 1. Considered IMC model

In memory mode, the writing operation in an 8T SRAM cell is similar to that of the 6T. The data is loaded on the Bit Line (BL) and its inverse on the Bit Line Bar (BLB). Then, the concerned Write Word Line (WWL1 or WWL2) is activated. To read the content of cell, the Read Bit Line (RBL), initially precharged at Vdd, remains floating at '1'. Then, the concerned Read Word Line (RWL1 or RWL2) is activated. Let us consider that the first cell stores a '0'. In this case, the NMOS transistor TN1 of the read port whose gate is connected to the memory node S1 will be in the off state. The RBL will therefore be maintained at Vdd, so a '0' will be read on the read output port (considering the presence of an inverter at the "Read" output of RBL). In case the cell stores a '1' (S1 = '1'), on the other hand, the RBL will be discharged through TN1 and TN2, so that a '1' will be read on the read output port after inversion.

In computing mode, the read operation is performed on the two 8T SRAM cells by simultaneously activating their RWLs. The output of the read port (RBL) subsequently shows a NOR behavior of the selected 8T SRAM cells.

III. Defect Analysis of 8T SRAM-Based IMC

Figure 2 shows the resistive defects we have injected into the read port of the 8T SRAM cell. Six defects (three open and three short defects) were considered for each transistor. Defects on the remaining six transistors behave in the same manner as defects in the conventional 6T cell and hence have not been considered.

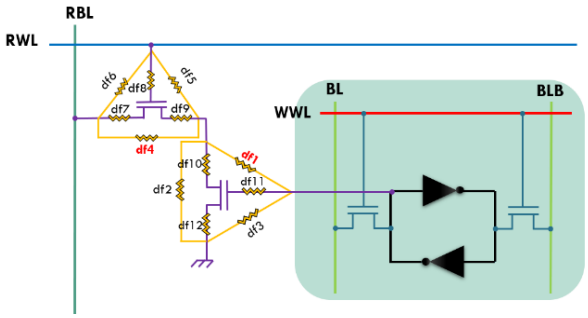

Fig. 2. Resistive open and short defects injected in the read port of an 8T SRAM cell

A. *Analysis of resistive short defect df1*

To analyze the behavior of a defective 8T SRAM cell in presence of df1, let us consider the case where the cell is initially loaded by a '0' (S=0). By activating the RWL, node S will cause the RBL voltage to drop due to defect df1, thus leading to an incorrect R0 operation on the cell.

In the following figures, read operations RX and write operation WX are in green when correctly executed and red when affected by the defect under study.

The behavior of the cell in presence of df1 with a defect resistance of 1Ω (i.e., a pure short defect) is illustrated in Fig. 3. The R0 operation is indeed incorrect since, at t=5ns after the RWL activation, RBL is completely discharged. At t=10ns, the W1 operation is not executed since the voltage at node S has remained at a value lower than Vdd/2.

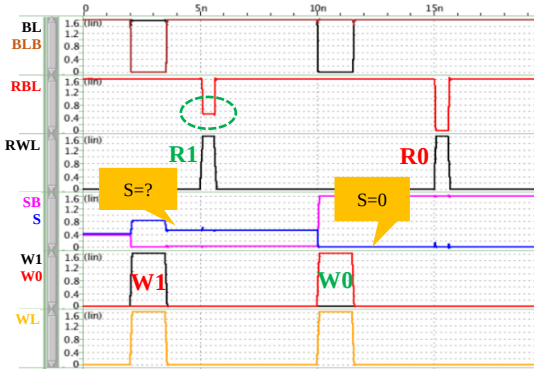

Fig. 3. Simulation of the behavior of a faulty SRAM 8T cell in presence of df1=1Ω

Figure 4 shows the execution of operations (W1, R1) through the behavior of the storage node S and the voltage of the RBL when the resistance of df1 varies. According to the behavior of the storage node S and for any resistance value lower than 150KΩ, the W1 operation is not performed. Although, the R1 operation is always correct since for any value of the resistance of df1, the voltage at the RBL remains lower than Vdd/2.

To summarize, df1 affects the 8T SRAM cell in both memory and computing modes. In memory mode, R0 and W1 operations are corrupted. In computing mode, the NOR(0, 0) function is incorrect too. These faulty behaviors are observed for a defect size lower than 150kΩ.

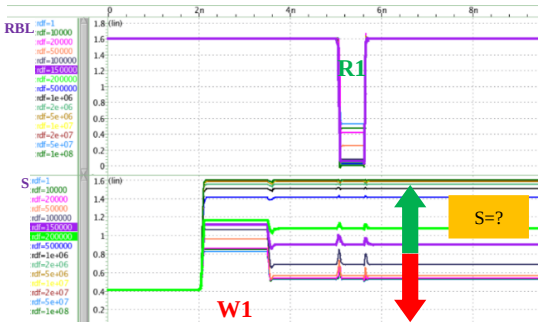

Fig. 4. W1 and R1 operation behaviors depending on the resistance value of defect df1

Figure 5 depicts the faulty behavior of the RBL during execution of the R0 operation when the resistance of df1 varies. As can be seen, for any resistance value of defect df1 lower than 5 MΩ, the R0 operation is incorrect.

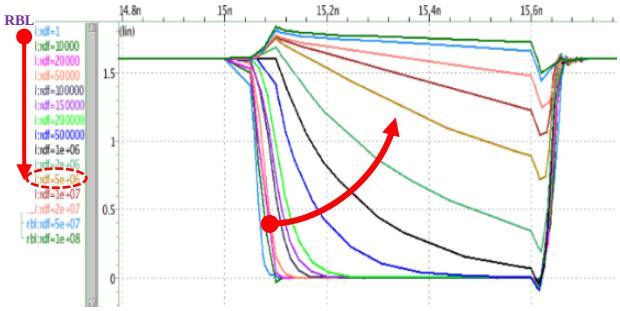

Fig. 5. Execution of the R0 operation depending on the resistance value of defect df1

B. *Comprehensive results of resistive defect injections*

From the analysis of short resestive defects injected in the read port of the 8T SRAM cell, Table I summarizes the various faulty behaviors by specifying the resistance range for which defects are detectable.

TABLE I. Summary of the faulty behavior caused by resistive short defects with the resistance range for which they are detectable

Resistive short defects	Memory mode	Computing mode	Detectable resistance
df1	R0 incorrect W1 incorrect	NOR (0,0) incorrect	R<150kΩ
df2	R0 incorrect	NOR (0,0) incorrect	R≤5MΩ
df3	W1 incorrect R1 incorrect	NOR (1,0) incorrect	R<150kΩ
df4	Correct behavior	Correct behavior	--
df5	R1 incorrect	NOR (1,0) incorrect	R<15kΩ
df6	R0 incorrect R1 incorrect	Incorrect behavior	R<20kΩ

Different orders of critical resistance were found, about hundreds of kΩ for df1 and df3, twenties of kΩ for df5 and df6, and in the order of MΩ for df2. These defects can be correctly tested by classical March test algorithms except df4 which is a particular defect affecting all cells of the same RBL.

IV. Conclusion

In this paper, we first discussed the IMC memories based on 8T SRAMs and we presented the model considered to simulate and analyze their behavior in presence of defects injected in the read port of the cell. Existing test algorithms do not detect all resistive defects in an 8T SRAM cell, especially those located in the read port. The next step in our work will be to establish the testability conditions of an 8T SRAM IMC and develop test algorithms to be used in both modes of operation.

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