A Highly Robust and Low-Power Flip-Flop Cell With Complete Double-Node-Upset Tolerance for Aerospace Applications

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***Abstract*—This paper proposes a Highly Robust and Low Power Flip-Flop cell (HRLPFF) with complete double-node-upset (DNU) tolerance for aerospace applications. The HRLPFF cell is constructed from a master latch and a slave latch. The master latch mainly comprises two 2-input C-elements as well as one 2-input clock-controlled C-element; the slave latch is similar to the master but has an extra keeper to avoid high-impedance state of the output-level C-element. HSPICE-tool based simulation results demonstrate that the proposed HRLPFF cell can provide complete DNU-tolerance. Simulation results also demonstrate that the proposed HRLPFF cell can reduce power dissipation by roughly 65% on average when compared with typical existing radiation-hardened flip-flop cells and that the proposed HRLPFF cell is not only completely DNU-tolerant but also insensitive to high-impedance-state.**

***Index Terms*—Radiation protection, circuit hardening, flip-flop reliability, soft error tolerance, double-node-upset**

I. Introduction

With the aggressive shrinking of transistor feature sizes of *complementary metal oxide semiconductor* (*CMOS*) integrated circuits, the amount of critical charge required to change the state of a storage node is constantly decreasing, easily causing soft errors [1]. Hence, for storage circuits working under harsh radiation environments, soft errors caused by the hit of high-energy particles (such as protons, neutrons, alpha particles and heavy ions) have become one of the major reliability challenges to their operations [2]. It is well known that *single-node-upset* (*SNU*) is one of the common soft errors. When the charge generated by a radiative particle striking through silicon is collected by the source/gate diffusion of a CMOS transistor, an SNU may occur. To effectively mitigate SNUs, the *radiation-hardening-by-design* (*RHBD*) technique for designing robust circuits is an efficient approach, based on which many radiation-hardened *static random-access memories* (*SRAMs*), latches and *flip-flops* (*FFs*), such as those in [1, 3-7], have been proposed in the literature. This paper focuses on the design of a novel FF cell. Note that this paper is an extended version of paper [8 - ref. paper VTS'22]

In the RHBD approach, traditional inverters and *C-elements* (*CEs*) are widely used components for radiation-hardening of FF cells. Figure 1 shows the transistor-level schematic of two types of CEs, i.e., a 2-input CE as well as a *clock-gating* (*CG*)-based 2-input CE. The operation principle of a CG-based CE is that it works as an inverter when its inputs, including the *system clock* (*CLK*) and the *negative system clock* (*NCK*) signals, have an identical value. However, if its input values become different, its output will enter into the *high impedance state* (*HIS*) [7], thus keeping its previous output value for a period of time. Non-CG-based CEs have a similar operational principle. Note that a CE is different from an XOR gate that outputs logic 1 if its two input values are different; if its two input values are identical, it outputs logic 0.

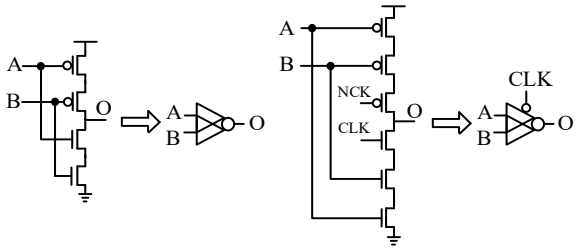

Fig. 1. Transistor-level schematic of two types of C-elements. (a) 2-input. (b) Clock-gating-based 2-input.

In deep nano-scale CMOS technologies, with the rapid advancement in circuit integration as well as the aggressive reduction of transistor feature sizes, one radiative particle has a high probability to simultaneously affect multiple adjacent nodes due to charge-sharing [7-9], resulting in *multiple-node-upset* (*MNU*). *Double-node-upset* (*DNU*) is the most concerned MNUs. Furthermore, compared with latches, FF cells generally have extra transistors and thus larger area, making them more susceptible to high energy particles

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generating DNUs. Consequently, protection against DNUs for FF cells becomes mandotory, especially for aerospace applications that have to face harsh radiation. However, to the best of our knowledge, few approaches have been proposed to efficiently address the DNU tolerance of FF cells.

In this paper, we propose a novel and reliable FF cell, namely HRLPFF, providing complete DNU tolerance with extremely low power consumption. The proposed HRLPFF cell is constructed through a master latch as well as a slave latch. The master latch consists of five *transmission gates* (*TGs*) as well as three 2-input CEs, two of them feeding the inputs of the third CE. The slave latch has the same structure as the master latch but it also has a keeper at the output stage. Using high-speed transmission paths, CG technologies as well as fewer transistors, the proposed HRLPFF cell consumes very low power as well as moderate transmission delay area, leading to an efficient power-delay-area product.

The rest of this paper is organized as follows. Section II reviews typical existing flip-flop cells. Section III presents the circuit schematic, working principles as well as verification results of the proposed HRLPFF cell. Section IV describes evaluation and comparison results among different existing flip-flop cells. Section V concludes this paper.

II. Existing Flip-Flop Cells

Figure 2 shows the schematics of typical existing FF cells to that are reviewed in this section. Figure 2-(a) shows the structure of the *traditional unhardened flip-flop* (*TUFF*). The TUFF is made up of a traditional unhardened master latch as well as an unhardened slave latch so that it cannot tolerate SNUs.

Figure 2-(b) shows the structure of the *triple modular redundancy flip-flop* (*TMR-FF*). The TMR-FF consists of three TUFFs as well as one 3-input voter that comprises three AND gates and one OR gate. If two or more TUFFs are simultaneously impacted by soft errors, the voter cannot output valid values. Hence, the TMR-FF cannot provide complete DNU-tolerance. Furthermore, the TMR-FF has high power as well as large area.

Figure 2-(c) presents the schematic of the *dual-redundancy radiation-hardening flip-flop* (*DRRH-FF*) [10]. Its master latch consists of dual parallel traditional unhardened D-latches but the slave latch mainly comprises three 2-input CEs as well as two inverters. Clearly, if the slave latch is impacted by a DNU (e.g., the outputs of the internal CEs are impacted), the error will be kept and the output-level CE cannot intercept the kept error. Hence, the FF cannot provide DNU-tolerance. Furthermore, the DRRH-FF is insensitive to the HIS since the node Q may float to an uncertain value when the inputs of the output-level CE change to different values due to a DNU.

Figure 2-(d) presents the structure of the *DNU-resilient flip-flop* (*DNUR-FF*) [11]. In this FF, many CEs and inverters feed each other to construct reliable feedback loops to robustly store values. However, the FF cannot provide DNU-tolerance because the middle input as well as the output of any 3-input CE in the FF cell may be upset by a DNU, resulting in wrong value retention. Furthermore, the DNUR-FF cell is HIS-sensitive as well.

Figure 2-(e) presents the structure of the Quatro-FF [12] that comprises many transmission transistors as well as double

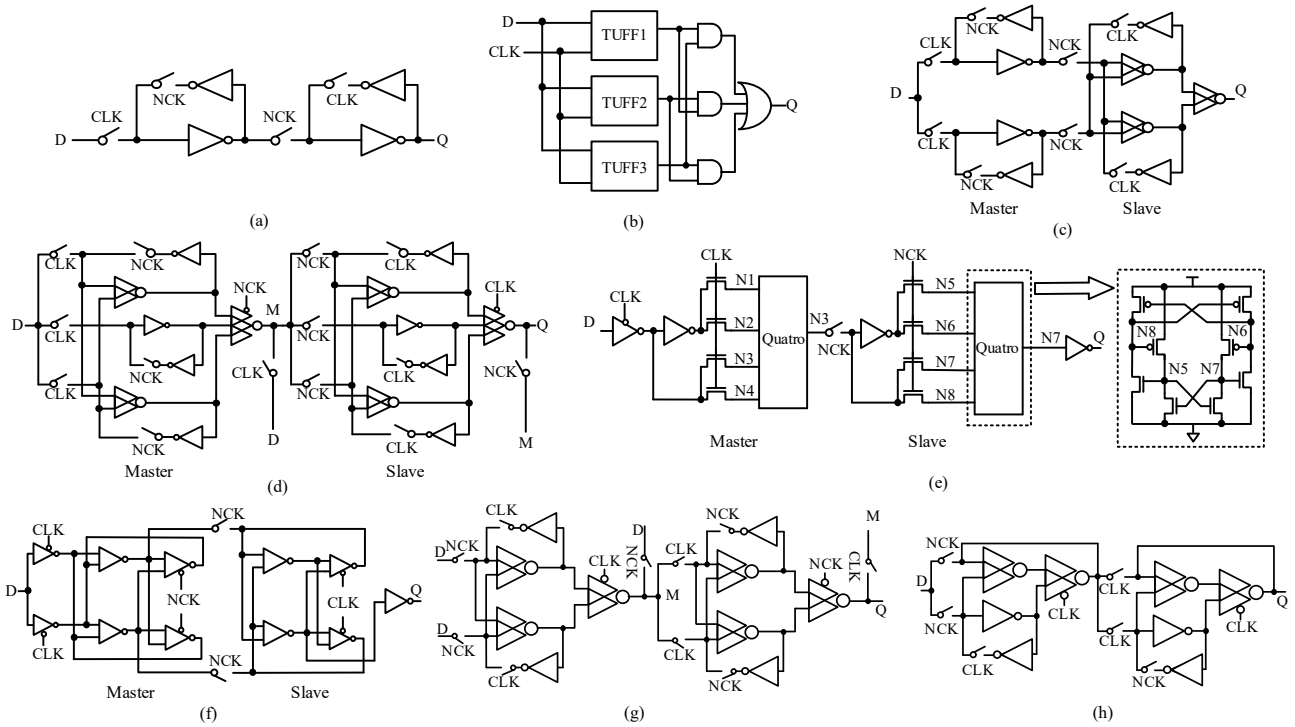

Fig. 2. Schematics of existing FF cells. (a) TUFF, (b) TMR-FF, (c) DRRH-FF [10], (d) DNUR-FF [11], (e) Quatro-FF [12], (f) DICE-FF [14], (g) HPST-FF [15], (h) SNUR-NVFF [16].

Quatro cells [13]. With extra feedback loops, the Quatro-FF cell can retain its previous correct output value even if one of its four input nodes (e.g., M5, M6, M7 and M8) is flipped. Note that, if one particle impacts two nodes in any Quatro cell through charge sharing, the FF cannot output correct values. Hence, the FF is not DNU-tolerant. Furthermore, the FF has high power as well as large delay.

Figure 2-(f) presents the structure of the *dual-interlocked-storage-cell flip-flop* (*DICE-FF*) [14] that respectively uses one DICE cell as its master/slave latch. Note that, a DICE cell can provide complete self-recovery from any SNU but it cannot provide complete DNU-tolerance. This means that, in the worst case, if one node-pair of a DICE is flipped by a DNU, the DICE-FF will output a flipped value. Hence, the FF is not completely DNU-tolerant.

Figure 2-(g) shows the structure of the *high performance SNU tolerant flip-flop* (*HPST-FF*) [15]. To effectively tolerate SNUs, the FF primarily makes use of four interlocked feedback loops connected to the two CG-based 2-input CEs. However, the FF cannot provide complete DNU-tolerance because a DNU may flip the inputs of the output-level CE of the master/slave latch.

Figure 2-(h) shows the structure of the *SNU-resilient non-volatile flip-flop* (*SNUR-NVFF*) [16]. In order to tolerate SNUs, its master/slave latch primarily makes use of two series-connected 2-input CEs and a keeper to construct reliable feedback loops. However, the SNUR-NVFF, as the HPST-FF, is not completely DNU-tolerant.

III. Proposed HRLPFF Cell

Figure 3 shows the schematic of the proposed HRLPFF cell, in which all the switches are TGs. Let us first explain the clock-connections of a TG. If it is marked with CLK, the gate-terminal of the NMOS transistor is connected to the CLK signal and the gate-terminal of the PMOS transistor is connected to the NCK signal.

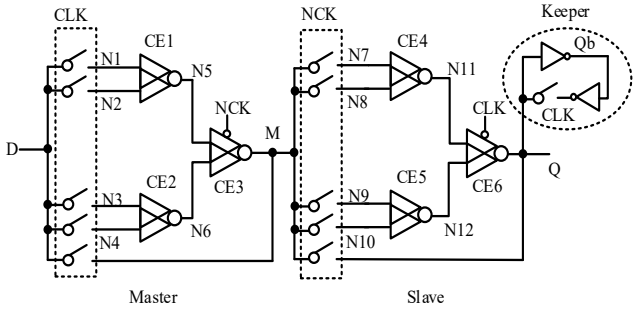

Fig. 3. Proposed HRLPFF cell.

As shown in Fig. 3, the HRLPFF consists of a master latch as well as a slave latch. The input D of the master latch is connected to the inputs (i.e., N1 to N4) of two parallel 2-input CEs (i.e., CE1 and CE2) through four switches. The outputs of the above CEs feed the inputs of CE3. The output node of CE3 (i.e., M) is also the output node of the master latch, feeding the input of the slave latch. Note that the input D is directly connected to the node M through the left-bottom switch to construct a high-speed path to reduce transmission delay. The slave latch is very similar to the master latch except that an extra keeper is employed at the output of the HRLPFF cell. Nodes M and Q are the input and output of the slave latch, respectively. Figure 4 shows the layout of the proposed HRLPFF cell.

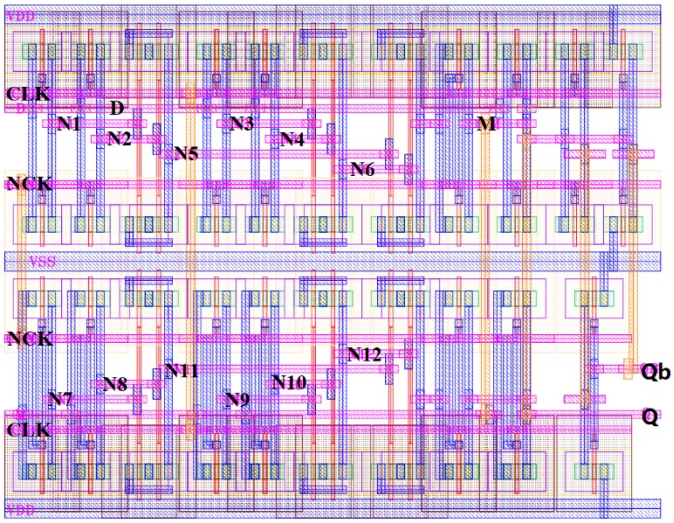

Fig. 4. Layout of the proposed HRLPFF cell.

Figure 5 presents the functional waveform obtained for the error-free HRLPFF under the voltages of 0.6V, 0.7V, 0.8V, 0.9V and 1.0V. It can be seen from Fig. 5 that the value of Q changes along with the value of D only at the falling edge of the CLK signal; in any other time period, Q just retains its previous value. The waveform demonstrates that the HRLPFF can work correctly at 500MHz (the clock period is 2ns) and can also work correctly at 500+ MHz. Note that the proposed HRLPFF cell was designed/implemented in a 22nm CMOS technology from GlobalFoundries. The PMOS transistors had a W/L ratio of 90nm/22nm and the NMOS transistors had a W/L ratio of 45nm/22nm. The standard supply voltage was set to 0.8V and the working temperature was set to room temperature. The simulations were performed with the Synopsys HSPICE tool.

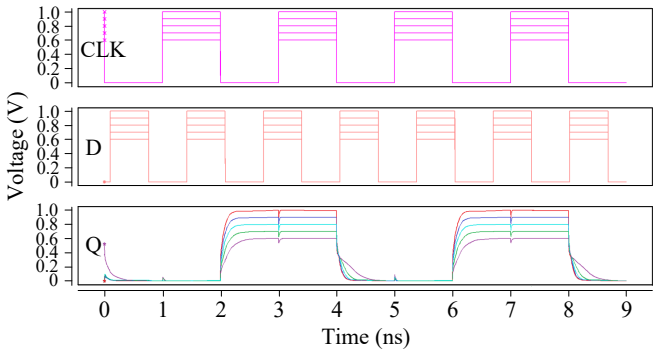

Fig. 5. Verification waveform with no error injections for the proposed HRLPFF cell under the voltages of 0.6V, 0.7V, 0.8V, 0.9V and 1.0V.

According to Fig. 5, the detailed working principle of the proposed HRLPFF is as follows.

(1) Initially (see 0 ns in Fig. 5; CLK = 1), the input D-value can be transmitted through five switches to the master latch that

works in transparent mode. In other words, the input D-value can initialize the devices in the master latch. However, because the data paths between the master latch and the slave latch are OFF through five TGs (i.e., the switches between nodes M and N7~N10), the slave latch cannot receive any value from the master latch. At this time, the node M can be determined only through the left-bottom switch instead of CE3 to reduce transmission delay.

(2) When CLK changes to low (see the time period between 0 ns to 1 ns in Fig. 5; CLK = 0), the input D-value can no longer be transmitted through TGs to the master latch that works in hold mode, but the master latch is pre-charged in the above step. At this time, node M can be outputted through CE3 instead of the left-bottom switch that is turned off. Meanwhile, the slave latch working in transparent mode can receive the M-value stored in the master latch and can output the value through Q. Note that, when the slave latch works in transparent mode, the feedback loop in the keeper cannot be formed due to clock-gating so that there is no current competition at Q.

(3) When CLK returns to high (see the time period between 1 ns to 2 ns in Fig. 5; CLK = 1), the master latch can receive a new D-value from D through switches and can output the value to M through the left-bottom switch. At this time, the slave latch enters into the hold mode, and stores and outputs the value it received in the above step. Moreover, Qb is connected to Q through an inverter as well as a switch, and hence a feedback loop can be formed in the keeper. Note that, the HRLPFF is HIS-insensitive. The reason is that, if the inputs of CE6 become different due to a soft error, Q can still have its previous correct value through the constructed feedback loop in the keeper.

(4) When CLK changes to low once again (see the time period between 2ns to 3ns in Fig. 5; CLK = 0), the master latch keeps the D-value received in the above step and the slave latch receives the value and outputs the value to Q. Therefore, the Q-value can be changed along with the D-value only at the falling edge of the CLK signal.

Now, let us discuss the fault-tolerance principle of the proposed HRLPFF cell. Considering the structural similarity between the master latch and the slave latch, we only discuss the fault-tolerance principle of the slave latch in this paper. In the case where the latch suffers from an SNU, all situations can be divided into three categories: **(a)** One input node of CE4 or CE5 suffers from an SNU. Clearly, the CE can intercept the SNU. **(b)** One input node of CE6 suffers from an SNU. Clearly, the CE can intercept the SNU as well. **(c)** Q suffers from an SNU. In this situation, the Q-value can be self-recovered through CE6 since the inputs of CE6 are both correct. Hence, the representative single nodes for SNUs of the latch are N7, N11, and Q only. Note that, Qb suffering from an SNU in hold mode is equivalent to the case where Q suffers from this SNU so that Qb can also self-recover from an SNU. Therefore, the proposed HRLPFF cell can effectively provide complete SNU-tolerance.

Figure 6 shows the verification waveforms for the SNU injections on the representative single-nodes in the proposed HRLPFF cell. Note that we used a controllable double exponential current-source model to simulate/mimic node upsets as in [3, 5, 7] and used the error-injection statements in HSPICE tool to finish the error injections. The double exponential current-source model is presented as follows.

$$I_{inj}(t) = \frac{Q_{inj}}{\tau 1 - \tau 2}\left(e^{-\frac{t}{\tau 1}} - e^{-\frac{t}{\tau 2}}\right) \quad (1)$$

In Eq. (1), Q_{inj} is the amount of charge that is injected to a node, $\tau 1$ is the time constant for junction collection, and $\tau 2$ is the time constant for the ion track's initial establishment. Since our objective is to validate the operation of the circuit under extreme node-upset conditions that disturb circuit nodes, the worst-case Q_{inj} for each node in this work was selected to be 20fC and the values for $\tau 1$ and $\tau 2$ were set to 0.1 and 3.0 ps, respectively.

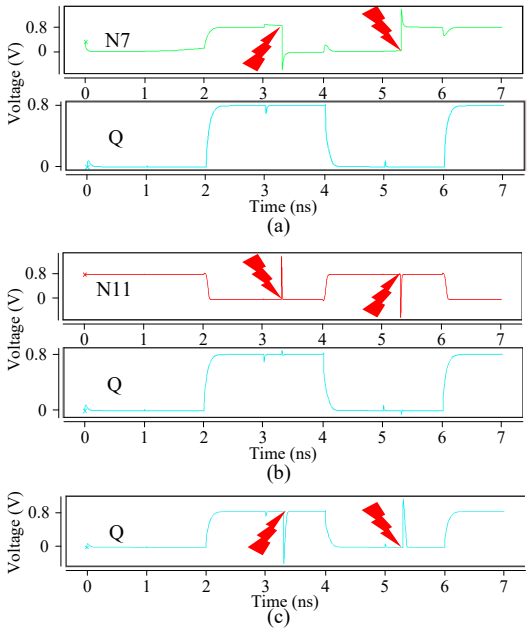

Fig. 6. Verification waveforms for the SNU injections on the representative single-nodes in the HRLPFF cell. (a) SNU on N7, (b) SNU on N11, and (c) SNU on Q.

In Fig. 6, the lightning marks denote the injected SNU errors. It can be seen that, after the injection of an SNU on N7, the waveform of Q is still correct. After the injection of an SNU on N11 or Q, the affected single nodes can self-recover. Therefore, the simulation results clearly demonstrate the effective SNU-tolerance for the proposed HRLPFF cell.

Next, let us consider the situations where the HRLPFF cell suffers from a DNU. If one of the impacted nodes belongs to the master latch while the other belongs to the slave latch, the DNU is equivalent to two simultaneous SNUs. Therefore, the HRLPFF cell can tolerate this type of DNUs. When both nodes belong to one latch (we only need to consider the slave latch), there are only two cases (Case A and Case B in the following) that need to be discussed. Note that, if node-pair <Q, Qb> is impacted by a DNU in hold mode, this equals to the case that Q or Qb is impacted by an SNU. Therefore, this node-pair can be omitted for the discussion of DNU-tolerance.

Case A: A DNU impacts a pair of nodes that do not belong to the same CE. The DNU node-pairs are <N7, Q>, <N7, N12>,

<N7, N9>, <N7, N10>, <N8, Q>, <N8, N12>, <N8, N9>, <N8, N10>, <N9, Q>, <N9, N11>, <N10, Q> as well as <N10, N11>.

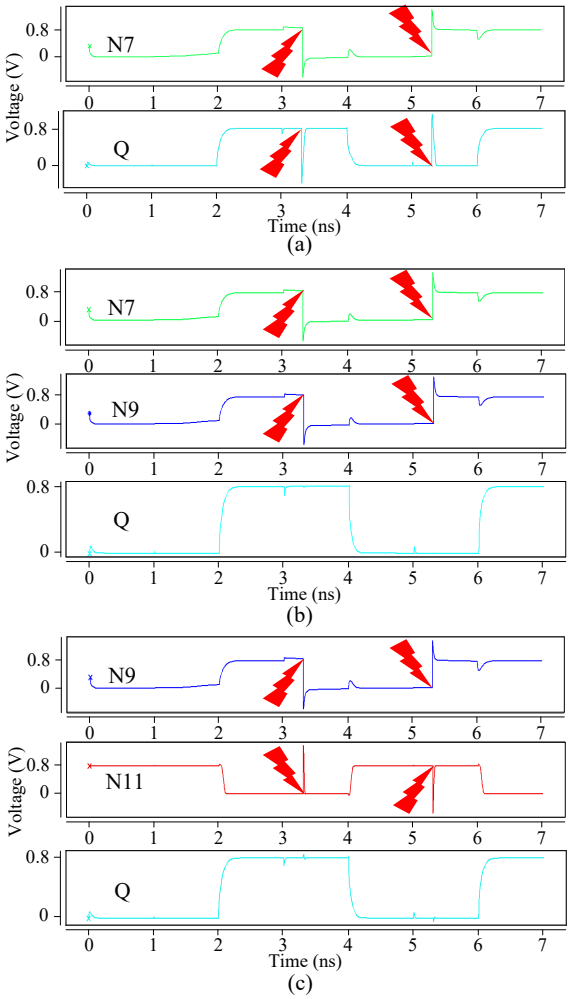

Fig. 7. Verification waveforms for the representative DNU (Case-A) injections in the HRLPFF cell. (a) DNU on <N7, Q>, (b) DNU on <N7, N9>, and (c) DNU on <N9, N11>.

Note that we can further divide Case A based on the locations of the impacted node-pairs as follows: **(A1)** When the node-pair includes Q as well as one input of CE4/CE5, the DNU node-pairs are <N7, Q>, <N8, Q>, <N9, Q> and <N10, Q>. Clearly, CE4/CE5 can intercept the error at its single inputs, and thus the values of N11 and N12 cannot be flipped. Hence, node Q can recover through CE6; **(A2)** When the node-pair includes the output of CE4/CE5 as well as one input of CE5/CE4, the DNU node-pairs are <N7, N12>, <N8, N12>, <N9, N11> and <N10, N11>. Clearly, N11 (N12) can recover since the inputs of CE4 (CE5) are correct. Therefore, Q is still correct; **(A3)** When the node-pair includes one input of CE4 and one input of CE5, the DNU node-pairs are <N7, N9>, <N7, N10>, <N8, N9> and <N8, N10>. Clearly, CE4 and CE5 can intercept the errors at their single inputs, and thus N11 and N12 cannot be flipped. Therefore, Q is still correct. In summary, the proposed HRLPFF cell can provide complete DNU tolerance in Case A. Note that, we select one node-pair from each of the sub-cases, and thus the representative DNU node-pairs in Case-A are <N7, Q>, <N7, N9> and <N9, N11> only.

Figure 7 shows the verification waveforms for the representative DNU injections on the node-pairs of the above-mentioned Case-A, respectively. Note that we use two simultaneous SNUs to mimic a DNU. It can be seen from Fig. 7 that, when <N7, Q> is impacted by a DNU, node Q can self-recover; when the other node-pairs are impacted by a DNU respectively, node Q can still retain its previous correct value.

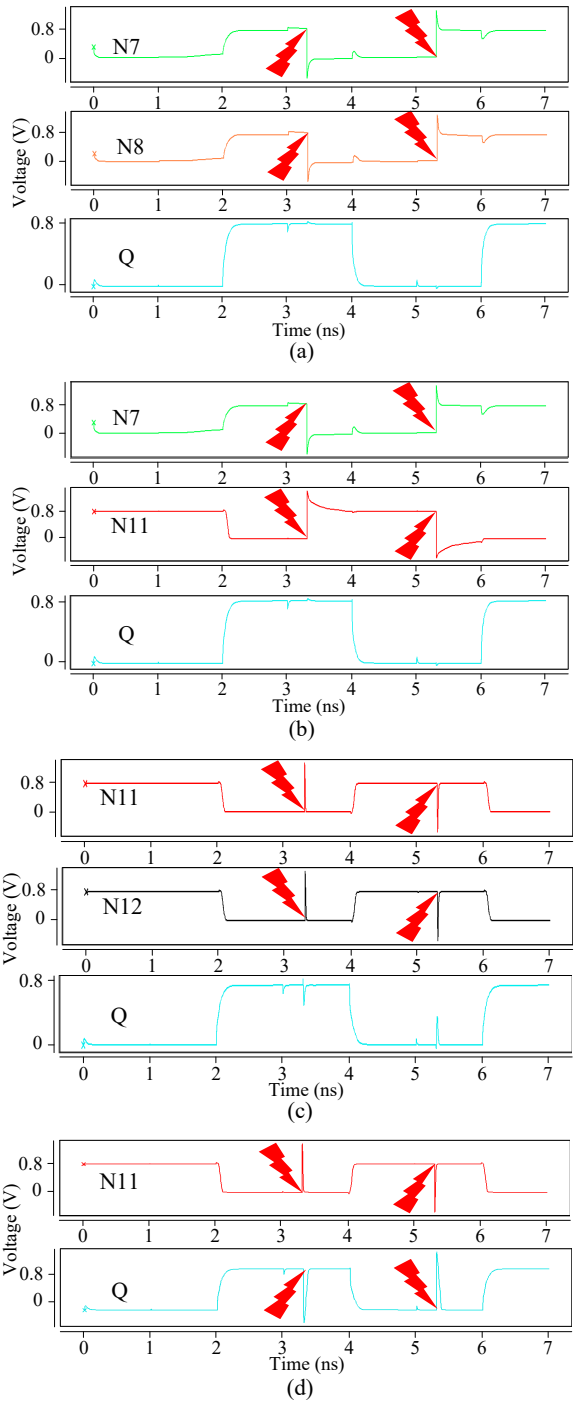

Fig. 8. Verification waveforms for the representative DNU (Case-B) injections in the HRLPFF cell. (a) DNU on <N7, N8>, (b) DNU on <N7, N11>, (c) DNU on <N11, N12> and (d) DNU on <N11, Q>.

Case B: A DNU impacts a pair of nodes from one CE. The DNU node-pairs are <N7, N8>, <N7, N11>, <N8, N11>, <N9,

N10>, <N9, N12>, <N10, N12>, <N11, N12>, <N11, Q> as well as <N12, Q>.

In this case, we can further divide Case B based on the locations of the impacted node-pairs as follows: **(B1)** When the node-pair includes double nodes of CE4/CE5, the DNU node-pairs are <N7, N8>, <N7, N11>, <N8, N11>, <N9, N10>, <N9, N12> as well as <N10, N12>. In this case, CE4/CE5 cannot block errors at its inputs. However, the outputs of CE4 and CE5 cannot have an error at the same time in this sub-case. Hence, the error at N11 or N12 can be intercepted by CE6 and this means that Q is still correct. **(B2)** When the node-pair includes double nodes of CE6, the DNU node-pairs are <N11, N12>, <N11, Q> as well as <N12, Q>. In this case, N11 and N12 can self-recover through CE4 and CE5 since the inputs of CE4 and CE5 are both correct. Hence, Q can self-recover through CE6 since the inputs of CE6 are both correct. Consequently, the proposed HRLPFF cell can provide complete tolerance against DNUs of this type. Note that, we select one node-pair from each of the sub-cases, and thus the representative DNU node-pairs in Case B are <N7, N8>, <N7, N11>, <N11, N12> as well as <N11, Q> only. In summary, the proposed HRLPFF cell can provide complete DNU-tolerance.

Figure 8 shows the verification waveforms for the representative DNU injections on the node-pairs of the above-mentioned Case B. It can be seen that, when a DNU affects <N7, N8>, <N7, N11>, or <N11, N12>, node Q can still retain its previous correct value; when a DNU affects <N11, Q>, this node-pair can self-recover. Note that, when <N11, N12> suffers from a DNU, this node-pair can self-recover as well. In summary, the above verification results demonstrate that the proposed HRLPFF cell can provide complete tolerance against SNUs and DNUs.

IV. Evaluation and Comparison Results

To do fair comparisons, the TUFF as well as all the reviewed FF cells in Fig. 2 have been designed/implemented under the same conditions as mentioned in the previous section (22nm CMOS technology from GlobalFoundries, 0.8V standard supply voltage, and room temperature).

Table I shows the reliability comparison results among the unhardened and hardened flip-flop cells. It can be seen that the TUFF cell cannot tolerate SNUs/DNUs but it is insensitive to the HIS. The DRRH-FF, DNUR-FF, HPST-FF as well as SNUR-NVFF cells can tolerate SNUs but they are sensitive to the HIS. The Quatro-FF, DICE-FF and TMR-FF cells can tolerate SNUs and are also insensitive to the HIS. Note that the proposed HRLPFF cell is not only insensitive to the HIS but also provides complete SNU/DNU tolerance.

Moreover, the critical charge (Qcirt) of these cells is shown/compared in the last column of Table I. Using the approach described in [17], we measured the Qcirt of these FF cells. It can be seen that the Qcirt of the proposed HRLPFF cell is the smallest among these FF cells. However, the proposed HRLPFF cell can provide complete tolerance against SNUs and DNUs. It can also be seen from Table I that the Qcirt of the Quatro-FF cell is the largest among these FF cells. However, the Quatro-FF cell cannot provide complete tolerance against DNUs. In summary, the proposed HRLPFF has a higher reliability than other FF cells although its Qcrit is small.

Table II shows the overhead comparison results in terms of power consumption, CLK-Q delay, silicon area as well as *power-delay-area product* (*PDAP*), among the unhardened and hardened flip-flop cells. Note that the CLK-Q delay is defined as the average of CLK-Q rise delay and CLK-Q fall delay (see Fig. 9 and Eq. (2)), the power consumption is defined as the average of dynamic power and static power, the silicon area is measured through the approach in [7], and the PDAP is defined as the product of delay, power, and area (see Eq. (3)). The PDAP is used to comprehensively compare all aspects of the overhead of all alternative FF cells (clearly, a small PDAP is better).

TABLE I
Reliability Comparison Results among the Unhardened and Hardened Flip-Flop Cells

Flip-Flops	Ref.	SNU Tolerant?	DNU Tolerant?	HIS Insensitive?	Q_{cirt} (fC)
TUFF	-	No	No	Yes	3.23
DRRH-FF	[10]	Yes	No	No	3.80
DNUR-FF	[11]	Yes	No	No	3.18
HPST-FF	[15]	Yes	No	No	4.52
SNUR-NVFF	[16]	Yes	No	No	3.73
Quatro-FF	[12]	Yes	No	Yes	6.02
DICE-FF	[14]	Yes	No	Yes	2.47
TMR-FF	-	Yes	No	Yes	3.76
HRLPFF	Proposed	Yes	Yes	Yes	1.02

TABLE II
Overhead Comparison Results among the Unhardened and Hardened Flip-Flop Cells

Flip-Flops	Power (µW)	Delay (ps)	10^{-4}×Area (μm^2)	10^{-2}× PDAP
TUFF	1.06	17.23	2.97	0.54
DRRH-FF	1.58	43.16	5.94	4.05
DNUR-FF	2.26	42.70	11.29	10.89
HPST-FF	1.00	23.00	8.32	1.91
SNUR-NVFF	1.03	18.30	5.94	1.12
Quatro-FF	4.95	38.99	6.14	11.85
DICE-FF	1.79	17.13	5.64	1.73
TMR-FF	2.97	45.38	9.66	13.02
HRLPFF	0.71	29.24	8.02	1.66

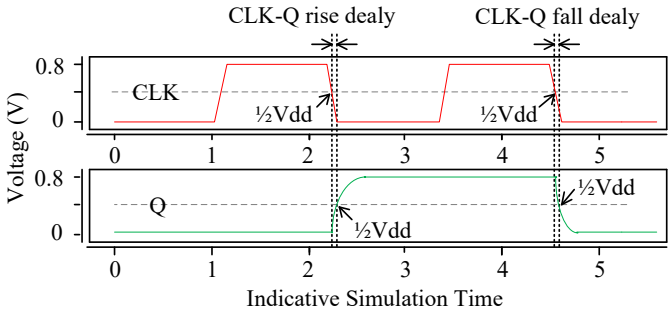

Fig. 9. CLK-Q rise delay and CLK-Q fall delay.

$$\text{CLK-Q delay} = (\text{CLK-Q fall delay} + \text{CLK-Q rise delay}) / 2 \quad (2)$$

$$\text{PDAP} = \text{CLK-Q delay} \times \text{Power} \times \text{Area} \quad (3)$$

It can be seen from Table II that, among all the alternative FF cells, the TUFF cell has a lower power, a smaller delay, and the smallest area as well as PDAP. This is because the TUFF is not SNU/DNU hardened. To tolerate SNUs and/or DNUs, by means of the RHBD approach, extra overhead has to be introduced.

In terms of power, among all the compared alternative FF cells including the proposed HRLPFF, the Quatro-FF has the highest power consumption since there is significant current competition in the Quatro cell of the FF. However, the proposed HRLPFF cell has the lowest power dissipation. This is because each node can be determined by the output of only one device, leading to the least current competition in the HRLPFF cell. Note that there is only one feedback loop (i.e., the keeper at the output stage) in the FF.

In terms of delay, among all the compared alternative FF cells, the TMR-FF cell consumes the largest delay. This is mainly because there are many devices from the input D to the output Q, i.e., the transmission path is long. Note that, as shown in Fig. 5, Q can be changed to D only at the falling edge of the CLK signal. Consequently, the devices between D and Q can determine the transmission delay. The DICE-FF has the smallest delay because the path between D and Q only includes a few inverters. The proposed HRLPFF cell consumes a moderate delay because the path between D and Q only includes a few C-elements (note that the delay of an inverter is little smaller than that of a C-element).

In terms of area, the DNUR-FF cell consumes the largest area because it uses many transistors to provide partial DNU-tolerance. Furthermore, among all the hardened FF cells including the proposed HRLPFF, the DICE-FF consumes the smallest area because it mainly employs some inverters to provide SNU tolerance/recovery as well as partial DNU tolerance so that it only uses a few transistors; however, the DICE-FF cannot provide complete tolerance against DNUs. The proposed HRLPFF cell consumes moderate area because only a moderate number of devices are employed to provide complete tolerance against SNUs and DNUs.

In terms of PDAP, the TMR-FF cell has the largest PDAP because its delay is the largest and meanwhile its power and area are not small. Furthermore, the TUFF cell consumes the smallest PDAP because its area is the smallest and meanwhile its power and delay are not large. The proposed HRLPFF cell has moderate PDAP since its power is the smallest while its delay and area are moderate.

Table III shows the quantitative comparison results of overhead among the hardened alternative FF cells. In Table III, ΔPower means the percentage of power reduction of the proposed HRLPFF cell compared with the hardened alternative FF cells, and it is calculated through Eq. (4). Hence, the meaning of ΔDelay, ΔArea as well as ΔPDAP can be known and the calculation for them can be performed similarly.

The average percentage of overhead reduction of the proposed HRLPFF cell compared with the hardened alternative FF cells are discussed here. The HRLPFF cell can reduce power consumption by roughly 65%, CLK-Q delay by 9% and PDAP by 71%, respectively, at the cost of increasement of 5.3% silicon area on average. Nevertheless, none of the state-of-the-art FF cells can provide complete tolerance against DNUs. Furthermore, the proposed HRLPFF cell is insensitive to the HIS and thus Q is reliable. In summary, compared with all the hardened alternative FF cells, our proposed HRLPFF cell can not only provide the highest robustness but also the lowest power consumption as well as a moderate overhead in terms of delay and area.

$$\Delta Power = \frac{Power_{\text{comparedFF}} - Power_{\text{proposedFF}}}{Power_{\text{comparedFF}}} \times 100\% \qquad (4)$$

TABLE III
QUANTITATIVE COMPARISON RESULTS OF OVERHEAD AMONG THE HARDENED FLIP-FLOP CELLS

Flip-Flops	ΔPower (%)	ΔDelay (%)	ΔArea (%)	ΔPDAP (%)
DRRH-FF	55.06	32.25	-35.02	59.01
DNUR-FF	68.58	31.52	28.96	84.76
HPST-FF	29.00	-27.13	3.61	13.09
SNUR-NVFF	31.07	-59.78	-35.02	-48.21
Quatro-FF	85.66	25.01	-30.62	85.99
DICE-FF	60.34	-70.69	-42.20	4.05
TMR-FF	76.09	35.57	16.98	87.25
Average	65.13	9.30	-5.27	71.27

One may question about the fact that there is no any feedback loop in the master latch of the proposed HRLPFF cell (although the intrinsic capacitances of these CEs can temporarily retain the value once D is cut off when the master latch works in hold mode). Nevertheless, even though there is probably a risk with the master latch in hold mode (CLK = 0), its value has already been transmitted to the slave latch. Hence, no changes in N1~N6 will affect node M at all (due to the error interception of CEs). If node M suffers from strike and is discharged, the error may propagate to the slave latch but will have to fight against Q. If Q is strong enough (it has to be stronger as it has to drive all loads downstream), it would not overturn Q. In other words, the combined capacitance of nodes M and Q as well as all those distributed capacitances in the TG CE4 and CE5 make it much less likely to be upset so that the risk is low. For the other (CLK = 1) phase, any upset in the master latch is irrelevant since as the upstream D-value will correct it when clock resumes. Therefore, this problem should be minimal if the clock stopping logic is a little smarter.

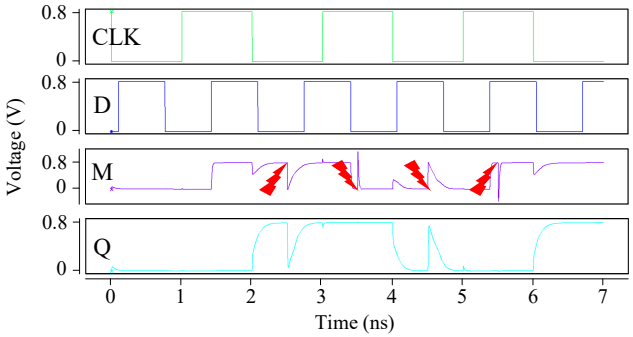

Fig. 10. Simulation waveforms for the error injections at M of the proposed HRLPFF cell.

Figure 10 shows the simulation waveforms for the error

injections at M in the proposed HRLPFF cell. When CLK = 1, the value of D can be transmitted to M. When CLK = 0, the value of M can be transmitted to Q. When CLK = 0, for the errors injected at M (see the first and third error injections), although the errors at M can propagate to Q, M can self-recover through CE3 whose inputs are both correct, and thus Q can also self-recover. When CLK = 1, the value of D can be transmitted to M but the value of M cannot be transmitted to Q. For any error injected at M (see the second and fourth error injections) cannot propagate to Q and M can self-recover immediately through D. Moreover, as mentioned in the above section, if one of the impacted nodes belongs to the master latch while the other belongs to the slave latch, the DNU is equivalent to two simultaneous SNUs. Therefore, the HRLPFF cell can tolerate this type of DNUs where node M is also impacted.

FF cells, particularly those implemented in nanoscale CMOS technologies, are becoming more sensitive to *process, supply voltage, and temperature* (*PVT*) variations. Therefore, we also used the same approach as in [18] to evaluate the PVT variations effects on FF cells. According to [18], when evaluating the effects of PVT variations on a latch, only one parameter is changed at a time while the other parameters remain unchanged. For example, to evaluate the impact of supply voltage variations on a latch, we only change the supply voltage while keeping all other parameters constant.

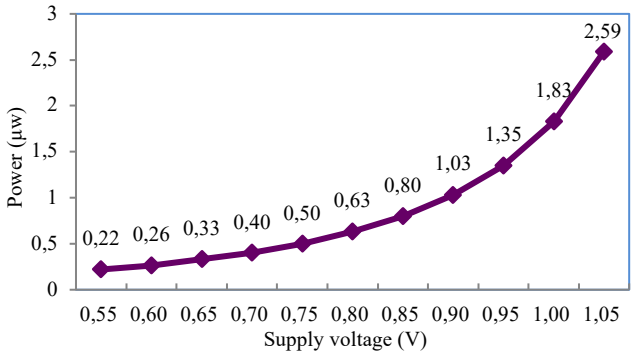

Fig. 11. The effect of supply voltage variations on power for HRLPFF.

The effect of supply voltage variations on power for the proposed HRLPFF cell is shown in Fig. 11. There are eleven samples for supply voltage variations with a step of 0.05V from 0.55 to 1.05V. These samples form ten curve segments, i.e., <0.55, 0.60>, <0.60, 0.65>, <0.65, 0.70>, <0.70, 0.75>, <0.75, 0.80>, <0.80, 0.85>, <0.85, 0.90>, <0.90, 0.95>, <0.95, 1.00> and <1.00, 1.05>. The slope of each curve segment can be computed. For example, the slope of <0.55, 0.60> is equal to the difference between the power consumption measured at 0.55V and 0.60V. Then, the *average slope* (*AS*) of the entire curve (<0.55, 1.05>) can be obtained by averaging the absolute value of the slope of 10 curve segments. Table IV shows the calculation result of each slope as well as the AS. Clearly, AS can represent the sensitivity of the power consumption of the HRLPFF cell to the variation of the supply voltage. The AS can be utilized to assess the sensitivity of each FF cell to PVT variations. We assume that D_1, D_2, D_3, …, D_i are samples of delay or power of a latch, where i is the sample count. Then, the AS (sensitivity) can be calculated with Eq. (5), respectively.

$$AS = \frac{1}{i-1}\sum_{k=2}^{i}|D_k - D_{k-1}| \quad (5)$$

TABLE IV
THE CALCULATION RESULT OF EACH SLOPE FOR FIG. 11

Curve	Slope	Curve	Slope
<0.55, 0.60>	0.04	<0.80, 0.85>	0.17
<0.60, 0.65>	0.07	<0.85, 0.90>	0.23
<0.65, 0.70>	0.07	<0.90, 0.95>	0.32
<0.70, 0.75>	0.10	<0.95, 1.00>	0.48
<0.75, 0.80>	0.13	<1.00, 1.05>	0.76

* The average slope is 0.24.

We calculated the AS (sensitivity) of delay or power of each FF cell to PVT variations with Eq. (5) and the results are shown in Table V. In Table V, ECLs denote *effective channel length* of transistors; "Supply voltage vs. Delay", "Temperature vs. Delay", "Threshold-voltage increment vs. Delay" and "ECL vs. Delay" denote the sensitivity of delay of each FF cell to variations of supply voltage, temperature, threshold-voltage and ECL, respectively; "Supply voltage vs. Power", "Temperature vs. Power", "Threshold-voltage increment vs. Power", and "ECL vs. Power" denote the sensitivity of power consumption of each FF cell to variations of supply voltage,

TABLE V
SENSITIVITY OF DELAY OR POWER OF THE ALTERNATIVE HARDENED FF CELLS TO PVT VARIATIONS

Latch	Supply voltage vs. Delay	Supply voltage vs. Power	Temperature vs. Delay	10^2 × Temperature vs. Power	Threshold-voltage increment vs. Delay	10^2 × Threshold-voltage increment vs. Power	ECL vs. Delay	10^2 × ECL vs. Power
TUFF	12.56	0.52	7.72	7.00	1.68	3.60	4.99	4.00
DRRH-FF	18.59	0.57	17.67	8.63	4.27	4.00	8.46	11.70
DNUR-FF	14.02	0.97	11.08	11.75	5.90	11.80	8.27	10.90
TMR-FF	19.08	1.43	16.12	18.38	5.11	10.30	10.66	15.20
Quatro-FF	12.56	1.82	10.79	19.50	2.42	23.40	37.70	39.10
DICE-FF	5.79	0.59	3.30	5.75	1.87	4.60	5.31	5.40
HPST-FF	6.55	0.45	4.93	7.13	4.37	6.10	6.44	6.20
SNUR-NVFF	6.88	0.40	4.16	4.75	2.67	3.20	4.36	3.90
HRLPFF	9.92	0.24	5.53	3.25	5.22	1.60	8.69	2.10

temperature, threshold voltage and ECL, respectively. The standard supply voltage was set to 0.8V but ranged from 0.75V to 1.25V, increasing 0.05V at each step for variation simulations. The standard temperature was room temperature but ranged from -20°C to 120°C, increasing 20°C at each step for variation simulations. The standard threshold-voltage increment was set to 0V but ranged from 0V to 0.1V, increasing 0.01V at each step for variation simulations. The standard ECL was set to 22nm but ranged from 22nm to 32nm, increasing 1nm at each step for variation simulations.

In terms of "Supply voltage vs. Delay", it can be seen from Table V that the delay of DRRH-FF and TMR-FF cells is more sensitive to supply voltage variations, while the delay of the proposed HRLPFF cell is moderately sensitive to supply voltage variations. In terms of "Supply voltage vs. Power", it can be seen from Table V that the power consumption of HPST-FF, SNUR-NVFF, and the proposed HRLPFF is less sensitive to supply voltage variations. In particular, the power consumption of the proposed HRLPFF cell is the least sensitive to supply voltage variations.

In terms of "Temperature vs. Delay", it can be seen from Table V that the delays of DRRH-FF, DNUR-FF, TMR-FF, and Quatro-FF cells are more sensitive to temperature variations, whereas the delay of the proposed HRLPFF cell is less sensitive to temperature variations. In terms of "Temperature vs. Power", it can be seen from Table V that the power consumptions of DNUR-FF, TMR-FF, and Quatro-FF cells are more sensitive to temperature variations, while the power consumption of the proposed HRLPFF cell is the least sensitive to temperature variations.

In terms of "Threshold-voltage increment vs. Delay", it can be seen from Table V that the delay of TUFF and DICE-FF is less sensitive to threshold-voltage increment variations, and the delay of the proposed HRLPFF cell is more sensitive to threshold-voltage increment variations. In terms of "Threshold-voltage increment vs. Power", it can be seen from Table V that the power consumption of the HRLPFF cell is the least sensitive to threshold-voltage increment variations, while the power consumption of DNUR-FF, TMR-FF, and Quatro-FF cells is less sensitive to threshold-voltage increment variations.

In terms of "ECL vs. Delay", it can be seen from Table V that the delay of the SEUR-NVFF cell is the least sensitive to ECL variations, and the delay of the proposed HRLPFF cell is moderately sensitive to ECL variations. In terms of "ECL vs. Power", it can be seen from Table V that the power consumption of the proposed HRLPFF cell is the least sensitive to ECL variations, while the power consumptions of the TMR-FF and Quatro-FF cells are quite sensitive to ECL variations compared with the other FF cells. In summary, the delay of the proposed HRLPFF cell is less or only moderately sensitive to PVT variations and its power consumption is the least susceptible to PVT variations.

V. Conclusion and Further Work

Due to the aggressive shrinking of transistor feature sizes, DNU is becoming a more and more severe type of soft errors. However, few existing FF cells can provide completely DNU-tolerance. To ensure high reliability with cost-effectiveness, we have proposed a novel HRLPFF cell featuring complete SNU and DNU tolerance. The proposed cell uses combined CEs in a multi-level manner to efficiently intercept DNUs, uses a keeper at the output stage to avoid HIS-sensitivity, and uses a small number of devices from the input to the output to reduce CLK-Q transmission delay. Comprehensive evaluations demonstrate that the proposed HRLPFF cell can indeed achieve the highest reliability with the smallest power consumption.

Reference [19] has reported a scan FF which is very interesting. Our further work will focus on the hardened scan FF designs.

Acknowledgement

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