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Abstract—Quantum-dot cellular automata (QCA) is a novel nano-electronic technology. QCA has attracted wide attention due to its extremely small feature sizes at the molecular or even atomic scale and ultra-low power consumption, making it a promising candidate to replace the complementary metal oxide semiconductor (CMOS) technology. Binary-Coded Decimal (BCD) adders are widely used in industrial computing. In this paper, we propose two types of excess-3 code (XS-3) based BCD adders (XS-3DAs). We use ripple-carry adders (RCA) and parallel binary adders (PBA) to construct XS-3DAs in QCA Designer tool, respectively. The PBA-based XS-3DA is constructed with a new correction logic. 4-bit, 8-bit, and 16-bit XS-3DAs are constructed based on the two proposed XS-3DAs, respectively. Comparisons show that, with the increase of design scaling, the delay and area-delay product (ADP) of the PBA-based XS-3DAs can be significantly reduced in comparison with that of the RCA-based XS-3DAs. Compared with the 16-digit RCA-based XS-3DA, the cell count, area, delay and ADP of the proposed 16-digit PBA-based XS-3DA are reduced by 37.88%, 25.99%, 37.68% and 53.88%, respectively.

Index Terms—Quantum-dot cellular automata, Excess-3 code, BCD adder

I. Introduction

The processing of all data in computers is essentially the processing of binary numbers. Only binary numbers can be directly recognized and processed by computers, and people are more accustomed to using decimal numbers in practice. Therefore, there is a strong need for computers to directly process data expressed in decimal form.

In the near future, the CMOS technology will encounter bottlenecks due to its short channel effect and the high lithography cost. Nanotechnologies, especially QCA, have become the promising alternatives, which provide new choices for the design and manufacture of integrated circuits. The QCA technology is a widely studied nanotechnology. Its high device density, fast switching speeds and ultra-low energy consumption indicate enormous research potentials and broad application prospects.

The concept and advantages of XS-3 is briefly introduced here. The XS-3 is formed by the addition of 8421 BCD codes and (0011)2, which is a self-complementary BCD code. This code has a biased representation. It is easy to be 9's complemented by inverting all bits, which facilitates the calculation. For example, the XS-3 of 2 are 0101 and the binary number after reversing each digit is 1010 that is exactly the XS-3 of 7. Moreover, when the sum of two XS-3s is greater than 9, the carry bit of a 4-bit binary adder can be set high. So far, researchers have proposed some QCA-based BCD converters, i.e., 8421 BCD code to the XS-3 converters and XS-3 to 8421 BCD code converters [1-2]. The advantages of XS-3 motivate us to use it to design BCD adders.

There are many previous works on BCD adders. In 2008, Taghizadeh et al firstly proposed a modular design of a BCD adder in QCA [3]. In 2017, Abedi et al proposed a QCA decimal full adder that is mostly composed of fully utilized majority gates (i.e., with no constant inputs), and rarely includes partially utilized majority gates [4]. A new correction logic formulation was proposed to reduce the delay of single and multi-digit BCD adders [5]. In 2018, Zhang et al proposed a carry look ahead structure for calculating all intermediate output carries and used this method to design multi-digit decimal adders [6]. In 2018, Li et al proposed a new structure for BCD adders. It achieved a more compact layout by making some equivalent replacement and introducing XOR operations [7]. In 2021, Chu et al proposed a BCD adder based on 3-input XOR gates and 3-input majority gates [8]. The introduction of 3-input XOR gates is conducive for achieving compact logic representations. All of the above BCD adders are designed based on 8421 BCD code.

To the best of our knowledge, there is no QCA-based XS-3DAs in the literature. In this paper, we propose RCA-based and PBA-based XS-3DAs. The PBA-based XS-3DA is constructed using a new correction logic. The RCA-based and PBA-based XS-3DAs are implemented in the QCA Designer tool [9]. We analyze the characteristics of the proposed two types of XS-3DAs. Comparisons show that, with the increase of design scaling, the delay and ADP of the PBA-based XS-3DAs can be significantly reduced compared with that of RCA-based XS-3DAs.

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The rest of the paper is organized as follows: Section II introduces the preliminaries of the QCA technology. Section III presents RCA-based and PBA-based XS-3DAs. Section IV details the simulation results and comparisons. Section V concludes this paper.

II. Preliminaries of QCA

QCA cells are the basic unit in QCA. A common QCA cell is composed of two free electrons and four quantum dots. Due to the effect of electrostatic force, the free electrons in a cell can eventually get into two stable states, which represent two binary states. The unique clock mechanism in QCA ensures the stable transmission of signals. Figure 1 shows the cells and clock mechanism of QCA. A QCA clock has four clock phases: switch, hold, release, and relax. In the switch phase, the QCA cells enter the polarization state. In the hold phase, the QCA cells reaches the maximum polarity and remain unchanged. In the release phase, the polarity of the QCA cells begins to decrease. In the relax phase, the QCA cells completely lose polarization and reach a non-polarized state.

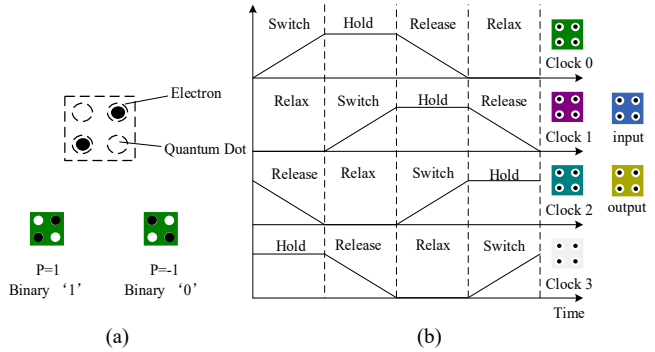

Fig. 1. QCA cells and QCA clock. (a) QCA cells and (b) QCA clock.

The basic logic devices in QCA are 3-input majority gates and inverters. Figure 2 shows some devices in QCA. The inverter can reverse the input signal, and the 3-input majority gate can output the signal that follows the majority rule as shown in Fig. 2 (a)-(b). The XOR function can be realized by a QCA-based gate, which is different from the construction of the XOR gate in the CMOS circuit. Figure 2 (c) shows a 3-input XOR gate.

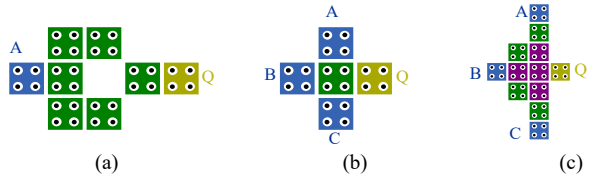

Fig. 2. QCA basic gates. (a) inverter, (b) 3-input majority gate and (c) 3-input XOR gate.

III. Proposed RCA-based and PBA-based XS-3DAs

A. RCA-based XS-3DAs

The XS-3 is formed by the addition of 8421 BCD codes and $(0011)_2$. When two decimal numbers represented by XS-3s are added, the carry can be generated correctly, but the sum must be corrected. The correction method is as follows. If the carry is "1", the sum needs to be added with $(0011)_2$; if the carry is "0", the sum needs to be added with $(1101)_2$. The two correction signals $(0011)_2$ and $(1101)_2$ can be generated by the correction logic circuit.

Figure 3 shows the block diagram of the 1-digit RCA-based XS-3DA. It can be seen that, the 1-digit RCA-based XS-3DA includes 4-bit binary adder (ADD_1), correction logic (CL) and 4-bit binary adder (ADD_2). The signals $dA_{3:0}$ and $dB_{3:0}$ are two decimal input numbers represented by excess-3 codes. The signals dC_{out} and $dS_{3:0}$ are the carry and sum of the 1-digit XS-3DA. The ADD_1 adds the three signals of $dA_{3:0}$, $dB_{3:0}$ and dC_{in} to obtain binary $bS_{3:0}$ and carry bC_{out}. At this time, the carry bC_{out} is correct and does not need to be corrected. The function of the CL circuit is to generate the correction signal. It is composed of an inverter, which can generate $cL_{3:0}$. When bC_{out} is 1, $cL_{3:0}$ is $(0011)_2$; when bC_{out} is 0, $cL_{3:0}$ is $(1101)_2$. ADD_2 adds $cL_{3:0}$ and $bS_{3:0}$ to get decimal $dS_{3:0}$.

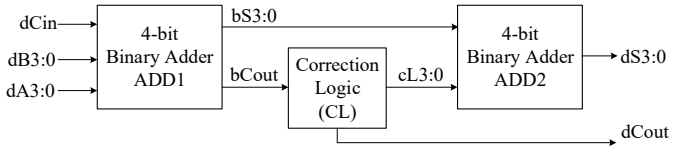

Fig. 3. Block diagram of 1-digit RCA-based XS-3DA.

The delay of the outputs (C_{out} and $dS_{3:0}$) of the 1-digit RCA-based XS-3DA can be expressed by formulas (1)-(2).

$$D(1)_C = D_{ADD1} \quad (1)$$

$$D(1)_S = D_{ADD1} + D_{CL} + D_{ADD2} \quad (2)$$

D_{ADD1}, D_{CL} and D_{ADD2} represent the delay of ADD_1, CL and ADD_2, respectively.

The delay of the outputs (C_{out} and $dS_{3:0}$) of the n-digit RCA-based XS-3DA can be expressed by formulas (3)-(4).

$$D(n)_C = nD_{ADD1} \quad (3)$$

$$D(n)_S = nD_{ADD1} + D_{CL} + D_{ADD2} \quad (4)$$

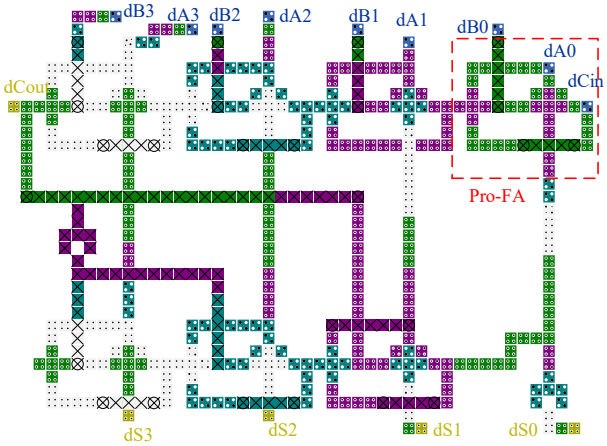

Fig. 4. Layout of the proposed 1-digit RCA-based XS-3DA.

Previous studies have proved that the introduction of XOR logic to construct full adders can effectively reduce overhead of QCA circuits [8]. We use a 3-input XOR gate and a 3-input majority gate to propose a full adder (see Pro-FA in Fig. 4 and Table II) to reduce circuit overhead. Figure 4 shows the layout of the proposed 1-digit RCA-based XS-3DA in the QCA

Designer tool. The cells marked with "○" are on the second layer, and the cells marked with "×" are on the third layer. The $dA_{3:0}$ and $dB_{3:0}$ are two groups of input signals. The dC_{in} represents the input carry signal, dC_{out} represents the output carry signal, and $dS_{3:0}$ represents the sum signal. The design consists of 539 cells, with an area of 0.60 um^2, a delay of 2.25 clocks for signal $dS_{3:0}$, and a delay of 1.25 clocks for the signal dC_{out}. It is a 3-layer design. ADD_1 and ADD_2 of the proposed 1-digit RCA-based XS-3DAs are implemented using the proposed FAs. Because the signal cL_0 is always "1", the rightmost FA of ADD_2 can be replaced by an inverter. N-digit RCA-based XS-3DAs can be constructed using the proposed RCA-based XS-3DAs.

B. PBA-based XS-3DAs

Figure 5 shows a block diagram of BCD adders [6]. Ajitha et al and Zhang et al have applied the block diagram to design BCD adders based on 8421 BCD codes, respectively [5-6]. We apply this method for the construction of XS-3DAs.

The following is the analysis of the proposed PBA-based XS-3DAs. The signals $dA_{3:0}$ and $dB_{3:0}$ are two decimal input numbers represented by excess-3 codes. It can be seen from Fig. 5 that, after adjusting the input of signal dC_{in}, when the signal $bS_{3:0}$ is greater than or equal to "10", the carry signal bC_{out} is correct no matter the value of dC_{in}; when $bS_{3:0}$ is less than "9", the carry signal bC_{out} is correct no matter the value of dC_{in}; when $bS_{3:0}$ is equal to "9" and dC_{in} is equal to "0", the carry signal bC_{out} is correct; when $bS_{3:0}$ is equal to "9" and dC_{in} is equal to "1", the signal bC_{out} is "0", which is wrong and needs to be corrected. The output carry dC_{out} of the XS-3DAs can be rewritten as formula (5).

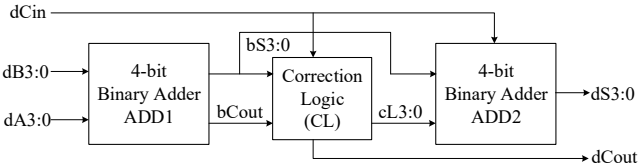

Fig. 5. Block diagram of 1-digit BCD adder [8].

$$dC_{out} = bC_{out} + (bS_{3:0} == 9)dC_{in} \quad (5)$$

The excess-3 code of "9" is $(1111)_{XS-3}$. Formula (5) can be rewritten as formula (6).

$$\begin{aligned} dC_{out} &= bC_{out} + (bS_{3:0} == (1111)_{XS-3})dC_{in} \\ dC_{out} &= bC_{out} + bS_3 \cdot bS_2 \cdot bS_1 \cdot bS_0 \cdot dC_{in} \\ dC_{out} &= bC_{out} + (bS_3 \cdot bS_2) \cdot (bS_1 \cdot bS_0) \cdot dC_{in} \end{aligned} \quad (6)$$

Figure 6 shows the proposed CL circuit of PBA-based XS-3DAs. The CL circuit of the proposed PBA-based XS-3DAs can process signals $bS_{3:0}$, bC_{out} and dC_{in} to obtain signals dC_{out}. Figure 7 shows the schematic diagram of the proposed PBA-based XS-3DAs. Compared with the CL circuit of the RCA-based XS-3DAs, although the proposed CL circuit of the PBA-based XS-3DAs has five more gates, the signal dC_{in} can flow directly into the CL circuit without flowing through ADD_1 and each ADD_1 of n-digit XS-3DA can be operated in parallel to reduce delay. Theoretically, when dC_{in} is inputted, the carry signal dC_{out} can be output after a delay of 0.5 clocks in QCA circuit, which can significantly reduce the delay of the n-digit XS-3DAs.

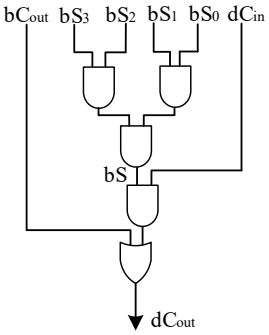

Fig. 6. The proposed CL circuit of PBA-based XS-3DAs.

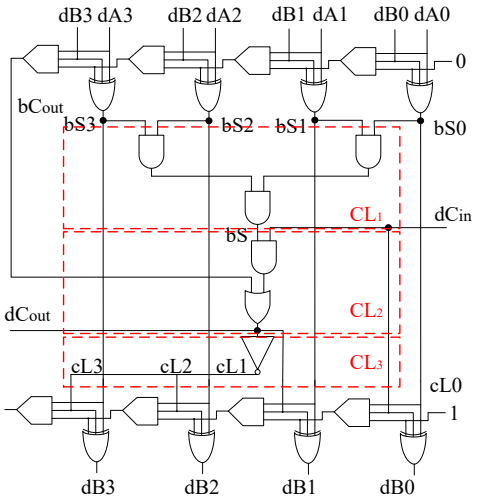

Fig. 7. Circuit diagram of the proposed 1-digit PBA-based XS-3DA.

The delay of the outputs (C_{out} and $dS_{3:0}$) of the proposed 1-digit PBA-based XS-3DA can be expressed by formulas (7)-(8). For brevity, the CL circuit is divided into CL_1, CL_2 and CL_3 as shown in Fig. 7.

$$D(1)_C = D_{ADD1} + D_{CL1} + D_{CL2} \quad (7)$$

$$D(1)_S = D_{ADD1} + D_{CL} + D_{ADD2} \quad (8)$$

The delay of the outputs (C_{out} and $dS_{3:0}$) of the proposed n-digit PBA-based XS-3DA can be expressed by formulas (9)-(10).

$$D(n)_C = D_{ADD1} + D_{CL1} + nD_{CL2} \quad (9)$$

$$D(n)_S = D_{ADD1} + D_{CL1} + nD_{CL2} + D_{CL3} + D_{ADD2} \quad (10)$$

Figure 8 shows the layout of the proposed 1-digit PBA-based XS-3DA implemented in the QCA Designer tool. The proposed 1-digit PBA-based XS-3DA is composed of 715 cells, with an area of 0.68um^2, a delay of 3.25 clocks for signal $dS_{3:0}$ and a delay of 2.25 clocks for the signal dC_{out}. It is a 3-layer design. The low carry input of the leftmost FA of ADD_1 is set to "-1", and the carry signal dC_{in} is directly inputted into the CL circuit and ADD_2 for calculation. The proposed designs can use the USE mechanism [13]. The USE mechanism can flexibly create feedback paths of any length and a well-defined clocking circuitry. The clock circuitry of the USE mechanism is simple and the design flexibility is high.

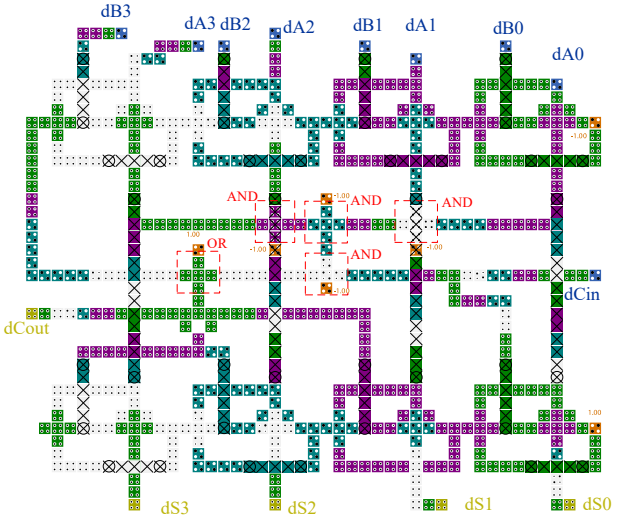

Fig. 8 Layout of the proposed 1-digit PBA-based XS-3DA.

IV. Simulation and Comparisons

A. Simulation Results

Figure 9 shows the simulation results of the proposed 1-digit PBA-based XS-3DA in the QCA Designer tool. The simulation engine of QCA Designer was set to the coherence vector engine. The other parameters of QCA Designer are set as default. The delay of signal dC_{out} is set to the same delay as signal $dS_{3:0}$ to synchronize outputs.

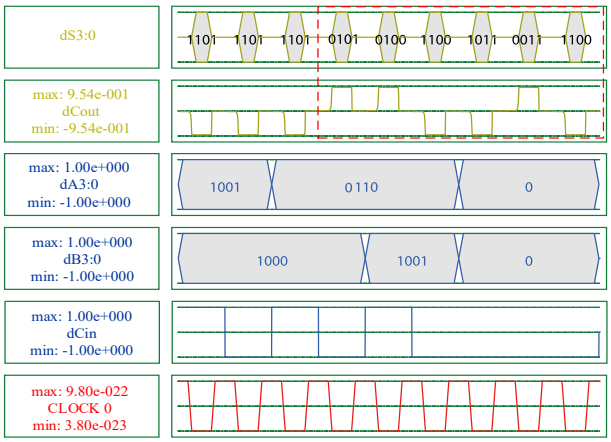

Fig. 9. Simulation results of the proposed 1-digit PBA-based XS-3DA.

B. Complexity Analysis

Table I shows the theoretical comparisons of the proposed XS-3DAs. We estimate area and delay based on the number of used QCA-based gates in the XS-3DAs. D_s presents the delay of the signal $dS_{n-1:n-4}$ and D_c presents the delay of the signal dC_{out}. Formula (11) presents the calculation method of ADP.

$$ADP = Area \times D_s \quad (11)$$

The proposed 1-digit RCA-based XS-3DA consists of 16 QCA-based gates, including 7 majority gates, 2 inverters and 7 XOR gates. Thus, the area complexity of the n-digit RCA-based XS-3DA is 16n. The used QCA-based XOR gate requires a delay of a gate for calculation. The QCA-based ADD_1 and ADD_2 both requires a delay of 4 gates for calculation. The CL circuit of the proposed RCA-based XS-3DA is composed of an inverter, which requires a delay of a gate. It can be seen from formulas (3)-(4) that, the input signals of the n-digit RCA-based adder flow through n ADD_1s to get the signal dC_{out}, and then flow through one CL circuit and one ADD_2 to get the signal $dS_{n-1:n-4}$. Therefore, the signals dC_{out} and $dS_{n-1:n-4}$ of the proposed n-digit RCA-based XS-3DA require a delay of 4n gates and 4n+5 gates, respectively.

TABLE I. THEORETICAL COMPARISONS OF THE PROPOSED XS-3DAS

Design	MG	INV	XOR	Area	Delay		ADP
					D_S	D_C	
Pro-RCA1	7	2	7	16	9	4	144
Pro-RCAn	7n	2n	7n	16n	4n+5	4n	$64n^2$+80n
Pro-PBA1	13	1	8	22	13	8	286
Pro-PBAn	13n	n	8n	22n	2n+11	2n+6	$44n^2$+242n

The proposed 1-digit PBA-based XS-3DA consists of 22 QCA-based gates, including 13 majority gates, 1 inverter and 8 XOR gates. Thus, the area complexity of the n-digit PBA-based XS-3DA is 22n. The CL_1, CL_2 and CL_3 of the proposed PBA-based XS-3DA require a delay of two gates, two gates and one gate, respectively. It can be seen from formulas (9)-(10) that, the input signals of the n-digit PBA-based XS-3DA flow through one ADD_1, one CL_1 and n CL_2s to get the signal dC_{out}, then flow through one CL_3 and one ADD_2 to get the signal $dS_{n-1:n-4}$. Therefore, the signals dC_{out} and $dS_{n-1:n-4}$ of the proposed n-digit PBA-based XS-3DA require a delay of 2n+6 gates and 2n+11 gates, respectively.

C. Comparisons

Table II shows the comparison of alternative adders. The proposed multilayer adder has a compact and regular layout, and the positions of the low carry terminal and the high output terminal are easy to access, which is very convenient for the construction of RCA. The proposed adder has a low delay and can be flexibly used in the design of decimal adders.

TABLE II. COMPARISONS OF ALTERNATIVE FAS

Design	Cell Count	Area (um^2)	Delay (Clocks)	ADP	Layer type	Total energy dissipation
[10]	86	0.09	0.75	0.068	M	2.92e-002
[11]	58	0.03	0.75	0.023	M	2.59e-002
[12]	57	0.04	1.00	0.040	C	1.86e-002
Pro-FA	57	0.05	0.50	0.025	M	2.89e-002

Table III shows the comparisons of the decimal adders in terms of cell count, delay, area, ADP and layer type. Based on the proposed two XS-3DAs, 4-digit, 8-digit and 16-digit XS-3DAs are constructed, respectively. The decimal adders in [4-8] are based on 8421 BCD code. It can be seen from Table III that the proposed RCA-based XS-3DAs have the lowest area and delay overhead. The proposed PBA-based XS-3DAs has the lowest area and ADP. Note that, the complexity analysis is based on the number of QCA gates, without considering the QCA wires for synchronous output. With the scale of the designs increases, the delay of the RCA-based XS-3DA begins to be greater than that of the PBA-based XS-3DA, so that the RCA-based XS-3DA requires more QCA wires to synchronize outputs, resulting in the increase of its area. It can be

calculated from Table III that, compared with the 16-digit RCA-based XS-3DAs, the cell count, area, delay and ADP of the 16-digit PBA-based XS-3DAs are reduced by 37.88%, 25.99%, 37.68% and 53.88%, respectively.

TABLE III. COMPARISONS OF THE DECIMAL ADDERS

Design	Digits	Cell Count	Area (um^2)	Delay (Clocks)	ADP	Layer type
RCA-based [4] (8421)	1	669	2.28	3.00	6.84	M
	4	3981	11.04	8.25	91.08	M
	8	11717	34.32	15.25	523.38	M
RCA-based [6] (8421)	1	918	3.03	4.00	12.12	M
	4	4226	17.04	7.00	119.28	M
	8	10091	48.27	11.00	530.97	M
PBA-based [6] (8421)	1	1294	2.64	3.75	9.90	M
	4	5500	11.46	5.25	60.17	M
	8	13456	35.13	7.25	254.69	M
RCA-based [7] (8421)	1	594	2.16	2.50	5.40	M
RCA-based [8] (8421)	1	476	0.64	2.25	1.44	C
	4	3075	5.37	8.25	44.30	C
	8	9265	18.15	16.25	294.94	C
RCA-based [8] (8421)	1	419	1.08	2.25	2.43	M
	4	2178	7.56	6.75	51.03	M
	8	5710	23.88	12.75	304.47	M
PBA-based [8] (8421)	1	733	1.01	3.50	3.54	C
	4	3494	4.98	6.50	32.37	C
	8	8572	12.73	10.50	133.67	C
PBA-based [8] (8421)	1	588	1.47	3.00	4.41	M
	4	2400	6.81	3.75	25.54	M
	8	5089	15.66	4.75	74.39	M
Pro-RCA (XS-3)	1	539	0.60	2.25	1.35	M
	4	2771	3.16	5.25	16.59	M
	8	7315	9.08	9.25	83.99	M
	16	28760	28.70	17.25	495.08	M
Pro-PBA (XS-3)	1	715	0.68	3.25	2.21	M
	4	3253	3.43	4.75	16.29	M
	8	7329	7.77	6.75	52.45	M
	16	17867	21.24	10.75	228.33	M

TABLE IV. COMPARISONS OF ENERGY DISSIPATION OF THE PROPOSED XS-3DAS

Design	Total energy dissipation (eV)	Average energy dissipation (eV)
Pro- RCA1	1.97e-001	1.79e-002
Pro- RCA4	8.70e-001	7.91e-002
Pro- RCA8	1.90e-000	1.72e-001
Pro- RCA16	4.50e-000	4.09e-001
Pro- PBA1	2.24e-001	2.04e-002
Pro- PBA4	9.94e-001	9.04e-002
Pro- PBA8	2.07e-000	1.88e-001
Pro- PBA16	4.45e-000	4.05e-001

Table IV shows the comparisons of energy dissipation of the proposed XS-3DAs. The energy dissipation of the proposed designs was estimated by QCA Designer-E tool. Because the CL circuit of the 1-digit PBA-based XS-3DA is more complex, its energy dissipation is greater than that of the 1-digit RCA-based XS-3DA. However, with the design scale increases, the energy dissipation of PBA-based XS-3DA is gradually less than that of RCA-based XS-3DA (see Pro-RCA16 vs Pro- PBA16).

V. CONCLUSION

In this paper, we have proposed novel RCA-based and PBA-based XS-3DAs in the QCA Designer tool. A new correction circuit is used to construct the PBA-based XS-3DAs. Our proposed RCA-based and PBA-based XS-3DAs show excellent performance in terms of area and ADP. We have analyzed and compared the characteristics of the two types of XS-3DAs. The proposed CL circuit can significantly reduce the delay and ADP of the n-digit RCA-based XS-3DAs, thus saving the overall cost of QCA circuit designs.

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