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Article

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Abstract: Quantum-dot cellular automata (QCA) has been considered as a novel nano-electronic technology. With the advantages of low power consumption, high speed, and high integration, QCA has been treated as the potential replacement technology of the CMOS (complementary metal oxide semiconductor) which is currently used in the industry. This paper presents a QCA-based array multiplier with an optimized delay. This type of circuit is the basic building block of many arithmetic logic units and electronic communication systems. Compared to the existing array multipliers, the proposed multipliers have the smallest cell count and area. The proposed designs used a compact clock scheme to reduce the carry delay of the signals. The 2 × 2 array multiplier clock delay was reduced by almost 65% compared to the existing designs. Moreover, since the multiplier exhibits a good scalability, for further proof, we proposed a 3 × 3 array multiplier. Simulation results asserted the feasibility of the proposed multipliers. Extensive comparison results demonstrated that when the design scaling was increased, our proposed designs still displayed an efficient overhead in terms of the delay, cell count, and area. The QCADesigner tool was employed to validate the proposed array multipliers. The QCADesigner-E was used to measure the power dissipation of the alternative compared solutions.

Keywords: QCA; array multiplier; XOR gate; full adder

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1. Introduction

Transistor feature sizes of silicon-based CMOS elements are rapidly approaching their limits. The quantum tunneling effect and the coulomb blockade of devices are also becoming more and more severe, and together, all of these bring great challenges to the stability and reliability of the CMOS circuits [1].

Since nano-electronic devices possess the advantages of having a high speed, a low power dissipation, and a high integration ability, nano-electronic devices have become the research focus of the next-generation electronic devices. These devices mainly include organic thin-film transistors, transparent oxide-thin-film transistors, resonant tunneling diodes, single-electron transistors, carbon nanotubes, quantum dot cellular automata (QCA), and so on [2,3]. QCA is favored by researchers because of its unique operating mechanism and advantages. QCA circuits output data based on the cellular automata principle and the coulomb interaction force. A QCA cell comprises free electronics, quantum dots, and tunnel junctions. A QCA cell can represent binary data by the positions occupied by the electrons in the cell [4]. The mechanism of operations for the QCA circuits is quite different from that of the CMOS circuits. The QCA circuit transmits data through the coulomb force between cells. QCA circuits have very low power consumption, high integration, fast operation speeds, and stable operations at room temperature [5]. QCA

technology provides a new solution to break through the performance bottleneck of the CMOS circuits. Currently, there are three main approaches to the physical implementation of QCA: molecular QCA, magnetic QCA, and electronic QCA. The advancement of nanofabrication technology has enabled the production of quantum dots on the nanoscale, which can be used to manipulate electrons in a controlled manner. This allows for the physical realization of the QCA cells and their simple circuits, thus validating the correctness of the QCA theory. Currently, there are four physical implementation schemes for QCA: semiconductor material-based, tunneling junction formation using metal materials, molecular material-based, and magnetic material-based schemes. Each of these schemes is supported by a substantial amount of theoretical and experimental research. However, at the current research level, there are still some challenges that need to be addressed. For the purposes of this article, the physical implementation of the current technology needs to be further explored, which will also become our future goal. In turn, QCA technology has been truly applied.

To the best of our knowledge, there are currently four different QCA models. Nanomagnets-based fan-out lines, silicon-based QCA lines, and ferrocene molecules-based QCA lines have all been proven through experimentation [6,7]. Meanwhile, logic circuit blocks, such as full-adders, XOR gates, multipliers, as well as dividers have already been verified through pertinent simulations.

Previous studies have assessed the impacts of array multipliers. In 2004, Walus et al. proposed a novel bit-serial/parallel multiplier based on a bit-serial-adder [8]. One input of the multiplier is serially loaded into the adder, while the other input is effectively loaded in parallel. The multiplier calculates the partial product and adds it to the sum immediately. In 2007, Hanninen et al. proposed a novel QCA-based pipelined array multiplier [9]. This design used a reasonable clock allocation to operate reliably without suffering from the effects of noise coupling. The design of the multiplier unit is typically complex, resulting in a large overall cost. In 2010, Lu et al. designed and analyzed a QCA-based systolic matrix multiplier [10]. The 2×2 systolic matrix multiplier consisted of four processing elements (PEs), each of them including an advanced 2-bit serial-multiplier as well as a novel 4-bit accumulator. In 2016, Chudasama et al. used a carry save adder to construct a QCA-based 4×4 Vedic multiplier [11]. In 2018, Babaie et al. proposed an efficient multilayer arithmetic logic unit [12] and Torres et al. proposed a model to explore performance and energy of QCA [13]. In 2019, Bhoi et al. proposed a novel, accurate method to synthesizing while also optimizing the Baugh–Wooley-multiplier [14]. In 2019, Yang et al. proposed a 2×2 array multiplier circuit, which uses an efficient full adder structure. Meanwhile, Bahar et al. proposed a serial Parallel Multiplier [15]. In 2020, Chu et al. proposed BCD adder with xor gates and majority gates [16] and other researches proposed Decimal full adders with different devices [17–19]. In 2021, Perri et al. proposed low-energy multi-bit approximate adders [20] and Khanet al. proposed efficient vedic square calculator [21]. The designs provided ideas for us to design multipliers. Dividers constructed using unit structures have also been proposed, including non-restoring dividers [22–27] and restoring dividers [28].

Currently, state-of-the-art works include many modules in traditional digital circuits, such as adders [29], multipliers [30,31], dividers [32,33] etc. In 2022, K Raja Sekar et al. proposed an array multiplier with a relatively high latency, and also proposed a high-speed serial–parallel multiplier. This is an efficient hardware circuit that has been used across different applications ranging from simple arithmetic circuits, to filters, and complex cryptographic systems. However, it uses a lot of cells and has a large area. In addition, a variety of QCA circuits have been proposed, such as: full adders [34,35], memory cell [36–38], multi-bit full comparator [39] and other circuits [40–45]. Sequential logic elements have also been implemented in these QCA circuits. In large-scale circuits, there are also programmable logic arrays and field-programable gate array circuits based on QCA technology. Indeed, QCA also has its unique research areas, such as clock schemes, logic synthesis, and layout algorithms. From the current level of research, there are still areas where QCA

circuits need to be improved, but these unique properties of QCAs are still considered by researchers to implement one of the most promising new nano-devices.

Considering the above existing problems, in this paper, we presented a novel QCA-based array multiplier. The proposed array multiplier was effectively simulated and verified through the QCADesigner tool [46]. Compared with existing designs, the proposed novel designs have the smallest delay, cell count, and area. Moreover, we analyzed the complexity of the n*n design and made a theoretical comparison between the amount of employed QCA-based devices and their delay costs. We found that when the design scaling was increased, the proposed schemes demonstrated an excellent circuit performance.

The organization of the rest of this paper is as follows. In Section 2, the preliminaries of the QCA technology were introduced. In Section 3, the proposed array multipliers were described. In Section 4, the simulation results and comparisons were presented. In Section 5, the conclusions were outlined.

2. Preliminaries

Figure 1 presents the structure as well as two types of QCA cells. Figure 1a presents the structure of the standard four quantum-dot QCA cell. As shown in Figure 1a, there is a tunnel junction present between each quantum-dot, and there exists two additional free-electrons in each QCA cell. Two free electrons can effectively tunnel between these quantum-dots through the tunnel junctions. Due to the coulomb repulsion between these electrons, when the cell is in a stable state, the electrons always occupy the diagonal position, meaning that the cell exhibits double-stable polarization states that can be effectively used to represent the binary data. Figure 1b shows two important types of QCA cells, i.e., the normal cells as well as the rotated cells.

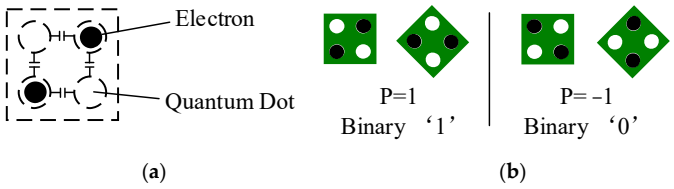

Figure 1. Structure and types of QCA. (**a**) Structure and (**b**) two types of QCA cells.

QCA encompasses a unique clock mechanism. A QCA clock can control the direction of information transmission and provide the energy of the QCA circuit. Figure 2 presents a QCA clock, which consists of four phases: switch, hold, release, and relax. In the switch phase, the cell will be polarized by the adjacent cells in the hold phase; in the hold phase, the polarization of the cell remains unchanged, and in the switch phase it can polarize the adjacent cells. The polarization of the cell gradually decreases in the release phase; the cell is in a non-polarization state in the relax phase [4].

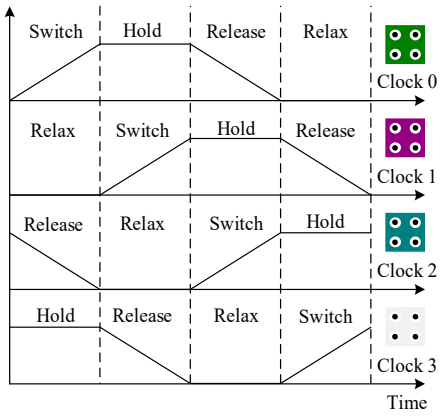

Figure 2. The QCA clock.

Figure 3 displays several QCA basic gates. Figure 3a shows an inverter, which can flip its input signal. Meanwhile, Figure 3b presents a novel majority gate, which can realize the function of Formula (1). The function of an AND gate or an OR gate can be realized through fixing an input of the majority gate as either 1 or 0 as M(A, B, 1) = A + B and M(A, B, 0) = AB, respectively. Figure 3c shows a 3-input XOR gate, which can implement the function of Formula (2). The 3-input XOR gate can realize the function of a 2-input XOR or XNOR gate by fixing one input as 1 or 0 as $X(A, B, 0) = A \oplus B$ and $X(A, B, 1) = \overline{A \oplus B}$, respectively.

$$M(A, B, C) = AB + AC + BC \tag{1}$$

$$X(A, B, C) = A \bigoplus B \bigoplus C \tag{2}$$

$$\begin{aligned} M(A, B, C, D, E) = {} & ABC + ABD + ABE + ACD + ACE \\ & + ADE + BCD + BCE + BDE + CDE \end{aligned} \tag{3}$$

$$MUX(A, B, Sel) = \overline{Sel}A + SelB \tag{4}$$

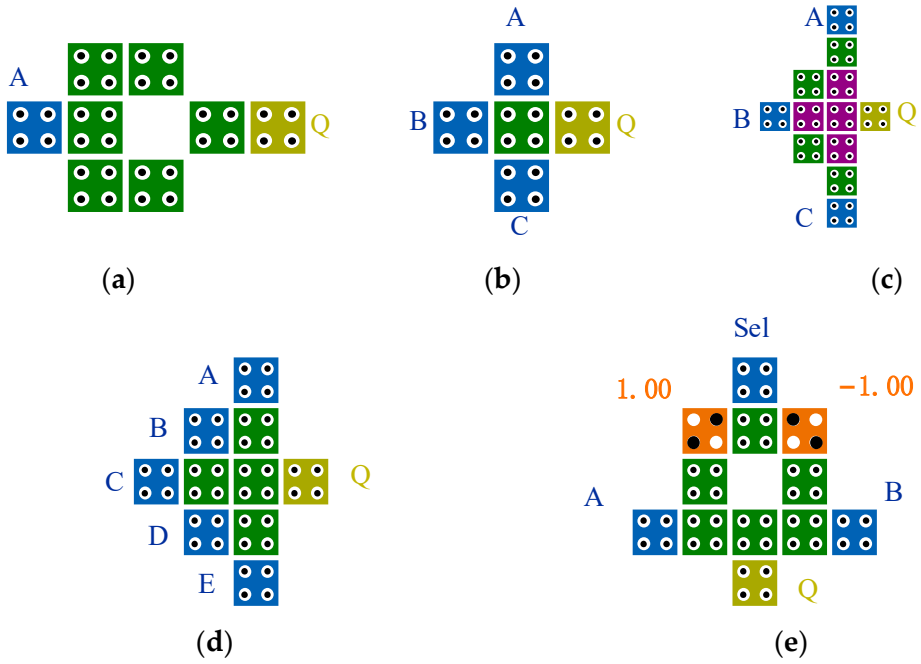

Figure 3. QCA-based basic gates. (**a**) Inverter. (**b**) Three-input majority gate. (**c**) Three-input XOR gate. (**d**) Five-input majority gate. (**e**) Two-to-one multiplexer designed by the authors of [47].

Figure 3d displays a 5-input majority gate. Formula (3) shows the boolean expression of the 5-input majority gates. By setting two inputs of the 5-input majority gate to either 0 or 1, the functions of the AND gate and OR gate can be realized, respectively. Figure 3e shows a two-to-one multiplexer that was put forward by the authors of [47]. Formula (4) shows the boolean expression of the two-to-one multiplexer. The multiplexer can output either signal A or signal B depending on the signal (Sel) of the two-to-one multiplexer. In Figure 3, the blue cells are the input cells and the yellow cells is the output cells.

Crossovers can cross two signals, which are widely used in QCA circuits. Figure 4 shows two crossovers. Figure 4a shows the multi-layer crossover. A multi-layer crossover requires at least three layers to cross signals. Figure 4b shows a coplanar crossover implemented using rotated cells. The two signals can correctly flow through the coplanar crossover. Due to the orthogonal electron configuration of these cells, the coulomb force between the cells can not interfere with their neighboring cells.

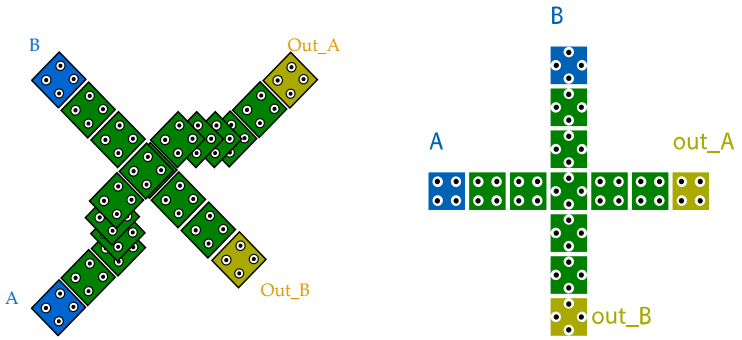

Figure 4. Crossovers. (**a**) Multi-layer crossover. (**b**) Coplanar crossover implemented by the rotating QCA cells.

3. Proposed Array Multipliers

3.1. Full Adder

Figure 5 presents the structure of a QCA-based full adder (FA) [48]. We can see from Figure 5 how the structure of the FA only requires one 3-input majority gate as well as one 3-input XOR gate. A is the augend, B is the addend, C_i is the low carry input, C_{i+1} is the high carry output, and S represents the sum, respectively. Formulas (5) and (6) display the boolean functions of the FA.

$$S = A \bigoplus B \bigoplus C_i = X(A, B, C_i) \tag{5}$$

$$C_{i+1} = M(A, B, C_{i+1}) \tag{6}$$

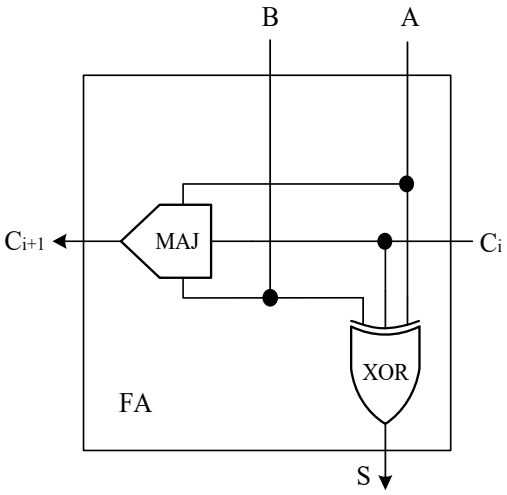

Figure 5. Schematic of the QCA-based FA outlined by the authors of [48].

3.2. Array Multiplier

Figure 6 shows the schematic of the multiplier unit [9]. The basic unit of the array multiplier consists of an AND gate and a FA. The array multiplier can be built with multiplier units. Figure 7 shows the schematic of the array multiplier [9]. X1/X2/X3/X4 is the multiplicand, Y1/Y2/Y3/Y4 is the multiplier, and m1/m2/m3/m4/m5/m6/m7/m8 is the product, respectively. Each row of the array multiplier is built with ripple carry adders (RCAs). The array multiplier needs to check the bits of the multiplier one at a time and produces the next partial product. A sequence of add and shift micro-operations are required to obtain the final results. Each bit of the multiplier and each bit of the multiplicand

are ANDed together. The binary output of each AND gate and the partial product in the previous level are then added in parallel to produce a new partial product, and the last level of the array multiplier produces the final product. Although the array multiplier requires many gate devices, its internal structure is regular and highly standardized, making it suitable for the implementation of the VLSI circuits.

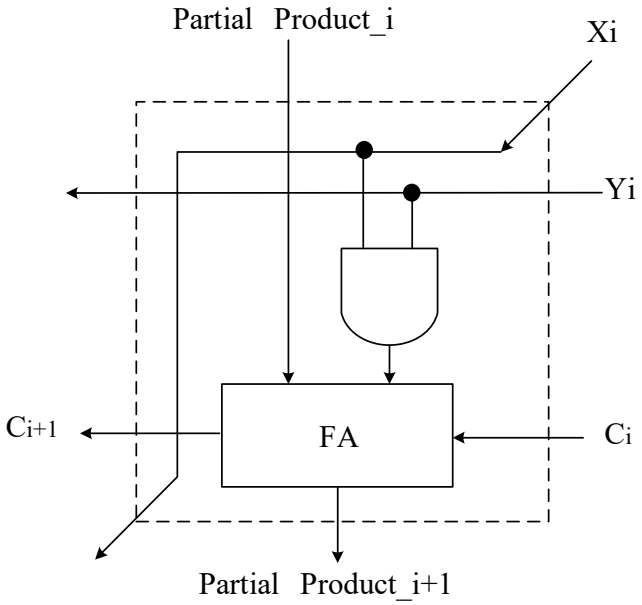

Figure 6. Schematic of the multiplier unit outlined by the authors of [9].

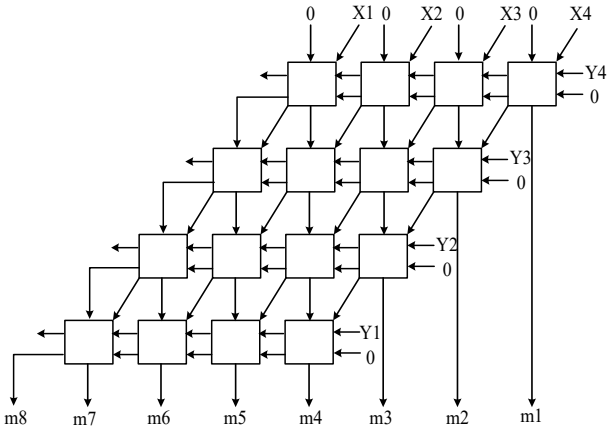

Figure 7. Schematic of the array multiplier outlined by the authors of [9].

Figure 8 shows the proposed QCA-based 2 × 2 array multiplier. The FA implemented by the authors of [29] was used to design the array multiplier. The multiplier unit is constructed with a FA and an AND gate. The proposed 2 × 2 array multiplier comprises 439 cells, having an area of 0.49 μm^2, as well as a delay of 1.75 clock-cycles. X1/X2 is the multiplicand, Y1/Y2 is the multiplier, and M1/M2/M3/M4 denotes the product, respectively. Figure 9 shows the proposed QCA-based 3 × 3 array multiplier, which consists of a three-layer design. The proposed 3 × 3 array multiplier comprises 1041 cells, having an area of 1.26 μm^2 and a delay of 2.50 clock-cycles. X1/X2/X3 is the multiplicand, Y1/Y2/Y3 is the multiplier, and M1/M2/M3/M4/M5/M6 represents the product, respectively. The used RCAs in each row of the proposed array multiplier adopt compact clock allocation in order to minimize carry delay. The array multiplier can output the calculation results after 2.50 clock cycles.

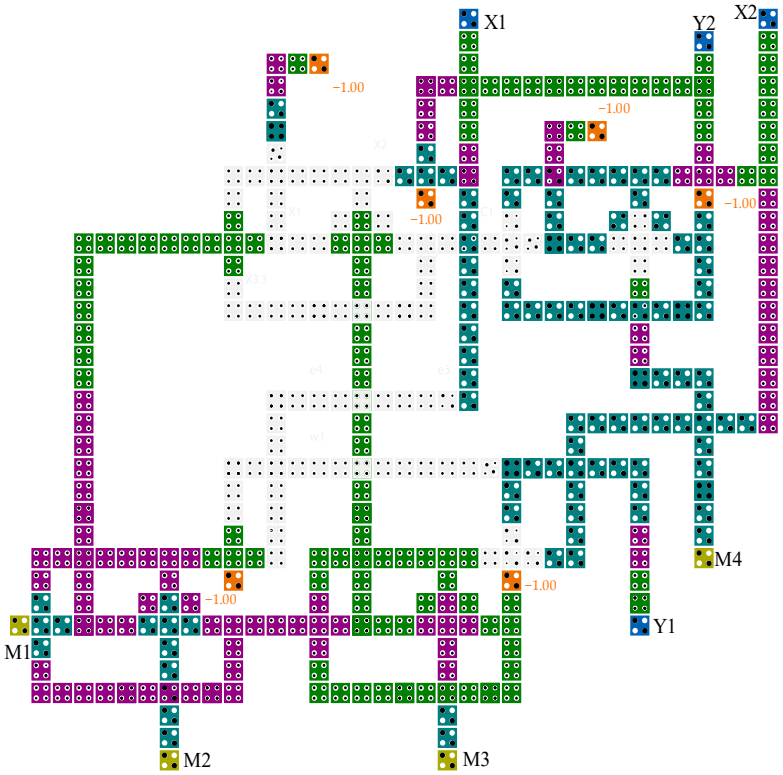

Figure 8. The proposed QCA-based 2 × 2 array multiplier.

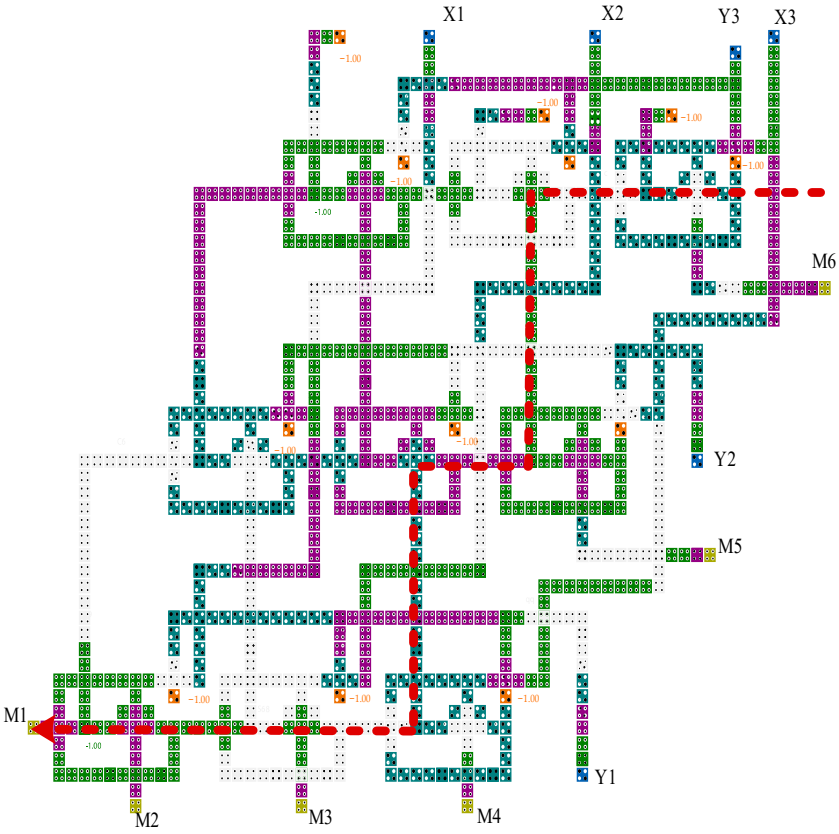

Figure 9. The proposed QCA-based 3 × 3 array multiplier.

4. Simulations and Comparisons

4.1. Simulations

We simulated and verified the proposed designs with the QCADesigner tool. The simulation process requires two multipliers, which are placed in the X and Y inputs, respectively, while the product displays the output. Figure 10 presents the results of the simulations that were performed using the proposed QCA-based 2 × 2 array multiplier, and also displays the results of the six consecutive pairs of multipliers that were used. X was set to {0, 1, 3, 2, 3, 2}, and Y was set to {3, 3, 2, 1, 3, 2}, respectively. The product was {7, 20, 10, 8, 14, 28} following calculations. The calculation process of the proposed array multiplier required 1.75 clock cycles. Since there are four clock zones in a clock cycle and the clock regions are numbered from 0, the product is displayed in clock 2 as a result. For example, when the first pair has a multiplier of 0 and the other has a multiplier of 3, the correct result of the multiplier of that pair appears after 1.75 clock cycles. Figure 11 presents the results of the simulations that were performed for the proposed QCA-based 3 × 3 array multiplier. Similarly, we set X and Y to the two multipliers, and the product to the output. X was set to {7, 5, 5, 4, 7, 7}, and Y was set to {1, 4, 2, 2, 2, 4}, respectively. The product was {7, 20, 10, 8, 14, 28} after calculations. The calculation process of the proposed array multiplier required 2.50 clock cycles. For example, when one multiplier is 1 and the other is 7, the product is calculated 7 after 2.5 clock cycles. In this context, this result was deemed to be correct.

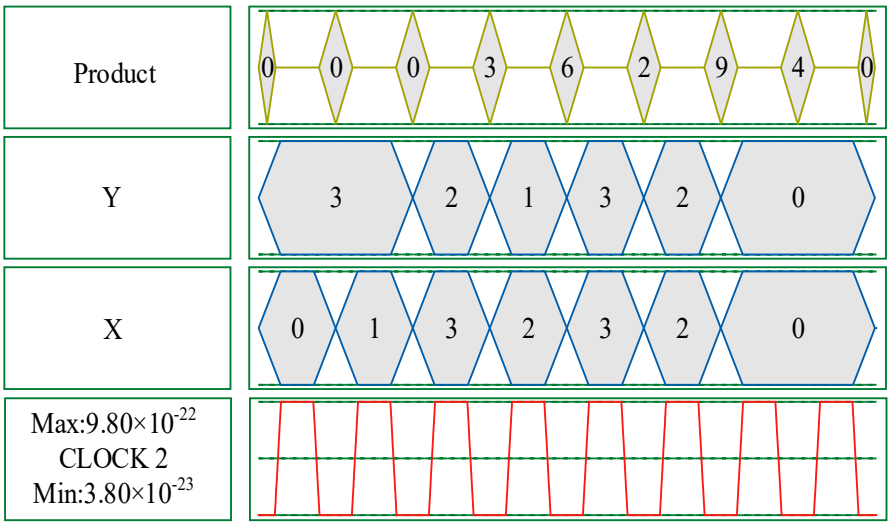

Figure 10. Results of the simulations for the proposed QCA-based 2 × 2 array multiplier.

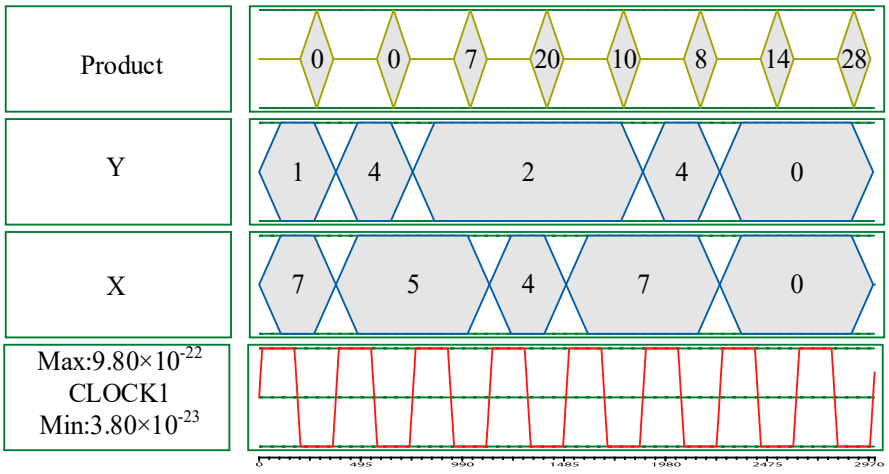

Figure 11. Results of the simulations for the proposed QCA-based 3 × 3 array multiplier.

4.2. Comparisons

Table 1 presents the results of the comparisons between the alternative multipliers. As multiplication does not require the judging of the most significant bit of each row, unlike division, but only requires the shift and add micro-operations, the delay of the array multipliers increases slowly with the increase in the design scaling. Compared with the work published by the authors of [49], the proposed array multiplier reduced the cell count, area, and delay by 10.95%, 31.94%, and 65.00%, respectively.

Table 1. Results of the comparisons for the alternative multipliers.

Design	Cell Count	Area (μm^2)	Delay	Layer Type
2 × 2 matrix multiplier [10]	7102	15.69	20	M
2-bit-serial multiplier [8]	306	0.48	8	C
2-bit multiplier [9]	1598	1.76	7	C
2 × 2 Baugh–Wooley multiplier [14]	688	0.91	3	M
2 × 2 array multiplier [49]	493	0.72	5.00	C
Pro 2 × 2 array multiplier	439	0.49	1.75	M
Pro 3 × 3 array multiplier	1041	1.26	2.50	M

Table 2 presents the results of the comparisons of energy consumption for the proposed designs. The energy consumption of the proposed designs under different temperatures was measured using the QCA-Designer-E tool [13], and other parameters present in the QCA-Designer-E tool were set as the default values. As clearly shown in Table 2, the energy consumption of the proposed array multiplier was deemed to be lower compared to the solution outlined by the authors of [49].

Table 2. Results of the comparisons of energy consumption for the proposed designs.

Design	Total Energy Dissipation (eV)	Average Energy Dissipation (eV)	Total Energy Dissipation (eV)	Average Energy Dissipation (eV)
	Temperature 1K		Temperature 2K	
MUL 2 × 2 [49]	1.78×10^{-1}	1.62×10^{-2}	1.83×10^{-1}	1.66×10^{-2}
Pro-MUL 2 × 2	1.56×10^{-1}	1.42×10^{-2}	1.54×10^{-1}	1.40×10^{-2}
Pro-MUL 3 × 3	3.79×10^{-1}	3.44×10^{-2}	3.76×10^{-1}	3.41 × 10-2

4.3. Complexity Analysis

The proposed designs were all constructed using separate QCA devices, such as 3-input majority gates, inverters, and 3-input XOR gates. The total amount of used QCA devices can be employed to effectively measure the area cost of n × n designs. An n × n multiplier requires 2n2 MGs and n2 XOR gates, and thus form a total of 3n2 QCA devices.

Formula (7) displays the theoretical delay of the n × n multiplier. Formula (5) can be obtained through analyzing the delay of the red path displayed in Figure 9. D_{n_MUL} represents the delay of the n*n multiplier and DMUL denotes the delay of the multiplier unit, respectively. It is clearly shown that when the design scaling is increased, the delay from the input to the output of the proposed multiplier also increased linearly.

$$D_{n\_MUL} = (3n - 2) \cdot D_{MU} \quad (7)$$

5. Conclusions

In this paper, we have proposed a new QCA-based 2 × 2 array multiplier, and based on this structure, a higher-digit 3 × 3 array multiplier has also been proposed. The improved clocking scheme reduces the carry delay, and the clock delay of the 2 × 2 array multiplier is reduced by almost 65% compared to the existing designs. Furthermore, the number of cells and the area has also been optimized, resulting in a faster circuit calculation. It is

beneficial to apply the proposed multiplier to a wider range of arithmetic logic units or communication system units. Moreover, according to our proposed design summary, as a complexity analysis method has been obtained, this can prove the rationality of the n*n design that we proposed and permit calculations of the theoretical delay of the multiplier. In conclusion, the proposed array multiplier exhibits significant advantages in terms of the delay, cell counts, and area. Moreover, previous research has indicated that fault tolerance is also an important issue which remains to be considered [50,51]. Going forward, we will consider this issue and provide the simulation results.

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