Two Double-Node-Upset-Hardened Flip-Flop Designs for High-Performance Applications

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Abstract—The continuous advancement of complementary metal-oxide-semiconductor technologies makes flip-flops (FFs) vulnerable to soft errors. Single-node upsets (SNUs), as well as double-node upsets (DNUs), are typical soft errors. This paper proposes two radiation-hardened FF designs, namely DNU-tolerant FF (DUT-FF) and DNU-recoverable FF (DUR-FF). First, the DUT-FF which mainly consists of four dual-interlocked-storage-cells (DICEs) and three 2-input C-elements, is proposed. Then, to provide complete self-recovery from DNUs, the DUR-FF which mainly uses six interlocked DICEs is proposed. They have the following advantages: (1) They can completely protect against SNUs as well as DNUs; (2) the DUT-FF is cost-effective but the DUR-FF can provide complete self-recovery from any DNU. Simulations show the complete SNU/DNU tolerance of DUT-FF and the complete SNU/DNU self-recovery of DUR-FF but at the cost of indispensable area overhead when compared to the SNU hardened FFs. Besides, compared to the FFs of the same-type, the proposed FFs achieve a low delay making them suitable for high-performance applications.

Index Terms—Radiation hardening, flip-flop, soft error, single-node-upset, double-node-upset

1 Introduction

With *complementary metal-oxide-semiconductor* (*CMOS*) technology scaling, the reduction of currents and node capacitances leads to an increase of circuit vulnerability to soft errors [1]. Soft errors are transient errors that can upset values kept in storage cells such as *flip-flops* (*FFs*) as well as *static random access memories* (*SRAMs*). In space environments, the strike of ionizing particles (alpha particles, heavy ions, etc.) can easily cause soft errors in storage elements designed without radiation-hardening [1-2]. When a particle hits the sensitive part of a CMOS circuit, it causes a voltage pulse at the output of a logical gate, known as a *single event transient* (*SET*) [3]. If the particle hits a storage cell, it can cause a *single-node upset* (*SNU*). Furthermore, the closeness of transistors can induce charge sharing so that one particle can impact double nodes inside a storage cell simultaneously, leading to a *double-node upset* (*DNU*) [4]. Due to the drastically increased sensitivity to SET, SNU, and DNU of modern devices, the use of *radiation-hardening-by-design* (*RHBD*) approaches for providing system robustness against transient errors has taken growing importance.

Hardening against SNUs and DNUs instead of SETs is considered in this paper (SET hardening can usually lead to large delay cost). Using RHBD, a series of structures, such as latches [5-8], SRAMs [9-12], and FFs [13-20], were proposed. Note that, many important works, such as those in [14-22], will be further evaluated and/or compared in the subsequent sections. The related works, such as those in [23-27], will be briefly commented in this section. Among them, *dual-interlocked-storage-cells* (*DICEs*) are used as an important component [28]. Figure 1 presents two types of DICE cells that have two key features: (1) it provides complete SNU self-recovery; (2) it only provides partial DNU self-recovery, and thus it cannot self-recover from some DNUs. Besides DICE, *C-elements* (*CEs*) are also widely used. Figure 2 shows four types of CEs. For example, the 2-input CE in Fig. 2-(a) acts as an inverter when the value of all inputs is the same. However, if the inputs change to have different values, its output can temporarily retain its original value due to capacitances. Note that the *clock-gating* (*CG*) based CEs can also be controlled by the *negative system clock* (*NCK*) and *system clock* (*CLK*). Therefore, the CG-based DICEs can also be constructed easily.

This paper focuses on the hardening of FFs that are mainly constructed from DICEs and CEs. The *typical unhardened FF* (*TUFF*) consists of a master *typical unhardened latch* (*TUL*) as well as a slave TUL [13]. Note that the TUL and TUFF cannot tolerate SNUs. For this reason, many SNU-hardened FFs such as those in [14-16,

- *Aibin Yan is with the School of Microelectronics, Hefei University of Technology and also with the School of Computer Science and Technology, Anhui University, Hefei 230601, China. (E-mail: abyan@mail.ustc.edu.cn).*
- *Aoran Cao and Jie Cui are with the School of Computer Science and Technology, Anhui University, Hefei 230601. (E-mail: arcao_ahu@163.com, cuijie}@mail.ustc.edu.cn).*
- *Zhengfeng Huang is with the School of Microelectronics, Hefei University of Technology, Hefei 230601, China. (E-mail: huangzhengfeng@139.com).*
- *Tianming Ni is with the School of Integrated Circuits, Anhui Polytechnic University, Wuhu 241000, China. (E-mail: timmyni126@126.com).*
- *Patrick Girard is with the LIRMM, University of Montpellier / CNRS, Montpellier 34095, France (E-mail: girard@lirmm.fr).*
- *Xiaoqing Wen is with the Graduate School of Computer Science and Systems Engineering, Kyushu Institute of Technology, Fukuoka 820-8502, Japan (E-mail: wen@cse.kyutech.ac.jp).*
- *Jiliang Zhang is with the College of Semiconductors (College of Integrated Circuits), Hunan University, Changsha 410082, China. (E-mail: zhangjiliang@hnu.edu.cn).*

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18-20, 26-27] were proposed. Moreover, to improve reliability, many DNU-hardened solutions such as those in [17, 21-25] were proposed. However, these FFs have the following existing problems that need to be solved.

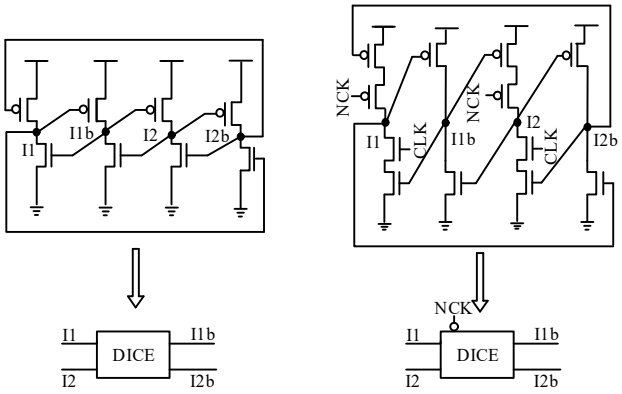

Fig. 1. Two types of Dual-interlocked storage-cells (DICEs) [28]. (a) DICE cell. (b) Clock-gating-based DICE cell.

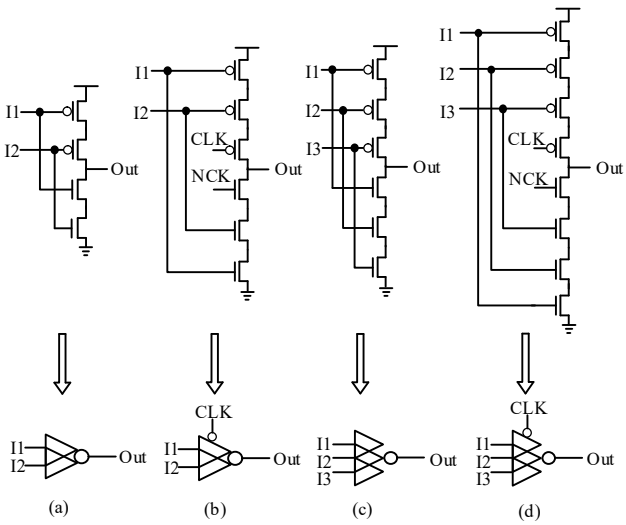

Fig. 2. Four types of C-elements. (a) 2-input C-element. (b) Clock gating based 2-input C-element. (c) 3-input C-element. (d) Clock-gating based 3-input C-element.

(1) Most FFs are not completely DNU-hardened [14-20, 23, 27, 29].

(2) Most FFs cannot provide complete SNU/DNU-recovery [14-21, 23-29] so that errors can be accumulated seriously impacting the reliability of circuits. Although DICE latches prevent DNUs by placing pairs of critical nodes far apart as in [30], the solution can increase the layout complexity for design.

(3) Most of them have to pay for large costs, especially in terms of transmission delay.

The contribution of this paper is summarized as follows. Firstly, to ensure low overhead, especially in terms of transmission delay, the DUT-FF with complete DNU-tolerance is proposed. Secondly, to provide complete SNU/DNU self-recovery, the DUR-FF with reasonable overhead, especially in terms of silicon area, is proposed. Moreover, p*rocess, voltage, and temperature* (*PVT*) analysis for the proposed FFs as well as the state-of-the-art FFs are performed and compared.

The rest of this paper is organized as follows. Section 2 reviews existing FF designs. Section 3 introduces the proposed DUT-FF. Section 4 presents the proposed DUR-FF. Section 5 provides comparisons and evaluations for the alternative FFs. Section 6 concludes this paper.

2 Previous Flip-Flop Designs

Figure 3 presents the structures of typical hardened FF designs. Note that, in Fig. 3, D is the input, Q is the output, and the switches are *transmission gates* (*TGs*). As for clock connections of TGs, for example, each TG marked with NCK indicates that the gate terminal of the PMOS and NMOS is linked to NCK and CLK, respectively. The above rules are applicable to all FFs in this paper. The *Static Single-Phased Contention-Free Flip-Flop* (*S2C-FF*) [14] is shown in Fig. 3-(a). It is not SNU/DNU tolerant due to its simple structure. The *Triple-Modular-Redundancy Flip-Flop* (*TMR-FF*) in Fig. 3-(b) comprises three TUFFs and a voter. The voter is used at the output of three copies of the TUFFs so that when one of the modules suffers from an SNU, the output of the FF is still correct. The *High-Performance SNU Tolerant Flip-Flop* (*HPST-FF*) [15] in Fig. 3-(c) uses four loops connected to two CG-based 2-input CEs providing SNU tolerance. Nevertheless, the FF has at least one counter-example that it cannot tolerate a DNU. The *SEU-Resilient Non-Volatile Flip-Flop* (*SEUR-NVFF*) [16] in Fig. 3-(d) mainly employs two 2-input CEs and two traditional latches connected to two CG-based 2-input CEs providing SNU tolerance. Nevertheless, the SEUR-NVFF cannot effectively tolerate DNUs as the HPST-FF.

The *DNU-Resilient Flip-Flop* (*DNUR-FF*) [17] in Fig. 3-(e) comprises four 2-input CEs and two traditional latches connected to two CG-based 3-input CEs to tolerate only a part of DNUs. Therefore, it is not completely DNU-hardened. Moreover, the delay of the DNUR-FF is large. The *Dual Redundancy Radiation-Hardened Flip-Flop* (*DRRH-FF*) [18] and the Quatro-FF [19] are shown in Fig. 3-(f) and (g), respectively. They are hardened against any SNU, but they cannot effectively tolerate DNUs. The *Dual-Interlocked storage-CEll Flip-Flop* (*DICE-FF*) [20] in Fig. 3-(h) comprises two DICEs to provide self-recoverability against any SNU. However, the DICE-FF is not completely DNU-hardened. Note that, the SEDU-FF [27] is hardened against any SNU, but it cannot completely tolerate DNUs. Similarly, the FF in [31] also suffers from the same problem.

The above-mentioned problems motivate us to propose a novel DUT-FF and its advanced version, namely DUR-FF, effectively protected against DNUs in this paper. Note that, compared to the preliminary conference version of the paper in [29], our key enhancements exclusive to this journal manuscript are the following: (1) we investigated SNU and DNU hardened FFs and added the review about them; (2) we found that the proposed DURI-FF in [29] cannot provide complete DNU-recovery, especially for the floated inputs of inverters so that a completely DNU-recoverable DUR-FF is proposed; (3) we found that, to provide complete DNU self-recovery for the DUR-FF, the

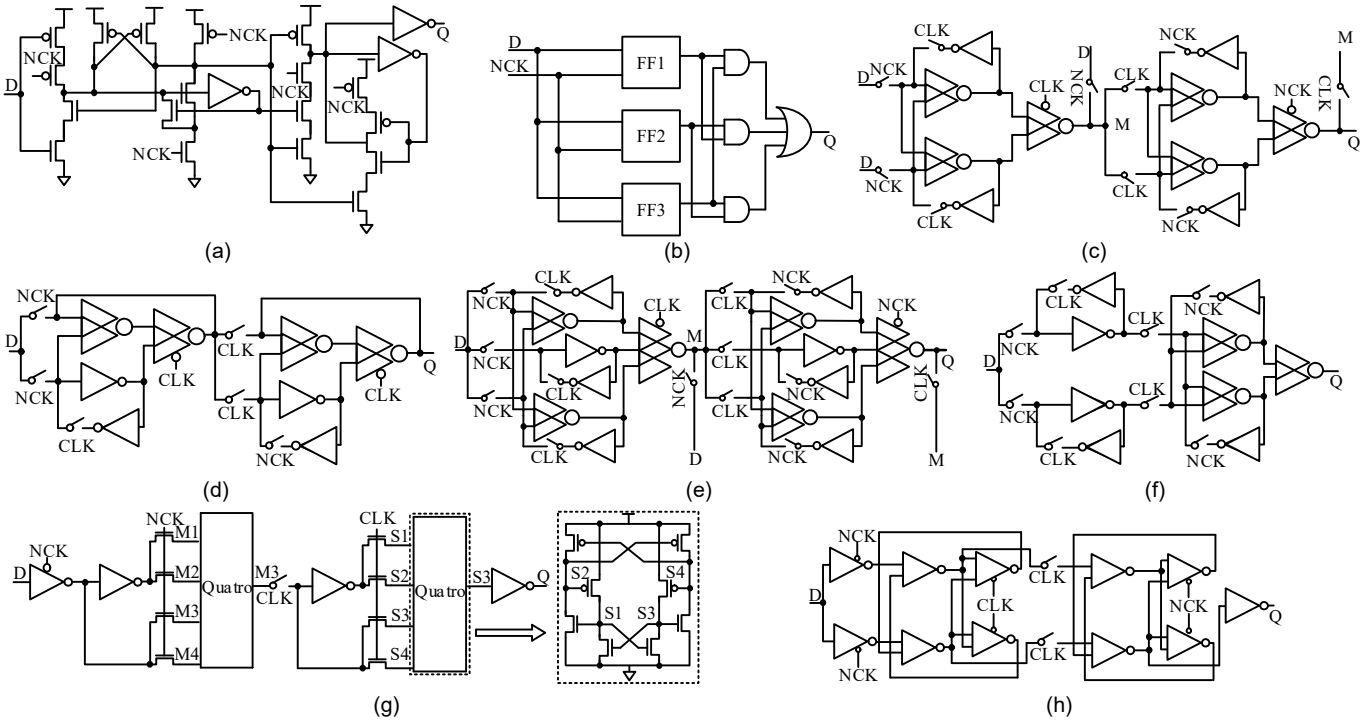

Fig. 3. Schematics of representative unhardened and hardened FF designs. (a) S2C-FF [14], (b) TMR-FF, (c) HPST-FF [15], (d) SEUR-NVFF [16], (e) DNUR-FF [17], (f) DRRH-FF [18], (g) Quatro-FF [19], and (h) DICE-FF [20].

extra overhead in terms of power and area has to be introduced. We consider that trading off overhead and reliability is indispensable for providing fault-tolerant FFs and thus the DUT-FF is additionally proposed in this paper; (4) a comprehensive comparison and evaluation of many different FFs has been performed and is presented in Section 5; and (5) the process, voltage, and temperature variations are also investigated and reported for all alternative FFs.

3 Proposed DUT-FF Cell

3.1 Structure and Simulations

The schematic of the proposed DUT-FF design is presented in Fig. 4. The FF mainly comprises two normal DICEs (i.e., DICE1 as well as DICE2), two normal 2-input CEs (i.e., CE1 as well as CE2), two CG-based DICEs (i.e., DICE3 and DICE4), and a CG-based 2-input CE (i.e., CE3). Note that two TGs are added into the FF to transfer values to nodes M2 and Q during the transparent mode of operation, hence reducing propagation delay (CLK-to-Q). The working operations of the DUT-FF are discussed below.

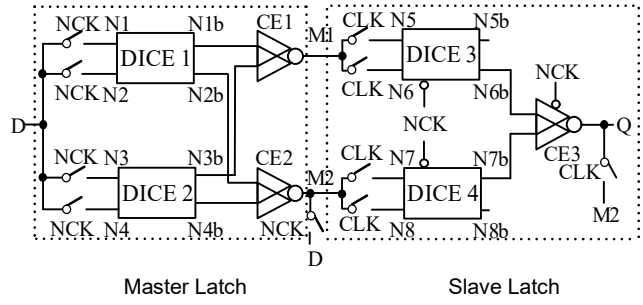

Fig. 4. Schematic of the proposed DUT-FF.

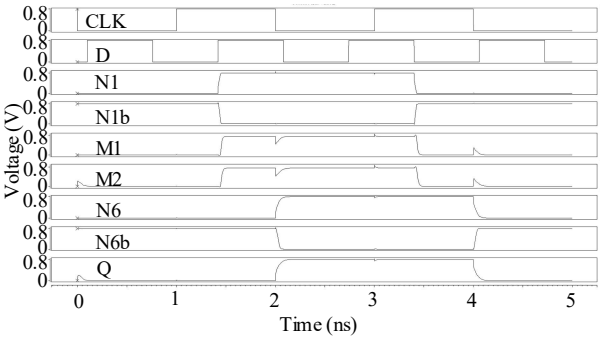

Fig. 5. Simulation results for normal operations of the proposed DUT-FF.

First, CLK is set to high and meanwhile, NCK is set to low. The master latch enters in the transparent mode of operation. Thus, the value at the input is transferred to node M2 through a TG (i.e., a switch marked with NCK at the output of CE2) and stored into the DICEs (i.e., DICE1 and DICE2), so that the master latch is initialized. However, the slave latch has currently no values.

(1) Next, CLK becomes low and NCK becomes high. The master latch enters into hold mode, thus storing the D-value. At this time, the slave latch works in transparent mode so that all TGs in the slave latch become ON. Hence, the slave latch outputs the D-value received from the master latch.

(2) Subsequently, CLK becomes high and NCK becomes low. The master latch receives the new D-value (N1 = N2 = N3 = N4 = D) and thus the slave latch can store/output the old D-value in step (2).

(3) Eventually, CLK becomes low and NCK becomes high. At this time, the master latch can retain the new D-value in step (3) but the slave latch can output this D-

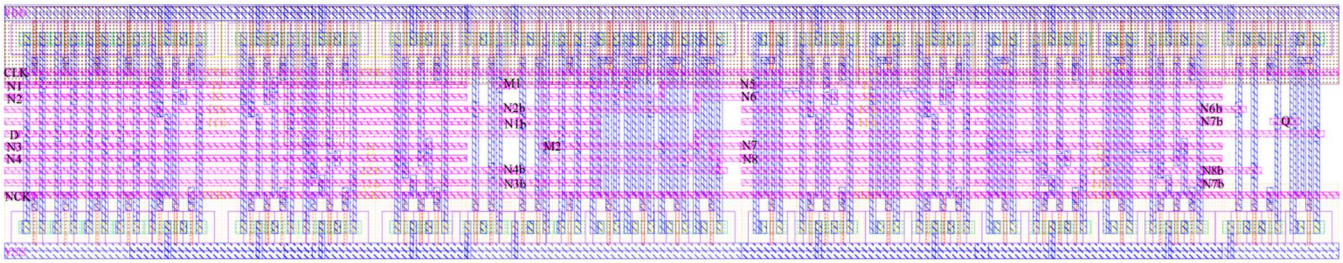

Fig. 6. Layout of the proposed DUT-FF design.

value received from the master latch.

Figure 5 presents the simulation waveforms of the normal operations of the DUT-FF. Note that, we used the Synopsys HSPICE tool with 22nm CMOS library from GlobalFoundries to perform all simulations in this paper. The supply voltage is 0.8V and the working temperature is the room temperature. In the DUT-FF, the PMOS transistors had the ratio W/L = 90nm/22nm, and the NMOS transistors had the ratio W/L = 45nm/22nm. Fig. 5 is discussed as below.

(1) Firstly, CLK is high, D = N1 = N2 = N3 = N4 = M2 and all node values in the master latch can be determined.

(2) Secondly, CLK becomes 0, the master latch can retain the D-value (i.e., 0) but the slave latch can output the retained D-value received from the master latch.

(3) Thirdly, when CLK becomes 1 at 1ns, the master latch can receive the new D-value until the FF enters the state in step (4), and at this time, the slave latch can store/output the original D-value (i.e., 0).

(4) Finally, when CLK becomes 0 at 2 ns, the master latch can store the final new D-value (i.e., 1) in step (3) but the slave latch can output this D-value received from the master latch. Therefore, the Q-value can be switched to the D-value only at the falling edge of the CLK signal. Simulation results in Fig. 5 demonstrate the correct functioning of the DUT-FF in normal mode. The layout of the proposed DUT-FF design is presented in Fig. 6.

3.2 SNU/DNU Tolerance and Verifications

Let us now discuss the SNU/DNU tolerance principles. Generally, only the principles for hold mode need to be analyzed. As for SNU tolerance, in the case where a representative single node inside the master latch (i.e., N1, N1b, or M1) is affected by an SNU, the master latch can provide recovery from the SNU since any DICE can self-recover from any possible SNU. Note that when M1 suffers from an SNU, it can self-recover by correct DICEs (i.e., DICE1 and DICE2) through CE1. On the other hand, a representative single node inside the slave latch (i.e., N6, N6b, or Q) can also be affected by an SNU and the slave latch can self-recover from the SNU since any DICE can provide complete SNU-recovery. As for Q, when it suffers from an SNU, it can self-recover by correct DICEs (i.e., DICE3 and DICE4) through CE3, so that Q can recover. In summary, the proposed FF is completely SNU-tolerant and even SNU-recoverable.

Let us now consider DNUs. Firstly, we consider that any node pair inside the master latch is affected by a DNU.

Case 1: Two nodes of a DICE inside the master latch are impacted by a DNU. All DICEs are equivalent for fault-tolerance, and thus we only take DICE1 as an example to consider possible node-pairs. The representative node-pairs are <N1, N1b>, <N1b, N2b>, and <N1, N2>. Note that, when <N1, N1b> suffers from a DNU, it can self-recover from the DNU when N1 = 1 (at this time, the DUT- FF can recover from the DNU). Nevertheless, it cannot recover when N1 = 0 [28]. In the case where N1 = 0, DICE2 is not affected. Thus, both CE1 and CE2 have correct single inputs, so that CE1 and CE2 can block this error and the CEs can still output their former correct values. Moreover, as for <N1b, N2b> and <N1, N2>, a similar scenario can be observed. Therefore, the FF can completely tolerate this type of DNUs.

Case 2: Two single nodes from two DICEs inside the master latch are impacted by a DNU. The representative DNU-node pairs are <N1, N3>, <N1, N3b>, and <N1b, N3b>. As for <N1, N3>, when it suffers from a DNU, it can self-recover from the DNU since N1 and N3 are single nodes of DICE. As for <N1, N3b> and <N1b, N3b>, a similar scenario can be observed. Therefore, this type of DNUs can be effectively tolerated by the FF.

Case 3: One node of a DICE and an output node of the master latch are impacted by a DNU. The representative node-pair is <N1, M1> only. As for <N1, M1>, when it suffers from a DNU, N1 can firstly self-recover since it is a single node of DICE1 that can self-recover from SNUs. Hence, the inputs of CE1 are still correct, so that the error at M1 can be removed through CE1. Therefore, the FF can tolerate this kind of DNUs.

Case 4: All these output nodes (i.e., <M1, M2>) are affected by a DNU and there is only one node pair. M1 and M2 can recover from the DNU by DICE1 and DICE2 through CE1 and CE2, respectively. Therefore, the FF can tolerate this DNU.

The above discussions show that the master latch of the proposed DUT-FF is completely DNU-tolerant. In the following, we consider that any node pair inside the slave latch is affected by a DNU.

Case 5: Two nodes of a DICE inside the slave latch are impacted by a DNU. All DICEs are equivalent for fault-tolerance, and thus we only take DICE3 as an example to consider possible DNU node pairs. According to the DICE structure shown in Fig. 1, the representative DNU node-pairs in DICE3 only include <N5, N5b> (the same as <N6, N6b>) and <N5, N6> (the same as <N5b, N6b>). Note that, when <N5, N5b> suffers from a DNU, DICE3 can recover from the DNU if N5 = 1. At this time, the

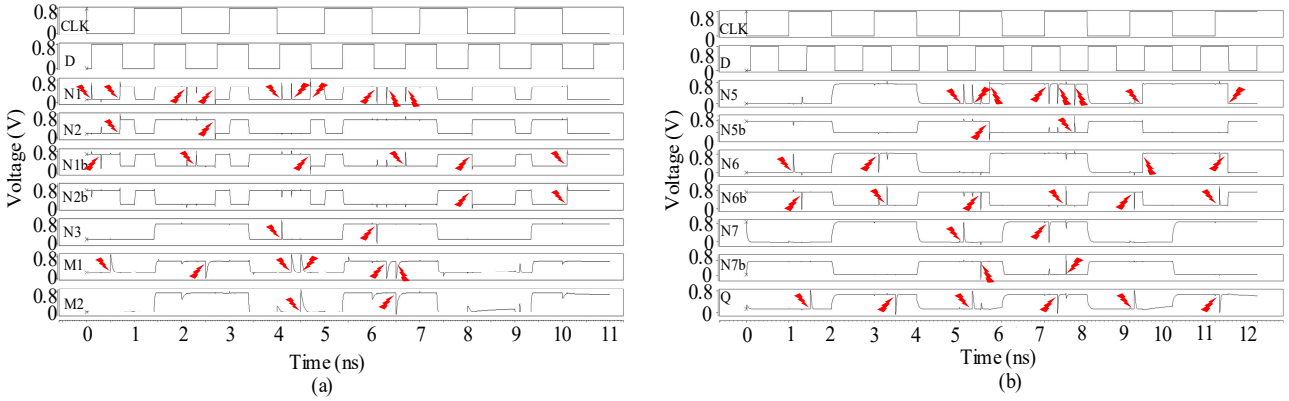

Fig. 7. Simulation results of all indicative SNU and DNU injections for the proposed DUT-FF, (a) Master Latch, (b) Slave Latch.

DUT- FF can recover from the DNU. Nevertheless, DICE3 cannot recover from the DNU if N5 = 0. At this time, DICE4 is not affected which means that CE3 has a correct single input, i.e., N7b, so that CE3 can block the error in DICE3 and the output of CE3 is still correct. Moreover, as for <N5, N6>, we can observe a similar scenario. Therefore, the proposed DUT-FF can completely tolerate this type of DNUs.

Case 6: Two single nodes from two DICEs inside the slave latch are impacted by a DNU. The representative DNU pairs include <N5, N7> and <N6b, N7b> only. As for <N5, N7>, when it suffers from a DNU, it can recover from the DNU since N5 and N7 are respectively single nodes of SNU-self-recoverable DICE3 and DICE4. As for <N6b, N7b>, a similar scenario can be observed. Therefore, the proposed DUT-FF can completely tolerate (and even recover from) this type of DNUs.

Case 7: One node of a DICE and the output node of the slave latch are impacted by a DNU. The representative DNU node-pairs include <N5, Q> and <N6b, Q> only. As for <N5, Q>, when it suffers from a DNU, N5 can firstly self-recover since it is a single node of DICE3 that can self-recover from SNUs. Hence, the inputs of CE3 are still correct, so the error at Q can be deleted through CE3. As for <N6b, Q>, a similar scenario can be observed. Therefore, the proposed DUT-FF can tolerate (and even recover from) this type of DNUs.

Figure 7 shows the simulation waveforms of all indicative SNU/DNU injections for the proposed DUT-FF. We can see from Fig. 7 that, when Q = 0, at 0.1ns, 0.3ns, 0.5ns, 0.7ns, 1.1ns, 1.3ns, 1.5ns, 4.1ns, 4.3ns, 4.5ns, 4.7ns, 5.1ns, 5.3ns, 5.5ns, 5.7ns, 8.1ns, 9.1ns and 9.3 ns, an SNU were respectively injected to single nodes N1, N1b, M1, N6, N6b, and Q. Meanwhile, a DNU was respectively injected to node-pairs <N1, N2>, <N1, N3>, <N1, M1>, <M1, M2>, <N1, N1b>, <N5, N7>, <N5, Q>, <N6b, N7b>, <N5, N5b>, <N1b, N2b>, <N6b, Q> and <N5, N6>. We can see from Fig. 7 that these single nodes, as well as node-pairs, can tolerate injected SNUs and DNUs, respectively. Moreover, when Q = 1, at 2.1ns, 2.3ns, 2.5ns, 2.7ns, 3.1ns, 3.3ns, 3.5ns, 6.1ns, 6.3ns, 6.5ns, 6.7ns, 7.1ns, 7.3ns, 7.5ns, 7.7ns, 10.1ns, 11.1ns, and 11.3ns, an SNU was also respectively injected to these single nodes. On the other hand, a DNU was injected into these node-pairs, respectively. We can see from Fig. 7 that these single nodes and DNU-node pairs can tolerate injected SNUs and DNUs, respectively. In summary, simulation results validate the ability of the proposed DUT-FF design to provide SNU and DNU tolerance.

Note that, we used the double-exponential current source model to perform all injections of SNUs/DNUs (see Eq. 1), where Qinj is the amount of injected charge, $\tau1$ is the collection time constant of the junction, and $\tau2$ is the time constant for the initial establishment of the ion track. In this work, Qinj was 25fC in the worst case for each node, which is large enough since our aim is to validate the circuit operation under extreme SNU and DNU conditions that disturb circuit nodes. $\tau1$ and $\tau2$ were set to 3.0 ps and 0.1ps, respectively. we choose the small rise time-period of injected errors so that the injected erroneous charge can have an immediate impact. The fall time-period is 30 times larger than the rise time-period so that 3.0 ps is sufficient enough for error injections. Note that, as in many papers [31-36], we used two simultaneous SNUs to mimic a DNU and the SNUs were injected with equivalent charge to share the charge of a DNU.

$$I(t) = \frac{Q_{inj}}{\tau1 - \tau2}\left(e^{-\frac{t}{\tau1}} - e^{-\frac{t}{\tau2}}\right) \quad (1)$$

4 Proposed DUR-FF Cell

4.1 Structure and Simulations

The schematic of the proposed DUR-FF design is presented in Fig. 8. It can be seen that the DUR-FF is made of a master latch as well as a slave latch, each constructed from triple mutually connected DICEs named DICE A1 to C1 (and A2 to C2 that are CG-based ones). The master latch has three common nodes (namely I1 to I3) between DICEs. The DUR-FF can be initialized through three TGs (i.e., switches marked with NCK). In the slave latch, I4 to I6 are common nodes between DICEs. In the DUR-FF, D and Q are the input and the output, respectively.

The normal working operations of the DUR-FF are discussed below.

(1) Firstly, CLK is set to high and NCK is set to low, thus D can initiate the master latch through three TGs (i.e.,

switches marked NCK). However, the slave latch still has no values because the inverters marked with CLK are blocked.

(2) Next, CLK becomes low and NCK becomes high, thus the master latch works in hold mode storing the D-value. Meanwhile, all inverters in the slave latch can output values, and thus the latch can output the value received from the master latch. At this time, feedback loops in the slave latch cannot be formed since the CG-based transistors in DICEs are OFF so that the inverters can initialize the slave latch easily and the value of Q can be determined by the output of the inverter only so as to reduce delay.

(3) Subsequently, CLK becomes high and NCK becomes low, thus the master latch can receive a new D-value but the slave latch can store (feedback loops in the slave latch can be formed) and output the former D-value.

(4) Finally, CLK becomes low and NCK becomes high, thus the master latch can store the current D-value received in step (3) and the slave latch can output this value received from the master latch.

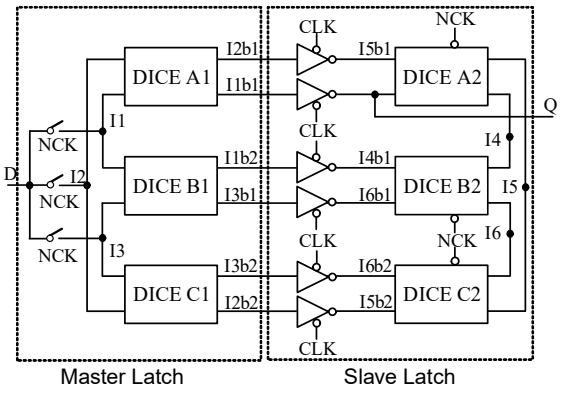

Fig. 8. Schematic of the proposed DUR-FF.

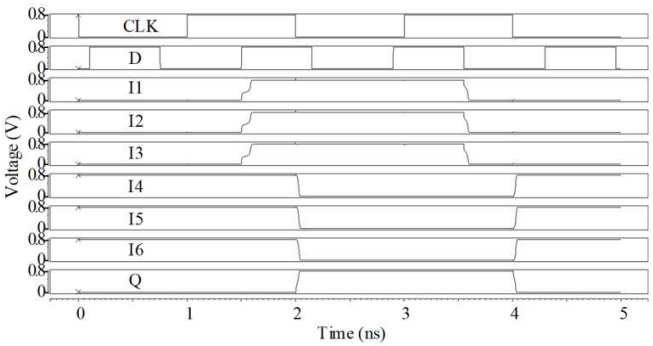

Fig. 9. Simulation results for normal operations of the proposed DUR-FF.

Figure 9 presents the results of the simulations for the normal operations. It should be noted that the simulation conditions of the proposed DUR-FF are the same as that of the proposed DUT-FF. The following scenarios can be seen from Fig. 9.

(1) Initially, when CLK is high (D has an initial D-value 0), the master latch can be pre-charged (I1 = I2 = I3 = D = 0).

(2) Next, CLK becomes 0 during 0ns and 1ns, hence the master latch can keep the D-value in (1) and the slave latch can output this value received from the master latch through Q.

(3) Subsequently, CLK becomes 1 during 1ns and 2ns, and hence the master latch can receive a new D-value. Meanwhile, the slave latch can store and output its former D-value.

(4) Finally, CLK becomes 0 during 2ns and 3ns, the master latch can keep the final D-value in step (3). Note that the final D-value is 1 because it is changed to 1 at about 1.5ns. Meanwhile, the slave latch can output this final D-value received from the master latch. Therefore, Q-value can change along with the D-value only at the falling edge of the CLK. We can see from Fig. 9 that the results of the simulations can clearly show the correct working flow of the DUR-FF. The layout of the proposed DUR-FF design is presented in Fig. 10.

4.2 SNU/DNU Tolerance and Verifications

SNU recoverability principles are firstly discussed. Note that a DICE cell is SNU-recoverable so that the interlocked DICEs in the master/slave latch are also SNU-self-recoverable. Therefore, the proposed DUR-FF is SNU-self-recoverable.

The DNU self-recovery principles are introduced here. Figure 8 indicates that the master latch has the same construction as the slave latch. Thus, only the slave latch is selected to discuss the DNU recoverability principles during hold mode (the inverters in the slave latch are blocked at this time). Note that only the inverters' outputs, as well as common nodes I4 to I6 of DICEs A2 to C2, should be considered for DNU-recoverability principle discussion. We only need to consider the following five cases due to the symmetrical structure of the slave latch.

Case 1: Two inputs of one DICE are impacted by a DNU. The key node-pair is <I5b1, Q> only. It can be seen from Fig. 8 that DICE A2's outputs are the single-nodes of the non-impacted DICEs B2 and C2, respectively. Hence, the DICE A2's outputs can keep correct values because non-impacted DICEs B2 and C2 are SNU-self-recoverable.

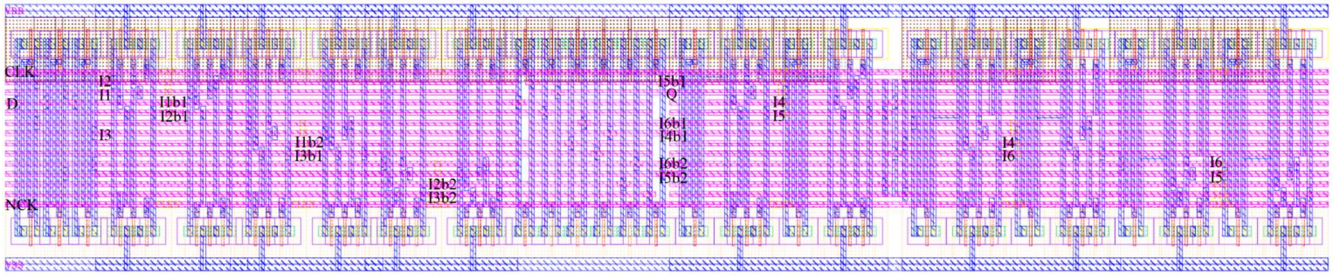

Fig. 10. Layout of the proposed DUR-FF design.

Therefore, the errors in the inputs of DICE A2 can be removed. In other words, <I5b1, Q> is DNU-self-recoverable (which will be demonstrated in Fig. 11).

Case 2: Two single-inputs of two DICEs are impacted by a DNU. Clearly, the representative node-pair is <I5b1, I4b1> only. We can see from Fig. 8 that only the single-nodes of DICEs A2 and B2 are affected. Thus, the DNU (i.e., two SNUs) can be removed by DICEs A2 and B2. In other words, <I5b1, Q> is DNU-self-recoverable.

Case 3: Two common nodes of DICEs are impacted by a DNU. The representative node-pair is <I4, I5> only. We can see from Fig. 8 that only the single-nodes of DICEs B2 and C2 are impacted. Thus, DICEs B2 and C2 can delete the DNU. Therefore, <I4, I5> is DNU-self-recoverable.

Case 4: A DNU impacts the output and one input of one DICE (or another DICE's output because it is a common node). The key node-pair only includes <I4, Q>. We can see from Fig. 8 that only a single node of the SNU-recoverable DICE B2 is affected. Therefore, the error on I4 of DICE B2 can be removed, and then the error on Q of DICE A2 can be removed. In other words, <I4, Q> is DNU-self-recoverable.

Case 5: One input of one DICE, as well as one output of another DICE (or the third DICE's output because it is a common node), are impacted by a DNU. The key node-pair only includes <I6b2, I4>. We can see from Fig. 8 that the DNU only impacts single-nodes of DICEs A2 to C2. Thus, the DNU can be removed by the SNU-recoverable DICEs. In other words, <I6b2, I4> is DNU-self-recoverable.

Figure 11 presents the simulation waveforms of all representative DNUs for Cases 1 to 5 as mentioned above. It can be seen that a DNU was injected to <I5b1, Q>, <I5b1, I4b1>, <I4, I5>, <I4, Q> and <I6b2, I4> during 1 and 2 ns when Q-value is 0, and a DNU was also injected to these node-pairs during 3 and 4 ns when Q-value is 1. Figure 11 also shows that all node-pairs can recover from DNUs. In summary, the DUR-FF is DNU-self-recoverable. Therefore, the DUR-FF is also SNU-self-recover.

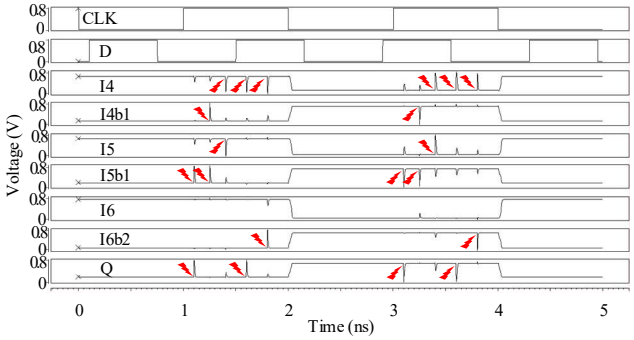

Fig. 11. Simulation results of all indicative DNU injections for the slave latch of the proposed DUR-FF.

5 Comparison and Evaluations

In this section, comparisons to typical FFs, such as the TUFF, the TMR-FF and those in [14-22, 24-25, 29, 34, 37] are performed using the same simulation conditions introduced in the above sections (22nm CMOS library and 0.8V supply voltage under room temperature).

Reliability comparisons are presented in Table 1. Clearly, the TUFF and the S2C-FF cannot tolerate SNUs and DNUs since they have at least one counterexample showing that they will output a wrong value when they suffer from an SNU/DNU. The TMR-FF, HPST-FF, SEUR-NVFF, DNUR-FF, DRRH-FF, Quatro-FF and HLCRT-FF are only SNU-tolerant. In other words, they cannot provide complete SNU recovery, DNU tolerance, and DNU recovery. Therefore, they are not reliable especially when SNU/DNU recovery is required. The DICE-FF and DURI-FF can only recover from any SNU; nevertheless, they can only recover from partial DNUs since it is only partially DNU hardened. We can see from Table 1 that the DUT-FF can tolerate SNUs/DNUs and the DUR-FF can provide not only SNU/DNU tolerance but also SNU/DNU recovery. Therefore, the proposed DUT-FF and DUR-FF are robust. Note that, some FFs constructed from DNU-tolerant latches, such as RH-2 [21], DNCSST [25], FDICE [24], DONUT [37], and DeltaDICE [22], are also compared in Table 1. Moreover, HTNURL [38] is a triple-node-upset hardened latch but this paper mainly considers DNU-hardening so that it is not considered for comparison.

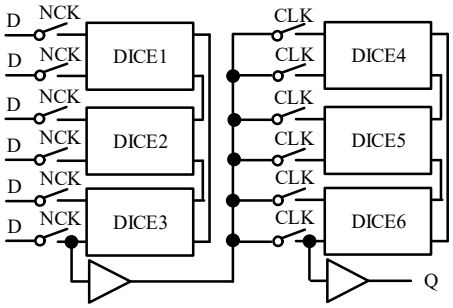

Fig. 12. Schematic of the DeltaDICE-FF.

Readers may concern that the proposed DUR-FF is similar to the DeltaDICE based FF, i.e., DeltaDICE-FF (see Fig. 12). However, compared to the DeltaDICE-FF, the DUR-FF is an advanced version with low delay, low power, low DPAP and low setup time. The DeltaDICE intended to use six transmission gates to pre-charge the latch, but we only use three transmission gates to pre-charge the master latch. The embedded buffer at the bottom of the DeltaDICE also impacts its performance. In DUR-FF, clocked transistors are used to reduce power for the slave latch but they are not used in the master latch so as to balance the power and area overhead.

Table 1 also shows the overhead comparisons among these FFs, in terms of delay, power dissipation, and silicon area. In Table 1, "Delay" means the transmission delay from CLK to Q, i.e., the average of the rise and fall delays from CLK to Q, "Power" means the average of dynamic and static power dissipation, "Area" means the silicon area measured through layout, and delay-power-area product (DPAP) means the product calculated by multiplying the CLK-Q delay, power consumption, and silicon area to comprehensively evaluate the overhead of all FFs. In Table 1, the setup time is also compared. The setup time is the minimum amount of time during which the input is held steady before a CLK event. Note that,

TABLE 1
RELIABILITY AND OVERHEAD COMPARISON RESULTS AMONG THE TOLERANCE AND RECOVERY FFS

FFs	SNU Tolerance	SNU Recovery	DNU Tolerance	DNU Recovery	Delay (ps)	Power (μW)	Area (μm^2)	DPAP $\times 10^2$	Setup Time (ps)
TUFF	×	×	×	×	17.23	1.06	2.97	0.54	6.62
S2C-FF [14]	×	×	×	×	29.37	1.08	4.20	1.33	10.49
TMR-FF	√	×	×	×	45.41	3.01	9.80	13.39	8.03
HPST-FF [15]	√	×	×	×	23.00	1.00	9.80	2.25	43.31
SEUR-NVFF [16]	√	×	×	×	18.30	1.03	7.35	1.38	7.30
DNUR-FF [17]	√	×	×	×	42.39	2.71	11.29	12.97	14.96
DRRH-FF [18]	√	×	×	×	43.01	1.58	5.94	4.04	8.28
Quatro-FF [19]	√	×	×	×	38.99	4.95	6.14	11.85	72.61
HLCRT-FF [34]	√	×	×	×	4.80	1.65	8.32	0.66	5.68
DICE-FF [20]	√	√	×	×	17.13	1.72	5.64	1.66	5.19
DURI-FF [29]	√	√	×	×	20.17	4.59	11.58	10.72	28.33
RH2-FF [21]	√	×	√	×	28.23	2.03	11.48	6.58	23.77
DNCSST-FF [25]	√	×	√	×	70.77	4.48	11.88	37.67	46.58
DUT-FF (Proposed)	√	×	√	×	14.00	2.13	9.50	4.35	14.29
FDICE-FF [24]	√	√	√	×	18.69	1.62	5.85	1.25	6.98
DONUT-FF [37]	√	√	√	√	37.56	4.25	11.58	18.49	30.12
DeltaDICE-FF [22]	√	√	√	√	89.82	5.45	12.77	62.51	54.38
DUR-FF (Proposed)	√	√	√	√	12.80	3.24	13.37	5.54	31.31

according to Figs. 5 and 9, the rise and fall delays from CLK to Q can be automatically estimated through the "measure" statement using Synopsis HSPICE.

(***Delay Comparison***) From a qualitative point of view, delay comparisons are presented in Table 1. We can see that the HLCRT-FF, DUT-FF and DUR-FF only have a small delay since there are only a few transistors between the CLK-controlled TGs in the slave latch and node Q of the FFs. Any other FF has a larger delay because there are redundant transistors in the paths from CLK to Q. Note that the HLCRT-FF has the smallest delay because Q is connected to the node that is close to the input of the FF.

(***Power Comparison***) In terms of power consumption, we can see from Table 1 that the HPST-FF has the lowest power consumption since the FF uses clock-gating to reduce current competition and its area is not large. However, the DeltaDICE-FF has the highest power consumption mainly since it has much current competition in feedback loops and its area is not small. The proposed DUT-FF and DUR-FF consume moderate power dissipation compared to the other FFs and the power consumption of the DUR-FF is even low when compared to the FFs of the same type.

(***Area Comparison***) In terms of silicon area, we can see from Table 1 that the TUFF consumes the smallest silicon area because of the use of less transistors. Conversely, the proposed DUR-FF has the largest area since it has to use extra logic to provide SNU/DNU recoverability. Note that, the proposed DUT-FF consumes moderate area and can also provide completely SNU/DNU tolerance.

(***DPAP Comparison***) In terms of DPAP, it can be seen from Table 1 that the TUFF has the smallest DPAP since its delay, power, and/or silicon area are small. On the contrary, the DeltaDICE-FF has the largest DPAP, mainly due to its large delay. Note that, the proposed DUT-FF and DUR-FF have moderate DPAP compared with the other FFs.

(***Setup time Comparison***) In terms of setup time, we can see from Table 1 that the DICE-FF, HLCRT-FF, and TUFF only need a small amount of time during which the input is held steady before a CLK event, and thus making that their setup time is small. Conversely, the DeltaDICE-FF and DNCSST-FF need a large amount of time during which the input is held steady before a CLK event, and thus making that their setup time is large. In addition, the setup time of the DUR-FF is larger (but not the largest).

TABLE 2
PERCENTAGE OF INCREASED COSTS FOR THE PROPOSED DUT-FF COMPARED WITH THE FFS OF THE SAME TYPE

FFs	Delay	Power	Area	DPAP	Setup time
RH2-FF	-50.41	4.93	-17.25	-33.89	-39.88
DNCSST-FF	-80.22	-52.46	-20.03	-88.45	-69.32
Average	-65.32	-23.77	-18.64	-61.17	-54.60

TABLE 3
PERCENTAGE OF INCREASED COSTS FOR THE PROPOSED DUR-FF COMPARED WITH THE FFS OF THE SAME TYPE

FFs	Delay	Power	Area	DPAP	Setup time
DONUT-FF	-65.92	-23.76	15.46	-70.04	3.95
DeltaDICE-FF	-85.75	-40.55	4.69	-91.14	-42.42
Average	-75.84	-35.06	10.08	-80.59	-19.24

Next, to provide a quantitative comparison result in terms of CLK-Q delay (ΔDelay), power dissipation (ΔPower), silicon area (ΔArea), comprehensive DPAP (ΔDPAP) and setup time (Δsetup time), the percentages of Increased costs (PICs) of the DUT-FF compared with the alternative FFs were calculated with Eq. (2) and the results are shown in Table 2. Clearly, the negative PICs are better. The average PICs are compared and discussed. For the DUT-FF, we can see from Table 2 that, compared to the FFs of the same type, all the average PICs are negative. Especially, the delay of the DUT-FF is reduced by 65.32% on average when compared to the FFs of the same type.

On the other hand, the PICs of the DUR-FF compared to the alternative FFs were also calculated with Eq. (2). It can be seen from Table 3 that, the average PICs of the CLK-Q delay, power consumption, silicon area, DPAP as well as setup time are -75.84%, -35.06%, 10.08%, -80.59% and -19.24%, respectively. Therefore, the advantages of the DUR-FF are achieved at the cost of silicon area. Especially, the delay of the DUR-FF is reduced by 75.84% on average when compared to the FFs of the same type. In summary, the DUT-FF and DUR-FF not only provide high reliability but also reduce delay especially when compared to the FFs of the same-type.

$$\Delta\,(\%) = [(Cost_{Proposed} - Cost_{Compared}) / Cost_{Compared}] \times 100 \quad (2)$$

It is reported in [32, 34, 38, 39] that the PVT variation impacts on storage cells are becoming much severe especially in nano-scale CMOS technologies. Here we use the method as in [32] to evaluate the PVT variation impacts on delay and power of FFs.

The effect of supply voltage variations on power of the proposed DUT-FF is measured (see Fig. 13). For the first datum/sample on the left-bottom side in this figure, i.e., 1.05uW, it means that, the power of the FF is 1.05uW when the supply voltage is 0.65V. It can be seen that the power of the FF increases when the supply voltage increases. There are seven samples in Fig. 13 for supply voltage variations from 0.65V to 0.95V. These samples can form six curve segments, i.e., <0.65, 0.70>, <0.70, 0.75>, <0.75, 0.80>, <0.80, 0.85>, <0.85, 0.90> and <0.90, 0.95>. The slope of each curve segment can be computed. For example, the slope of <0.65, 0.70> is equal to the difference between the power measured at 0.70V and 0.65V. Then, the average slope (AS) of the entire curve (i.e., <0.65, 0.95>) can be obtained by averaging the absolute slope values of six curve segments with Eq. (3). Table 4 shows the calculation result of each slope so that the average slope can be obtained. Clearly, the average slope can represent the sensitivity of the power of the DUT-FF to the variation of the supply voltage.

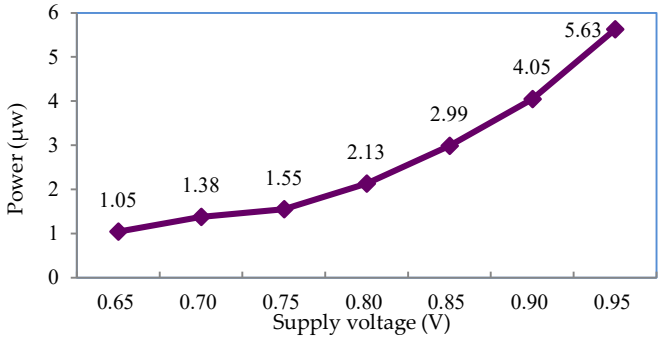

Fig. 13. The effect of supply voltage variations on power for DUT-FF.

$$AS = \frac{1}{i-1}\sum_{k=2}^{i}|P_k - P_{k-1}| \quad (3)$$

TABLE 4
THE CALCULATION RESULT OF EACH SLOPE FOR FIG. 13

Curve	Slope	Curve	Slope
<0.65, 0.70>	0.33	<0.80, 0.85>	0.86
<0.70, 0.75>	0.17	<0.85, 0.90>	1.06
<0.75, 0.80>	0.58	<0.90, 0.95>	1.58

* The average slope is 0.76.

We calculated all the average slopes (i.e., sensitivities) of delay and power of all alternative FF cells to PVT

TABLE 5
SENSITIVITY OF DELAY OR POWER OF THE ALTERNATIVE FFS TO PVT VARIATIONS

FF	Supply voltage vs Delay	Supply voltage vs Power	Temperature vs Delay	Temperature vs Power (×10²)	Threshold voltage increment vs Delay	Threshold voltage increment vs Power (×10²)	ECL vs Delay	ECL vs Power (×10²)
TUFF	12.56	0.52	7.72	7.00	1.68	3.60	4.99	4.00
S2C-FF	7.86	0.36	7.63	7.16	3.13	4.36	7.09	5.02
TMR-FF	19.08	1.43	16.12	18.38	5.11	10.30	10.66	15.20
HPST-FF	6.55	0.45	4.93	7.13	4.37	6.10	6.44	6.20
SNUR-NVFF	6.88	0.40	4.16	4.75	2.67	3.20	4.36	3.90
DNUR-FF	14.02	0.97	11.08	11.75	5.90	11.80	8.27	10.90
DRRH-FF	18.59	0.57	17.67	8.63	4.27	4.00	8.46	11.70
Quatro-FF	12.56	1.82	10.79	19.50	2.42	23.40	37.70	39.10
HLCRT-FF	0.75	0.26	0.68	6.83	0.83	5.85	2.62	5.85
DICE-FF	5.79	0.59	3.30	5.75	1.87	4.60	5.31	5.40
DURI-FF	3.21	1.55	4.14	20.54	1.75	15.33	13.20	5.13
RH2-FF	13.28	0.96	3.95	13.21	2.85	7.88	7.66	6.02
DNCSST-FF	17.85	0.78	1.23	9.77	3.66	13.02	4.43	7.33
DUT-FF (Proposed)	2.79	0.76	4.66	14.23	1.73	9.22	19.05	5.88
FDICE-FF	6.03	0.67	3.01	5.88	2.03	4.32	5.45	5.02
DONUT-FF	22.36	1.44	6.57	11.58	2.33	14.86	5.56	6.12
DeltaDICE-FF	23.56	1.66	5.61	25.69	2.21	15.56	13.96	6.26
DUR-FF (Proposed)	2.02	1.12	3.82	19.45	0.94	12.00	10.19	4.37

variations with Eq. (3) and the results are shown in Table 5. In Table 5, "Supply voltage vs Delay", "Temperature vs Delay", "Threshold voltage increment vs Delay" and "ECL vs Delay" denote the sensitivity of delay of each FF cell to variations of supply voltage, temperature, threshold voltage and ECL, respectively. Here, ECLs denote effective channel length of transistors. Moreover, "Supply voltage vs Power", "Temperature vs Power", "Threshold voltage increment vs Power", and "ECL vs Power" denote the sensitivity of power of each FF cell to variations of supply voltage, temperature, threshold voltage and ECL, respectively. The standard supply voltage was set to 0.8V. Supply voltages were varied from 0.65V to 0.95V with a 0.05V increment step by step for simulations of supply voltage variations. The standard temperature was room temperature. Temperatures were varied from -25°C to 125°C with a 25°C increment step by step for simulations of temperature variations. The threshold voltage was varied from the original value with a 0.01V increment step by step (totally 10 increments) for simulations of threshold voltage variations. The standard ECL was set to 22nm. ECLs were varied from 22nm to 32nm with a 1nm increment step by step for simulations of ECL variations. It should be noted that ECLs are difficult to be varied to small sizes below the standard values [39]. It can be seen from Table 5 that the proposed DUT-FF and DUR-FF are moderately sensitive to PVT variations.

6 Conclusions and Future Works

Technology scaling increases the sensitivity of integrated circuits to soft errors. This paper has presented a novel FF design (namely DUT-FF) that can completely tolerate SNUs/DNUs caused by the strike of particles in aerospace, making the DUT-FF suitable for aerospace applications. The use of fast-speed CLK-Q path and clocked transistors leads to a smaller delay, making the DUT-FF also applicable to high-performance applications. Besides, for those node-pairs that cannot self-recover from SNUs and DNUs, this paper has also presented an SNU/DNU self-recoverable DUR-FF. The SNU/DNU self-recovery is owing to the employed interlocked DICEs; the DNR-FF also has a smaller delay, making it suitable for high-performance applications. Simulation results have shown the SNU/DNU tolerance and/or recovery of the proposed FFs, the small delay overhead of the proposed FFs especially when compared to the FFs of the same-type, as well as the reasonable PVT variation impacts on the proposed FFs.

Note that, to propose an FF that has advantages in all respects (such as high reliability, small area, small delay, low power, insensitivity to PVT) is difficult. In our further work, we will try to propose an advanced FF that has advantages in most respects with much high novelty. Moreover, readers may concern experimental results (i.e., radiation campaign) for both proposals for more deep evaluations. However, due to limited simulation and experiment conditions, we currently cannot provide these evaluation results so that we consider them as interesting and important further works.

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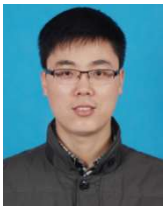
Aibin Yan received the Ph. D degree from Hefei University of Technology (HFUT), in 2015. In 2016, he joined Anhui University (AHU). In 2023, he joined HFUT working as a full professor and PhD supervisor. He created AHU Institute of Chip Design and Test and is serving as its director. His research interests include radiation hardening for ICs, etc.

Aoran Cao is with the School of Computer Science and Technology, AHU, Hefei, China. Currently, he is pursuing his M.S. degree for computer technology major in AHU. He received his B.E degree from Hebei North College in 2019. His research interests include radiation hardening for CMOS ICs, such as latches, flip-flops, and memory cells.

Zhengfeng Huang received his Ph.D. degree from Hefei University of Technology (HFUT) in 2009. He joined HFUT as an Assistant Professor in 2004 and now he is a professor since 2018. He worked as a visiting scholar at the University of Paderborn, Germany from 2014 to 2015. He served on the organizing committee of the IEEE ETS in 2014. His research interests include design for soft error tolerance/mitigation.



Jie Cui received his Ph.D. degree from University of Science and Technology of China, Hefei, in 2012. Currently, he is a vice dean, a professor, and a professor supervisor with the School of Computer Science and Technology, Anhui University, Hefei, China. His research interests include IoT security, applied cryptography, software defined networking, vehicular ad hoc network, and VLSI fault tolerance.

Tianming Ni received his Ph.D. degree from Hefei University of Technology, Hefei, China, in 2018. He joined the Key Lab of Advanced Perception and Intelligent Control of High-end Equipment, Ministry of Education, College of Electrical Engineering, Anhui Polytechnic University in 2018. His research interest includes built-in-self-test, design automation of digital systems, design for IC reliability, 3D IC test and fault tolerance.

Patrick Girard (Fellow, IEEE) received his Ph.D. degree from University of Montpellier, France, in 1992. He is currently Research Director at CNRS and works in LIRMM. He was head of Microelectronics Department of LIRMM. He is co-Director of an International Associated Laboratory « LAFISI » created by the CNRS and the University of Montpellier with the Politecnico di Torino, Italy. His research interests include aspects of digital testing and memory testing. Reliability and fault tolerance are also part of his research.

Xiaoqing Wen (Fellow, IEEE) received his Ph.D. degree from Osaka University, Japan, in 1993. He joined SynTest Technologies, Inc., USA, in 1998, and served as its CTO. He joined Kyushu Institute of Technology, Japan, where he is currently a professor. He founded Dependable Integrated Systems Research Center and served as its director. He holds 43 U.S. Patents and 14 Japan Patents on VLSI testing. His research interests include VLSI test, diagnosis, and testable design.

Jiliang Zhang received his Ph.D. degree from Hunan University (HNU), China in 2015. He worked as a Research Scholar at the Maryland Embedded Systems and Hardware Security Lab, University of Maryland, USA. In 2017, he joined HNU. He is currently a professor and vice dean at the College of Integrated Circuits, HNU. He was the recipient of CCF IC Early Career Award, and the winner of Excellent Youth Fund of the NSFC. His current research interests include Hardware Security, Integrated Circuit Design and Intelligent System.