Two sextuple cross-coupled SRAM cells with double-node-upset protection and cost optimization for aerospace applications

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Abstract—**This paper is the first to present a double-node upset (DNU) protected and sextuple cross-coupled static-random-access memory (SRAM) cell, i.e., SCCS-18T, for aerospace applications. The cell can recover from all possible single-node upsets (SNUs) as well as part of DNUs due to its large feedback loop that can retain values and intercept errors. To improve DNU self-recoverability, an enhanced version of the SCCS-18T cell, namely SCCS-18T-EV, is also proposed. With the new structure, the SCCS-18T-EV can recover from more DNUs. Since parallel access transistors are used, the proposed cells achieve optimized read/write performance. Simulation results clearly demonstrate the node-upset tolerance as well as the optimized operation performance of the proposed SCCS-18T and SCCS-18T-EV cells in comparison with the state-of-the-art of SNU and DNU hardened SRAM cells.**

Index Terms—static-random-access memory, radiation hardening, node-upset recovery, cost optimization

I. INTRODUCTION

MOORE's Law was found in 1965 by Gordon Moore, who stated that the number of transistors in a semiconductor integrated circuit would double every 18 months and the circuit's performance would improve accordingly. However, as the process of integrated circuits becomes more delicate, the distance between transistors becomes smaller, the supply voltage becomes lower, and the node capacitance becomes smaller, resulting in charge sharing of storage nodes. As a result, the occurrence probability of soft errors significantly increases [1]. Collisions of radiative particles with storage nodes can cause soft errors [2]. SNUs as well as DNUs are two common types of radiation-induced soft errors. On one hand, due to the charge drift between the drain and the substrate of a transistor caused by the strike of a particle, the logical state of a storage node can be changed, resulting in an SNU. On the other hand, due to charge-sharing, a particle strike can affect two adjacent nodes, causing a DNU. In a radiative environment, if a soft error occurs in an SRAM that cannot be recovered, the wrong value will be stored/used. Therefore, in the worst case, the entire system may crash [3]. These situations put high demands on the robustness of SRAMs, which brings more challenges to circuit designers. Therefore, there is a strong need for circuit designers to design novel radiation-hardened SRAM cells with better robustness.

SNU and DNU problems have been addressed by leading researchers using the radiation hardening by design (RHBD) approach to design innovative storage cells [4-19], among which SRAM cells [10-19]. A traditional 6T SRAM memory cell consists of two PMOS and four NMOS transistors, in which two of the NMOS transistors are used to access values, and all other transistors work to store values. However, a 6T storage cell is not SNU hardened; thus, many improved radiation-hardened storage cells have been proposed. Among them, NASA-13T [10], RHPD-12T [11], RHBD-10T [12], RHM-12T [13], Lin-12T [14], DNUSRM [15], QCCM-10T [16], QCCM-12T [16], S4P8N [17], and S8P4N [17] are typical SNU and/or DNU mitigated ones. However, they still suffer from the following severe problems.

(1) Some SRAM cells, such as NASA-13T [10], RHBD-10T [12], RHM-12T [13] and Lin-12T [15], have a large reading access time. Some SRAMs, such as NASA-13T [10] and DNUSRM [15], have a large write access time and a high power consumption.

(2) Some SRAM cells, such as NASA-13T [10], RHPD-12T [11], RHBD-10T [12], RHM-12T [13], QCCM-10T [16], and QCCM-12T [16], cannot recover from all possible SNUs.

(3) Some SRAM cells, such as NASA-13T [10], RHPD-12T [11], RHBD-10T [12], RHM-12T [13], S4P8N [17], S8P4N [17], and Lin-12T [14], cannot provide better recovery from DNUs.

We previously proposed a low-overhead SRAM cell [16]; however, but there is still at least one counter example showing that the cell cannot achieve complete SNU recovery. We also
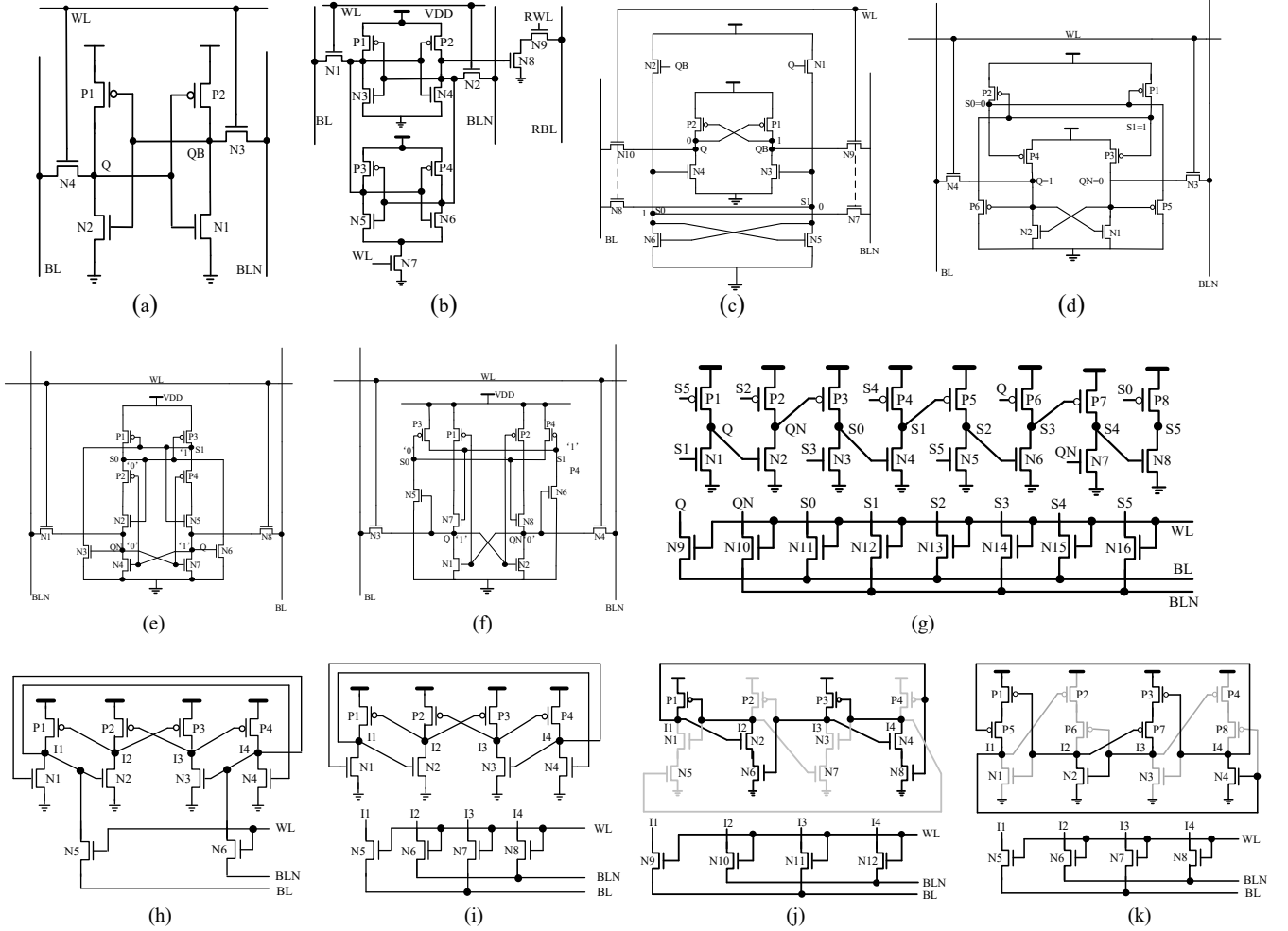
Fig. 1. Schematics of existing SRAMs. (a) 6T, (b) NASA-13T [10], (c) RHPD-12T [11], (d) RHBD-10T [12], (e) RHM-12T [13], (f) Lin-12T [14], (g) DNUSRM [15], (h) QCCM-10T [16], (i) QCCM-12T [16], (j) S4P8N [17], and (k) S8P4N [17].

proposed SNU and DNU hardened SRAM cells in [15], but their area overhead and power consumption are high. Reliability and overhead need to be well balanced for radiation-hardened SRAMs.

In this paper, by extending the basic idea of our previous paper [19], we propose two SRAM cells based on the RHBD approch. Both of them are composed of 6 PMOS transistors and 12 NMOS transistors. The 6 NMOS transistors are for reading and writing operations, and the remaining 12 transistors are for values storage. Owing to a novel interlocking mechanism, the proposed cells can recover from all possible SNUs and some DNUs with particularly significant cell-performance. The balanced robustness and cost effectiveness of the proposed cells are clearly verified by simulations.

The rest of this paper is organized as follows. Section II describes the previous hardened memory cells and their advantages and disadvantages. Section III presents the schematic of the proposed SCCS-18T cell, its working principles and simulation results. Section IV introduces the proposed SCCS-18T-EV cell. Section V describes the comprehensive evaluation and comparison results. Section VI concludes the paper.

II. TYPICAL HARDENED SRAM MEMORY CELLS

Figure 1 presents the structures of the various typical SRAM memory cells mentioned above, such as NASA-13T [10], RHPD-12T [11], RHBD-10T [12], RHM-12T [13], Lin-12T [14], DNUSRM [15], QCCM-10T [16], QCCM-12T [16], S4P8N [17], and S8P4N [17].

The conventional 6T cell comprises six transistors, as shown in Fig. 1-(a). In its schematic, transistors P1 and N2 form an inverter and transistors P2 and N1 form another inverter. These inverters feed each other to construct a feedback loop to retain values. However, it cannot provide protection against SNUs due to its simple structure. Consequently, many novel and robust cells have been designed by researchers for reliability enhancement.

Fig. 1-(b) shows the structure of the NASA-13T cell [10], which comprises two parts. The upper part is a traditional 8T cell that has an independent read access operation compared to the 6T cell. The lower part acts as a redundancy module for value retention. Compared with the 6T cell, the NASA-13T cell can provide SNU mitigation. Nevertheless, the NASA-13T cell cannot tolerate large-energy-particle-induced SNUs.

Fig. 1-(c) shows the structure of the RHPD-12T cell [11]. Compared with other existing SRAM cells, the RHPD-12T cell can not only recover from many possible single-node upsets, but can also provide better circuit performance. However, the RHPD-12T cell cannot tolerate large-energy-particle-induced DNUs.

Fig. 1-(d) shows the structure of the RHBD-10T cell [12]. Compared with other 10T SRAM cells, the RHBD-10T cell can provide recovery from many SNUs at the cost of increased read/write access time. Moreover, compared with other hardened SRAM cells, the RHBD-10T cell is a candidate for aerospace applications as it provides a trade-off among area, power, delay and reliability for storage circuits suffering from radiation.

Fig. 1-(e) shows the structure of the RHM-12T cell [13] that cannot recover from many SNUs regardless of upset polarity and strength but can also recover from DNUs on fixed node pairs. Process variation simulations demonstrated the SNU tolerance of the cell under process variations. Moreover, the cell has a low read static noise margin (RSNM). The transistors N4, N7, P1 and P3 can be enlarged and/or the transistors N1 and N8 can be shrunk so as to improve the RSNM but the other parameters, such as reliability, area, power, and delay, may be affected.

Fig. 1-(f) shows the structure of the Lin-12T cell [14]. The gate terminals of transistors N5 and N6 connect output nodes (Q and QN) that feed bit lines (BL and BLN) through access transistors. Gate terminals (S0 and S1) of redundant transistors P3 and P4 are also storage nodes that can ensure SNU recovery. Although the Lin-12T cell can recover from any possible SNU, only one pair of nodes can tolerate DNUs.

Fig. 1-(g) shows the structure of the DNUSRM cell [15] that comprises 24 transistors, i.e., 8 PMOS transistors and 16 NMOS transistors. N9-N16 are access transistors while the remaining are used for value storage. The DNUSRM cell can provide recovery from all DNU, because of its redundant feedback loops. However, the number of the used transistors is too large, so that the cell suffers from large area and delay.

Fig. 1-(h) shows the structure of the QCCM-10T cell [16] that comprises 10 transistors, i.e., 4 PMOS transistors and 6 NMOS transistors. Transistors N5 and N6 are for access operations and the other transistors are used for value storage. The QUCCM10T can recover from major SNUs but its reading/writing access time is large.

Fig. 1-(i) shows the structure of the QCCM-12T cell [16]. In order to improve the access time of QCCM-10T, the QCCM-12T adds two NMOS transistors to access values. Compared with QCCM-10T, the QCCM-12T cell can also recover from major SNUs but it only has one node pair that can recover from DNUs either.

Fig. 1-(j) shows the structure of the S4P8N cell [17] that comprises 16 transistors, i.e., 4 PMOS transistors and 12 NMOS transistors. Transistors N9-N12 are for access operations and other transistors are used for value storage. The S4P8N can provide recovery from any possible SNU as well as a part of DNUs.

Fig. 1-(k) shows the structure of the S8P4N cell [17] that comprises 16 transistors, i.e., 8 PMOS transistors and 8 NMOS transistors. Transistors N5-N8 are for access operations, and the other transistors are used for value storage. Compared with the S4P8N cell, the S8P4N cell has an equivalent SNU/DNU tolerance. Nevertheless, the S8P4N cell only has four node pairs that can recover from DNUs.

III. PROPOSED SCCS-18T SRAM CELL

A. Schematic and Operations

Figure 2 shows the structure of the proposed SCCS-18T cell, which comprises 6 PMOS transistors and 12 NMOS transistors. Among them, 6 PMOS transistors as well as 6 NMOS transistors (i.e., N1-N6) are used to store values; the remaining 6 NMOS transistors (i.e., N7-N12) are used to read/write values. The word line (WL) is connected to the sources of N7-N12, and WL connects storage nodes to bit lines (i.e., BL and BLN). Figure 3 shows the structure of the proposed SCCS-18T cell in normal operations. When WL = 0, all reading transistors are turned OFF, and thus the SRAM cell is in the hold state, as shown in Fig. 3-(a). When WL = 1, transistors N7-N12 are turned on, and thus the SRAM cell turns on the read mode.
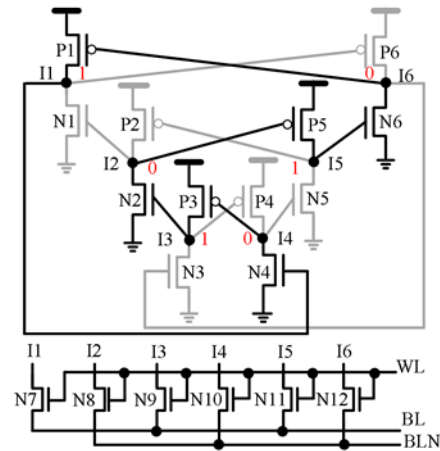

Fig. 2. The proposed SCCS-18T cell.

Let us now describe the read/write operations of the proposed SRAM cell. Assume that the SRAM cell currently stores the value 1, i.e., the values of I1, I3 and I5 are 1 and meanwhile the values of I2, I4 and I6 are 0. Before the writing 0 operation, set BL = 0, BLN = 1. At this time, the transistors P6, P4, P2, N1, N5 and N3 are ON, and the other memory transistors are OFF. This way, a large feedback loop (I6 -> I3 -> I4 -> I5 -> I2 -> I1-> I6) is formed to keep the value 0 in the SRAM cell and successfully write the value 0, as presented in Fig. 3-(b). Now, let us consider the operation of reading 0. Note that the BL and BLN values are preset to 1 before the read operation. At this point, since the reading transistors are all turned ON and I1 = I3 = I5 = 0, the BL voltage will discharge through N7, N9, and N11, while the BLN voltage remains 1 because I2 = I4 = I6 = 1. The voltage difference between BL and BLN can be amplified and detected by an induction amplifier, so as to read the value in the storage cell, as shown in Fig. 3-(c). Similarly,
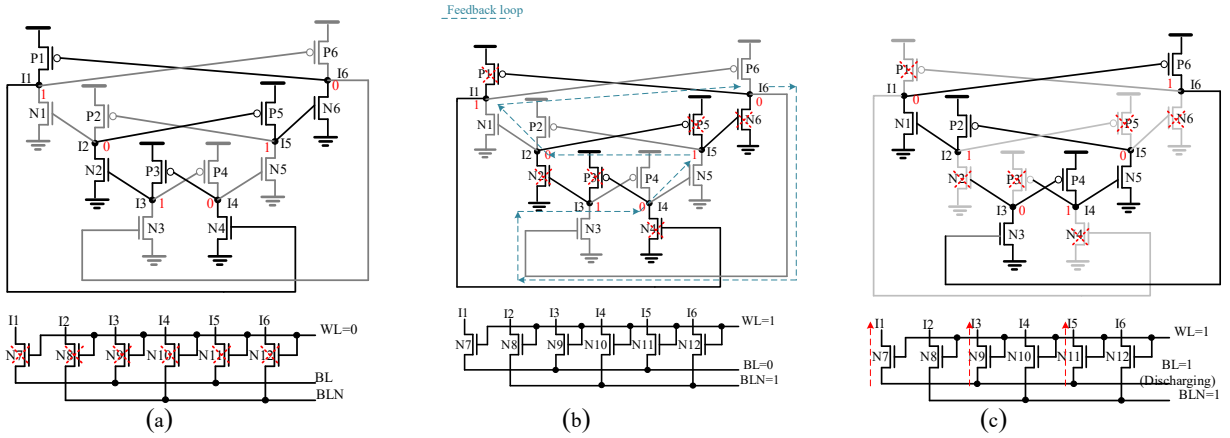
Fig. 3. Schematics of the proposed SCCS-18T cell's normal operations. (a) Hold '1'. (b) Write '0'. (c) Read '0'.

writing and reading 1 are similar to the operations discussed above; Therefore, they will not be described in detail. The layout of the SCCS-18T cell is shown in Fig. 4.
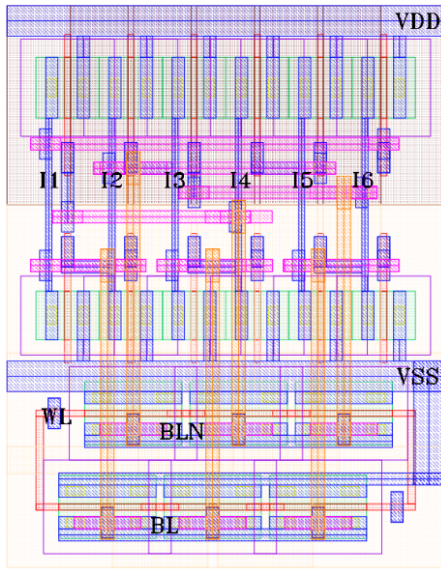

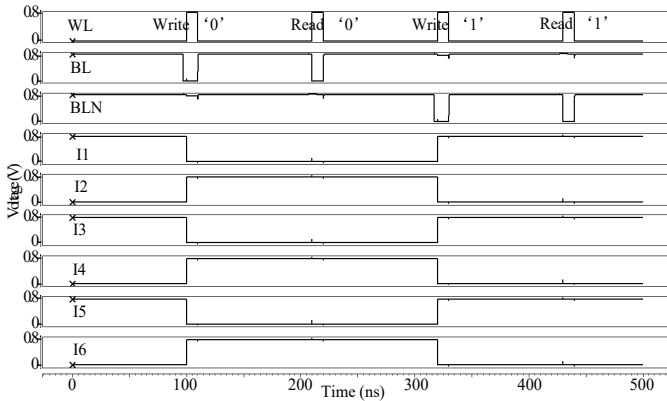Fig. 4. Layout of the proposed SCCS-18T cell.

Fig. 5. Read/write operations of the proposed SCCS-18T cell.

The SCCS-18T SRAM cell has been designed/implemented using a 22nm commercial CMOS process under the room temperature and with a 0.8V supply voltage. Figure 5 shows the simulation diagram of read and write operations of this cell. It

can be seen that the operations of writing 1 and 0 as well as reading 1 and 0 are correct. The correct values can also be stored in the SRAM cell through a special feedback loop.

The SNU-recovery of the SCCS-18T cell will be described below. Here, we only consider the SRAM cell when a 1 is stored in it (i.e., the values of I1, I3 and I5 are 1 and the values of I2, I4 and I6 are 0).

B. Principle of SNU Recovery

It can be seen from the structure of the SCCS-18T SRAM cell that I1 and I6, I2 and I5, and I3 and I4 are all symmetric nodes, meaning they have the same self-recovery situations when soft errors occur. Therefore, the self-recovery situations of I1, I2 and I3 nodes are analyzed.

Firstly, the situation of the I1 node upset is analyzed. When the value of I1 changes from 1 to 0, N4 is OFF and P6 is ON, while the values of I2, I3 and I5 do not change immediately. Therefore, N1 remains OFF, N6 remains ON, due to the temporary opening of P6, and the weak 1 of I6 is neutralized by the strong 0 of I6 so that I6 retains the value of 0. If I6 is 0, P1 is ON, N1 is OFF, and the value of I1 recovers to 1. At this point, N4 is ON and I4 remains 0. Hence, I1 can provide SNU recovery when it is flipped. The self-recovery the principle of I6 is similar.

Secondly, let us analyze the situation of the I2 node upset. When the value of I2 changes from 0 to 1, N1 will be turned ON and P5 will be OFF. However, the values of I3, I4 and I6 will not change immediately. Both P5 and N5 remain OFF, then I5 remains unchanged, P2 is OFF, N2 is ON, and I2 recovers to 0, P5 is ON, and I5 continues to maintain high voltage level. Therefore, I2 can provide SNU recovery when it is flipped. The self-recovery principle of I5 is similar.

Finally, let us analyze the situation of the I3 node upset. When the value of I3 changes from 1 to 0, N2 will be OFF and P4 will be ON, while the values of I1, I5 and I6 will not change immediately. Therefore, when N4 is ON, due to the temporary opening of P4, the weak 1 of I4 is neutralized by the strong 0 of I4, then I4 stays at the original value. Then P3 is turned ON, N3 is turned OFF, I3 is recovered to its correct value of 1, and N2 is turned ON, so that I2 continues to keep a low voltage level. Therefore, I3 can provide SNU recovery when it is flipped. The

self-recovery principle of I4 is similar.

In summary, nodes I1, I2 as well as I3 can be self-recovered, and I4, I5 and I6 nodes can also be self-recovered due to the symmetric nature. Therefore, all nodes of the SCCS-18T cell can provide SNU recovery. Figure 6 presents the SNU-recovery simulation results for the SCCS-18T cell. As shown in Fig. 6, I1 to I6 were simulated with downward-injection SNU-errors, respectively. Meanwhile, the upward-injection SNU-errors were also simulated on nodes I1 to I6, respectively. It can be seen from Fig. 6 that all nodes can recover from the SNU.
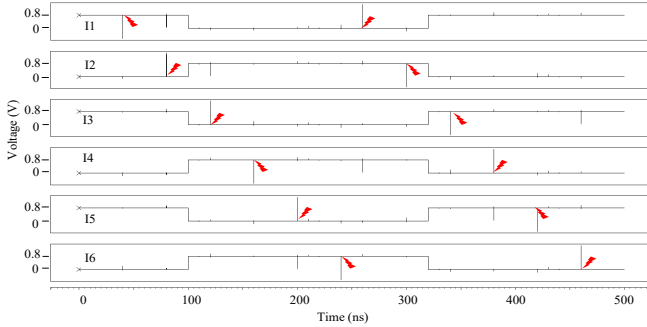

Fig. 6. Simulation result of SNU recovery for the SCCS-18T cell.

C. Principle of DNU Recovery

Let us first analyze the self-recovery of <I1, I2> node pair when the SCCS-18T cell stores 1. At this point, the value of I1 is 1, and the value of I2 is 0. After the upset, the value of I1 becomes 0 and value of I2 becomes 1, leading to the closure of N4 and P5 and the opening of P6 and N1. Since the value of I3 will not change immediately, P4 will remain OFF, while the value of I4 will remain unchanged and N5 will remain OFF. Since P5 is also turned OFF and the value of I5 remains at the original values, N6 is ON and P2 is OFF. Since P6 is temporarily ON, the strong 0 of I6 can neutralize the weak 1 of I6, so that the value of I6 remains at 0, then P1 is ON and N3 is OFF. Since I3 and I5 remain at original values, N2 remains ON, and P2 is OFF, I2 is restored, N1 is OFF, and I1 is restored. This shows that node pair <I1, I2> can recover from DNU when the cell stores 1. Due to the symmetry of the cell structure, <I5, I6> has the same DNU recovery principle.

Let us now analyze the self-recovery of <I3, I6> when the SCCS-18T cell stores 1. At this point, the value of I3 is 1, and the value of I6 is 0. After the upset, the value of I3 becomes 0 and the value of I6 becomes 1, causing N2 and P1 to become OFF and P4 and N3 to become ON. At this point, the values of I1 and I5 do not change immediately, so N4 is ON. Since P4 is temporarily ON, the value of I4 remains at 0. N6 remains ON and P6 remains OFF, so I6 returns to its original value of 0. If I4 and I6 retain their original values, N3 is OFF, P4 is ON, and I3 is restored to its original value 1. Therefore, node pair <I3, I6> can recover from DNU when the cell stores 1. Due to the symmetry of the cell structure, <I1, I4> has the same DNU recovery principle.

Finally, Let us analyze the self-recovery of <I4, I5> node pair when the SCCS-18T cell stores 1. However, for the brevity of the paper, the similar analysis of DNU recovery principle is omitted here. Note that <I2, I3> has the same DNU recovery principle compared with <I4, I5> because of the symmetry of the SCCS-18T cell.

It can be seen from the above discussions that, when the SCCS-18T cell stores 1, <I1, I2>, <I3, I6>, as well as <I4, I5> can recover from DNUs. Meanwhile, when the SCCS-18T cell stores 0, <I1, I4>, <I2, I3>, as well as <I5, I6> can recover from DNUs. This means that the SCCS-18T cell has up to six node pairs that can provide DNU recovery.

Figure 7 shows the simulation results of DNU-recovery for the proposed SCCS-18T. As shown in Fig. 7, when the SCCS-18T cell stores 1, after simulation verification, three node pairs <I1, I2>, <I3, I6> as well as <I4, I5> can provide DNU recovery. Meanwhile, when the SCCS-18T cell stores 0, after simulation verification, three node pairs <I1, I4>, <I2, I3> as well as <I5, I6> can provide DNU recovery. Note that node pairs <I1, I2>, <I1, I4>, <I2, I3>, <I5, I6>, < I3, I6>, and <I4, I5> were injected with an error at 50ns, 150ns, 200ns, 250ns, 370ns and 420ns, respectively. In summary, it can be seen from the above discussions and simulations that all of these above nodes can realize self-recovery.
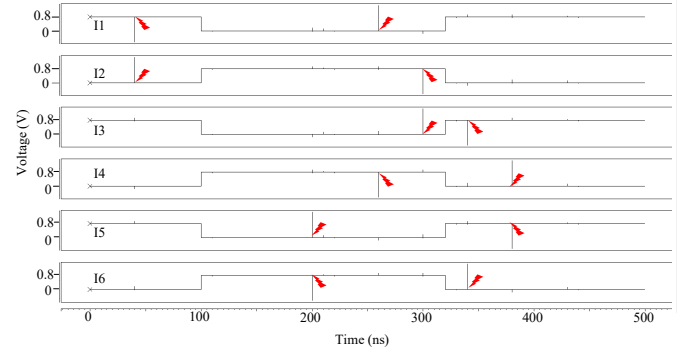

Fig. 7. Simulation results of DNU-recovery for the SCCS-18T cell.

For all error-injections, we used the double-exponential current-source model as in [17]. The rise and fall time parameters of the model were set to 0.1ps and 3.0ps, respectively [20]. We used the flexible HSPICE tool to perform all error-injections under a 22nm CMOS library with a 0.8V supply voltage and a considered room temperature.

IV. PROPOSED SCCS-18T-EV CELL

A. Structure and Operations

As shown in Fig. 8, the proposed SCCS-18T-EV storage cell comprises 18 transistors, i.e., 12 NMOS transistors and 6 PMOS transistors. P1-P6 and N1-N6 constitute the storage part, and N7-N12 transistors are read and write transistors. N7-N12 transistors are controlled by word lines and are connected to primary storage nodes I1-I6. When WL = 1, N7-N12 are turned ON and read/write operations are performed. When WL = 0, N7-N12 are turned OFF and the memory cell switches into hold mode (see Fig. 9-(a)).

Let us now discuss the read and write operations of the storage cell in detail. First, the write operation is discussed. Assuming that the SCCS-18T-EV cell stored 0, we need to set BL = 1 and BLN = 0 before this operation. When WL = 1, the access transistors are turned ON, then N6, P1, N4, P5, N2 and P3 are turned ON and the rest of the transistors are turned OFF, so that the memory cell forms a large feedback loop, i.e., I1 -> I6 -> I3 -> I4 -> I5 -> I2 -> I1, to store values. Note that the value 1 is stored in the storage cell (see Fig. 9-(b)). Let us now consider the read operation. Before reading 1, we set BL = 1

and BLN = 1. When WL = 1, BLN's voltage will discharge to a low level through transistors N8, N10 and N12, while BL's value remains at 1. At this time, the voltage difference between BL and BLN can be detected through a sense amplifier and thus the value is successfully read out (see Fig. 9-(c)). Note that, for the writing/reading 0 operation, a similar behavior can be observed for the cell. Figure 10 shows the layout of the proposed SCCS-18T-EV cell.
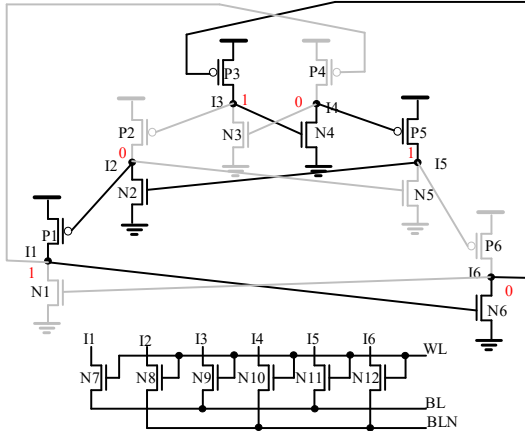

Fig. 8. The proposed SCCS-18T-EV cell.

The SRAM cell was designed/implemented using a 22nm commercial CMOS process, considering a room temperature and a 0.8V supply voltage. Figure 11 shows the simulation diagram of the read and write operations of this cell. It can be seen from the simulation diagram that the operation of writing 1 and 0 and reading 1 and 0 are correct. The correct values can also be stored in the SRAM cell through a special feedback loop.

B. Principle of SNU-Recovery

Similar to the SCCS-18T cell, it can be concluded from the symmetry of the SRAM storage cell that, I1 and I6, I2 and I5, and I3 and I4 are all symmetric points, and they have the same self-recovery behavior when soft errors occur. Therefore, the SNU-recovery of nodes I1, I2 and I3 is analyzed. We still assume that the stored value in the storage cell is 1.

Firstly, the I1 node is analyzed. When the I1 node is upset, the value of I1 changes from 1 to 0, which will lead to the opening of P4 and the closing of N6. Obviously, the values of I2, I3 and I5 will not change in a short time. P6 remains OFF, the value of node I6 remains at the original value, and N4 keeps ON (I4 outputs a strong 0). At the same time, I1 is changed from

1 to 0 temporarily, making I4 output a weaker 1, but a strong 0 of I4 will neutralize the weak 1, so that I4 remains at the original value as before (I4 = 0). N3 keeps OFF, so that values of I2 and I3 remain unchanged, then P1 turns ON and N1 turns OFF, so that I1 restores the original value 1. Due to the symmetry of the storage cell, I6 can also recover from SNU.

Let us now analyze the self-recovery of node I2. After the flipping, the value of I2 changes from 0 to 1, which will result in P1 being OFF and N5 being ON. The values of I3, I4 and I6 will not change in a short time, so P2 will remain OFF and P5 will remain ON (I5 still outputs 1, i.e., strong 1). N5 is temporarily opened due to the flipping of I2, resulting in a weak 0 as the output of I5. But a strong 1 of I5 will neutralize a weak 0, so that I5 remains at the correct value before (I5 = 1). The transistor N2 turns ON, so I2 reverts to its original correct value (I2 = 0). Due to the symmetry of the storage cell, I5 can also recover from SNU.

Finally, Let us analyze the self-recovery of node I3. After the flipping, I3's value changes from 1 to 0, which will cause P2 to open and N4 to OFF. The values of nodes I1, I5 and I6 will not change in a short time. Therefore, when P4 is OFF, the value of I4 remains at the original correct value (I4 = 0). Keeping the correct value of I4 will keep N3 OFF, while node I6's value being 0 will keep P3 ON, and thus node I3 will recover to the previous correct value (I3 = 1). Note that node I4 can also recover from SNU due to the symmetry of the storage cell.

It can be concluded from the above discussions that the proposed SCCS-18T-EV cell can recover from any SNU. Figure 12 shows the simulation results of SNU recovery for the cell. As shown in Fig. 12, when I1 = 1, we injected SNUs to nodes I1 to I6, respectively; when I1 = 0, we injected reversed SNUs to nodes I1 to I6, respectively. It can be seen from Fig. 12 that the SCCS-18T-EV cell can provide SNU recovery from any possible SNUs.

C. Principle of DNU-Recovery

Let us first analyze the DNU-recovery of node pair <I1, I3> when the SCCS-18T-EV cell stores 1. When a DNU impacts <I1, I3> and the storage cell stores 1, node I1 changes from 1 to 0, and node I3 changes from 1 to 0. As a result, P4 is ON, N6 is OFF, P2 is ON, and N4 is OFF. The value of I5 will not be affected in a short time, then N2 is ON and P6 is OFF. Since N6 and P6 are OFF, the value of I6 remains unchanged (I6 = 0), then N1 is OFF and P3 is ON. Because P2 is temporarily ON due to the flipping of I3, I2's strong 0 will neutralize its weak 1. The value of I2 remains 0, P1 is ON, N1 is OFF, and I1 is
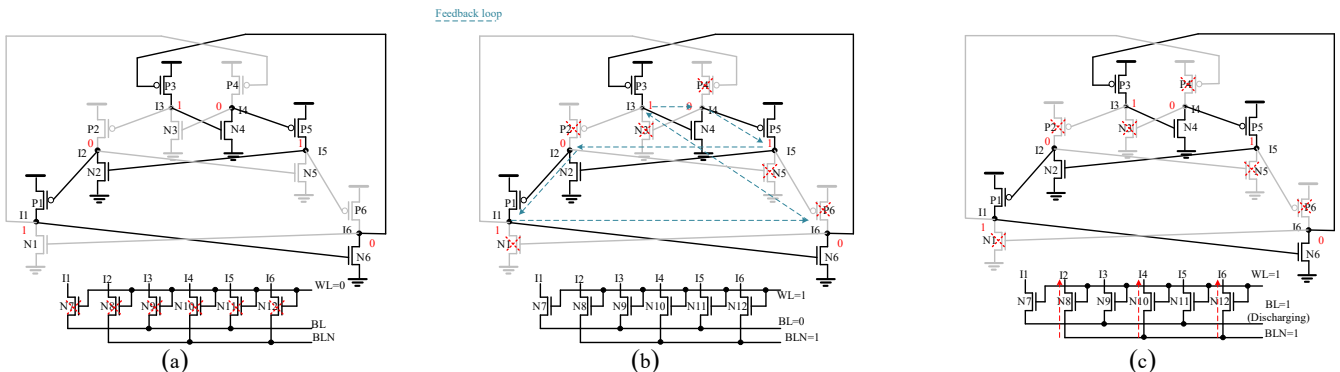

Fig. 9. Schematics of the proposed SCCS18T-EV cell's normal operations. (a) Hold '1'. (b) Write '1'. (c) Read '1'.

recovered to its original value (I1 = 1), so P3 is ON. N3 is temporarily ON due to node I4's flipping, I3's strong 1 neutralizes its weak, and node I3 recovers to its original value (I3 = 1). Therefore, node pair <I1, I3> can be self-recovered, and node pair <I4, I6> can also be self-recovered due to the symmetrical structure of the storage cell.
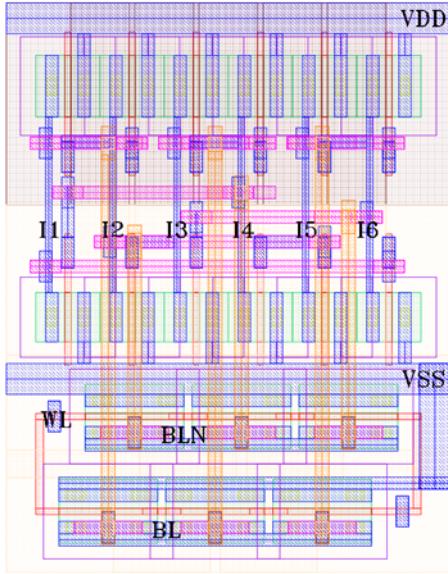

Fig. 10. Layout of the proposed SCCS-18T-EV cell.
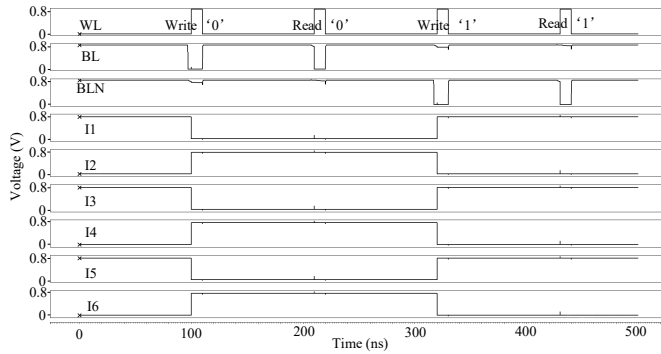

Fig. 11. Read/write operations of the proposed SCCS-18T-EV cell.

Let us now analyze the DNU-recovery of node pair <I1, I5> when the SCCS-18T-EV cell stores 1. When the storage cell stores 1, I1's value changes from 1 to 0, and I5's value changes from 1 to 0, which causes P4 to be ON, N6 to be OFF, N2 to be OFF, and P6 to be ON. The value of I3 is not affected in a short time, then P2 is OFF and N4 is ON. Since P2 is OFF and N2 is OFF, the value of I2 remains unchanged (I2 = 0), then P1 turns ON and N5 turns OFF. Transistor N4 is ON, P4 is also temporarily turned ON due to node I1's flipping, I2's strong 0 will neutralize its weak 1, the value of I4 remains 0, then N3 is OFF and P5 is ON. Since P5 is ON and N5 is OFF, node I5 can recover to its previous value (i.e., I5 = 1), then P6 is OFF. N1 is temporarily opened due to node flipping, and P1 is also ON at the same time. I1's strong 1 neutralizes its weak 0, and I1 recovers to the original value, then N6 is ON, so that I6 output 0. Therefore, node pair <I1, I5> can provide DNU-recovery. Because of the symmetry of the storage cell, node pair <I2, I6> can also provide DNU-recovery.

Let us now analyze the DNU-recovery of node pair <I1, I6> when the SCCS-18T-EV cell stores 1. When the storage cell suffers from a DNU, the value of I1 changes from 1 to 0, and the value of I6 changes from 0 to 1. As a result, P4 is ON, N6 is OFF, P3 is OFF, and N1 is ON. I2 and I5 are not affected temporarily, then P1 is ON, N5 is OFF, N2 is ON, and P6 is OFF. P1 is ON, N1 is temporarily ON due to node I6's flipping, I1's strong 1 will neutralize its weak 0, I1 node is recovered to its original value (I1 = 1), then N6 is ON. Because P6 is OFF, I6 is recovered to its original value (I6 = 0). Therefore, node pair <I1, I6> can provide DNU-recovery.
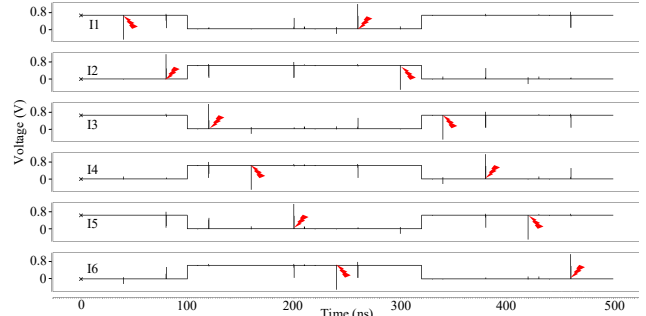

Fig. 12. SNU recovery simulation results of the SCCS-18T-EV cell.

Let us nos analyze the DNU-recovery of node pair <I2, I5> when the SCCS-18T-EV cell stores 1. When the storage cell suffers from a DNU, the value of I2 changes from 0 to 1, and the value of I5 changes from 1 to 0. In this case, P1 is OFF, N5 is ON, N2 is OFF, and P6 is ON. I3 and I4 are temporarily unaffected, then P2 is OFF, N4 is ON, N3 is OFF, and P5 is ON. N5 is temporarily ON due to node I2's flipping. I5's strong 1 will neutralize its weak 0. I5 recovers to its original value 1, and N2 is ON and P6 is OFF. Because N2 is ON and P2 is OFF, I2 also returns to its original value I2 = 0. Therefore, node pair <I2, I5> can provide DNU-recovery.

Finally, let us analyze the self-recovery of node pair <I3, I4> when the SCCS-18T-EV cell stores 1. When the storage cell suffers from a DNU, node I3 changes from 1 to 0, and node I4 changes from 0 to 1. This causes P2 to be ON, N4 to be OFF, N3 to be ON, and P5 to be OFF. I1 and I6 are temporarily unaffected, then N6 is ON, P4 is OFF, N1 is OFF, and P3 is ON. Node N3 is temporarily ON due to node I4's flipping, and I3' strong 1 will neutralize its weak 0. I3 is recovered to its original value 1, then N4 is ON, and since P4 is OFF, I4 can recover to its correct value 0. Therefore, node pair <I3, I4> can provide DNU-recovery.

When the storage cell stores 0, three node pairs can recover from DNUs. The following describes the three node pairs in detail.

Firstly, the DNU-recovery of node pair <I2, I4> is analyzed when the SCCS-18T-EV cell stores 0. When the storage cell stores 0, I2 changes from 1 to 0, and node I4 changes from 1 to 0, then P1 is ON, N5 is OFF, N3 is OFF, and P5 is ON. I6 is temporarily unaffected, thus P3 is OFF and N1 is ON. P1 is temporarily turned ON due to node I2's flipping, I1's strong 0 will neutralize its weak 1. The value of I1 remains 0, then P4 is ON and N6 is OFF. Because N3 is OFF and P3 is OFF, the value of I3 temporarily remains unchanged (i.e., I3 = 0), then P2 is ON and N4 is OFF. Since P4 is ON and N4 is OFF, node I4 recovers to its original value (i.e., I4 = 1), then N3 is ON and P5 is OFF. N2 will be turned ON temporarily due to node I5's flipping, I2's strong 1 will neutralize its weak 0, and I2 will be

recovered to its original value 1. Therefore, node pair <I2, I4> can provide DNU-recovery. Due to the symmetry of the storage cell, node pair <I3, I5> can also provide DNU-recovery.

let us now analyze the self-recovery of node pair <I2, I5> when the SCCS-18T-EV cell stores 0. When the storage cell stores 0, I2 changes from 1 to 0, and I5 changes from 0 to 1. As a result, P1 is ON, N5 is OFF, N2 is ON, and P6 is OFF. I3 and I4 are temporarily unaffected, then P2 is ON, N4 is OFF, N3 is ON, and P5 is OFF. P2 outputs a strong 1, due to node I5's flipping, N2 temporarily turns ON, I2's strong 1 will neutralize its weak 0. Therefore, I2 is recovered to its original value, then P1 is OFF and N5 is ON. Since P5 is OFF and N5 is ON, I5 can recover to its correct value 0. Therefore, node pair <I2, I5> can provide DNU-recovery.

Finally, the DNU-recovery of node pair <I3, I4> is analyzed when the SCCS-18T-EV cell stores 0. When the storage cell suffers from a DNU, I3 changes from 0 to 1, and I4 changes from 1 to 0, then P2 is OFF, N4 is ON, N3 is OFF, and P5 is ON. I1 and I6 are temporarily unaffected, then P4 is ON, N6 is OFF, N1 is ON, and P3 is OFF. P4 outputs strong 1, due to node I3's flipping, N4 temporarily ON, I4's strong 1 will neutralize its weak 0. I4 recovers to its original value 1, then P5 is OFF and N3 is ON. Since P3 is OFF and N3 is ON, I3 returns to its correct value 0. Therefore, node pair <I3, I4> can provide DNU-recovery.

When the SCCS-18T-EV cell stores 1, after simulation verification, five node-pairs <I1, I3>, <I1, I5>, <I1, I6>, <I2, I5>, and <I3, I4> can provide DNU-recovery. When the SCCS-18T-EV cell stores 0, after simulation verification, three node-pairs <I2, I4>, <I2, I5>, and <I3, I4> can provide DNU-recovery. Figure 13 shows the DNU-recovery of the proposed SCCS-18T-EV cell. Node pairs <I1, I3>, <I1, I5>, <I1, I6>, and<I2, I4> node pairs were injected with DNU errors at 50ns, 340ns, 380ns and 220ns, respectively. Node pair <I2, I5> is injected with DNU errors at 260ns and 460ns, < I3, I4> is injected with DNU errors at 300ns and 420ns. It can be seen from the simulation results that the above node-pairs can self-recover from DNUs.

It can be concluded from the above discussions that node pairs <I1, I3>, <I1, I5>, <I1, I6>, <I2, I5>, and <I3, I4> of the proposed SCCS-18T-EV cell can recover from DNUs when the cell stores 1; node pairs <I2, I4>, <I2, I5>, and <I3, I4> of the proposed SCCS-18T-EV cell can self-recover from DNUs when the cell stores 0. In summary, the SCCS-18T-EV cell has up to 8 node pairs that can provide DNU-recovery.
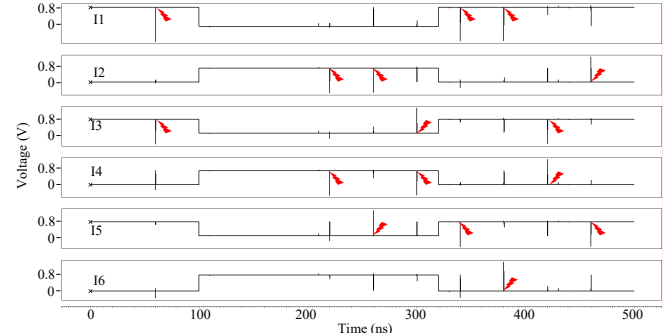

Fig. 13. DNU recovery simulation results of the SCCS-18T-EV cell.

V. COMPARISONS OF SRAMs

For fair comparisons, the reviewed SRAMs in Section II were also designed/implemented using the same conditions (a 22nm CMOS library, the room temperature and a 0.8V supply voltage) as for the proposed cells. Table I shows the reliability/overhead comparisons of all alternative SRAMs in terms of SNU-recovery (SNUR), the number of DNU-hardened node-pairs (#DHNPs), read-access time (RAT), write-access time (WAT), average power consumption as well as silicon area that was measured as in [20].

First, we discuss the reliability comparison. It can be seen from Table I that the proposed SRAMs can provide SNU-recovery as validated in Section III, but the other SNU-hardened SRAMs except Lin-12T, DNUSRM, S4P8N, and S8P4N cannot provide complete SNU-recovery because there is at least one counterexample for which the cell cannot recover from an SNU. Moreover, the 6T, NASA-13T, RHPD-12T, and

TABLE I
RELIABILITY AND OVERHEAD COMPARISON RESULTS AMONG THE UNHARDENED AND
HARDENED SRAMs UNDER 22NM CMOS TECHNOLOGY NODE

SRAM	SNUR	#DHNPs	RAT (ps)	WAT (ps)	Power (nW)	$10^{-3} \times$ Area (nm^2)
6T	×	0	25.88	3.65	5.24	4.35
NASA-13T [10]	×	0	128.67	16.39	18.92	9.07
RHPD-12T [11]	×	0	17.34	3.51	9.35	9.72
RHBD-10T [12]	×	0	21.09	3.05	11.75	6.86
RHM-12T [13]	×	1	38.11	4.28	7.89	9.28
Lin-12T [14]	√	2	37.68	3.78	9.74	9.28
DNUSRM [15]	√	16	6.63	4.71	20.86	17.42
QCCM-10T [16]	×	1	18.20	23.21	11.45	7.79
QCCM-12T [16]	×	1	12.99	4.22	10.43	8.71
S4P8N [17]	√	4	17.93	5.19	8.55	12.67
S8P4N [17]	√	4	12.94	3.67	9.26	10.65
SCCS-18T (Proposed)	√	6	8.30	4.18	15.63	13.07
SCCS-18T-EV (Proposed)	√	8	8.30	4.18	15.63	13.07

RHBD-10T SRAM cells have no DHNP, the RHM-12T, QCCM-10T, and QCCM-12T SRAMs have only one DHNP, and the Lin-12T has only two DHNPs; the S4P8N/S8P4N cells have four DHNPs. Clearly, the proposed SRAM cells both have larger #DHNPs that are 6 and 8, respectively. Therefore, the proposed SRAM cells are more reliable than the other cells except DNUSRM.

Next, we discuss the comparisons of overhead of SRAMs in Table I. In terms of RATs, the SCCS-18T and SCCS-18T-EV nearly have the best (smallest) RAT because they use six access transistors for read operations. Conversely, the NASA-13T cell has the worst (largest) RAT because of its special read transistors. In terms of WATs, the RHPD-12T, RHBD-10T, RHM-12T, and Lin-12T cells have a small WAT due to less current competition when writing values for them. Nevertheless, the NASA-13T cell has the worst (largest) WAT since it introduces more current competition when writing values. Compared with the other SRAMs, the proposed SCCS-18T and SCCS-18T-EV cells have a small WAT.

cannot tolerate SNU). The DNUSRM consumes the largest power mainly since it uses a large number of transistors to provide a high level of DNU-recovery. The RHPD-12T, S8P4N, and Lin-12T SRAMs have similar power dissipation owing to their comparable number of employed transistors as well as very similar structure. Moreover, the proposed SCCS-18T and SCCS-18T-EV SRAMs consume larger power and area since redundant transistors are used to ensure SNU/DNUs recovery as well as effective access operations. Therefore, the proposed SCCS-18T and SCCS-18T-EV SRAMs have a better trade-off between high robustness and effective access operations at the cost of slightly redundant silicon area as well as indispensable power dissipation compared with alternative SRAMs.

Finally, we quantitatively compare the overhead of SRAM cells. As in [15], the percentages of reduced costs (PRCs) can be computed to discuss the overhead of SRAM cells in a quantitative way. The PRCs of the WAT, power dissipation, and silicon area can be computed similarly as in [15] so that the average PRCs can be computed. For the brevity of the paper,
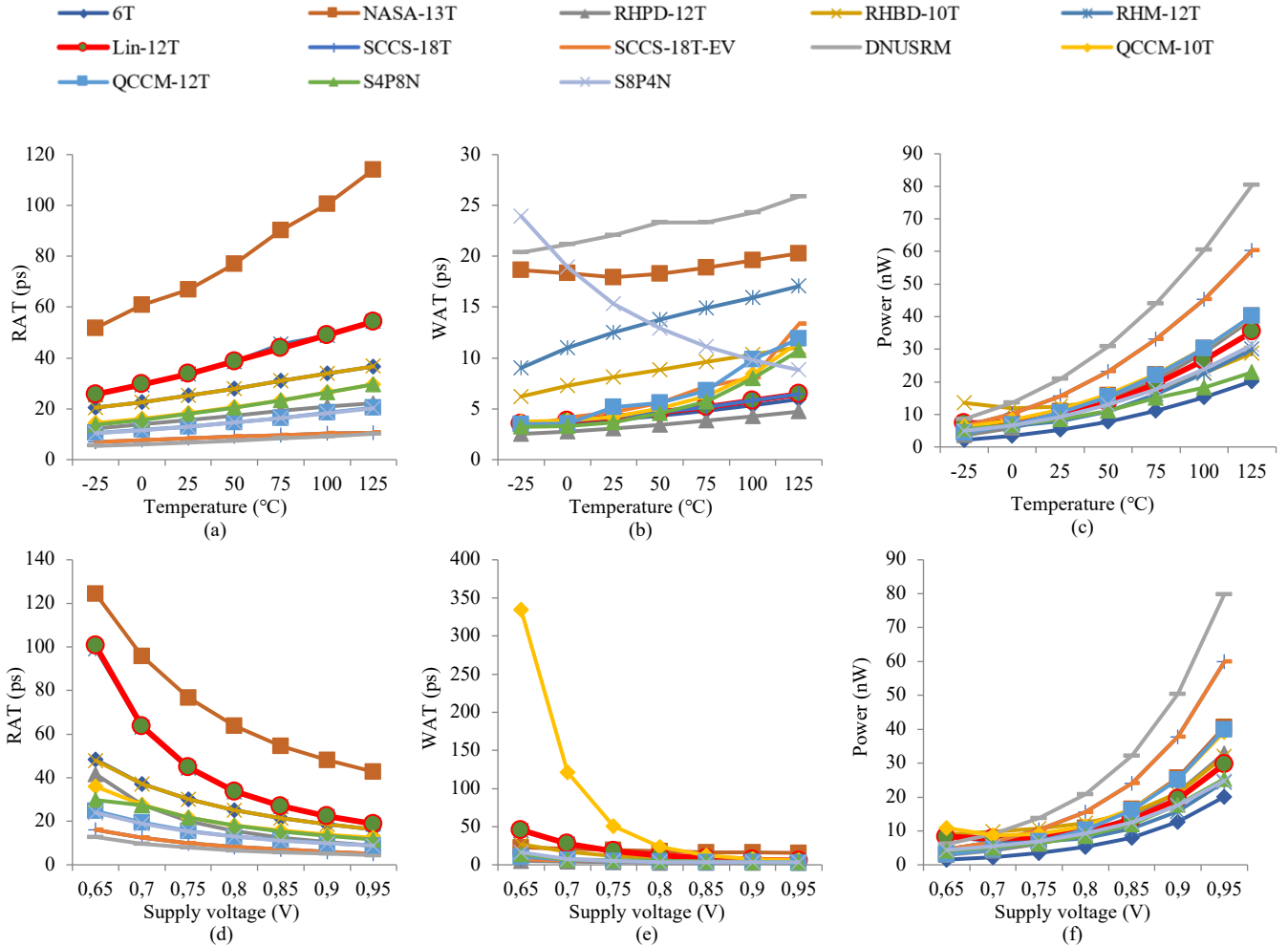

Fig. 14. Estimation results of PVT variation impacts on RAT, WAT, and power for the SRAM designs. (a) Impacts of temperature variations on RAT. (b) Impacts of temperature variations on WAT. (c) Impacts of temperature variations on power. (d) Impacts of supply voltage variations on RAT. (e) Impacts of supply voltage variations on WAT. (f) Impacts of supply voltage variations on power.

In terms of power and area, the 6T cell has the smallest power and area overhead because it only uses six transistors (so that it

we only discuss the average PRCs. Compared with alternative SRAM cells, the average PRCs of the RAT, WAT, power, and

area are 49.76%, 10.99%, -45.42%, and -36.95%, respectively. Therefore, the proposed SCCS-18T and SCCS-18T-EV cells can reduce RAT by 49.76% at the cost of 45.42% of additional power and 36.95% additional silicon area on average compared with alternative SRAM cells.

Next, we analyze the process-voltage-temperature (PVT) variation impacts on SRAM cells. Figure 14 shows the impacts of PVT variations on RAT, WAT, as well as the power consumption. Fig. 14-(a), (b), and (c) present the temperature variation (TV) impacts on RAT, WAT, as well as power, respectively. It can be seen that the RAT, WAT and power overhead of SRAMs increase as temperature increases. The RAT of RHM-12T, Lin-12T and NASA-13T are more sensitive to TVs mainly due to more decreased carrier mobility when the temperature is rising. Nevertheless, the power of our SCCS-18T and SCCS-18T-EV are less sensitive to TVs. The WAT of S8P4N and RHM-12T are more sensitive to TVs but the WAT of NASA-13T cell is less sensitive to TVs. Moreover, the power of DNUSRM, SCCS-18T and SCCS-18T-EV are more sensitive to TVs, mainly due to the introduced more current

and RHM-12T, has a low sensitivity to TVs.

Figure 14-(d), (e), and (f) present the sensitivity of RAT, WAT, and power of SRAMs to supply voltage variations (VVs). It is well known that large supply voltage of SRAMs can cause large power consumption but can reduce access time as the supply voltage increases. The RAT of Lin-12T, RHM-12T and NASA-13T cells are more sensitive to VVs but the RAT of SCCS-18T and SCCS-18T-EV are less sensitive to VVs. The WAT of QCCM-10T is more sensitive to VVs mainly because of its less read/write transistors. However, the WAT of SRAMs, such as RHPD-12T and 6T, has low sensitivity to VVs. Moreover, the power of DNUSRM, SCCS-18T and SCCS-18T-EV is more sensitive to VVs but the power of SRAMs, such as 6T and RHM-12T, is less sensitive to VVs.

Figure 15-(a), (b), and (c) present the sensitivity of RAT, WAT, and power of SRAMs to the threshold voltage variations that belongs to one important type of process variations (PV-1). It is well known that a large threshold voltage can reduce power consumption of SRAMs but can increase access time as the threshold voltage increases. The RAT of NASA-13T is the most
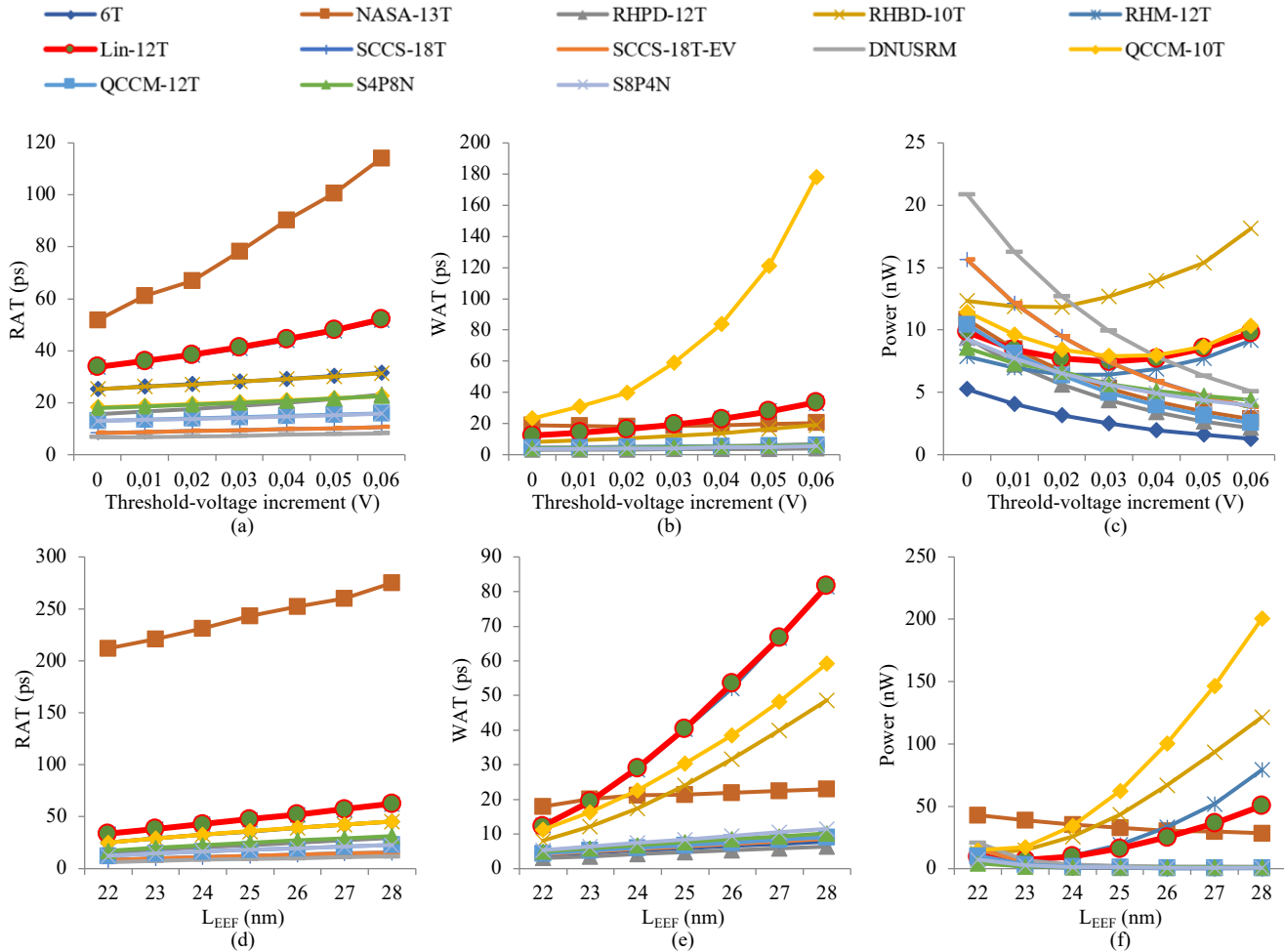

Fig. 15. Estimation results of PVT variation impacts on RAT, WAT, and power for the SRAM designs. (a) Impacts of threshold-voltage increment variations on RAT. (b) Impacts of threshold-voltage increment variations on WAT. (c) Impacts of threshold-voltage increment variations on power. (d) Impacts of L_{EEF} variations on RAT. (e) Impacts of L_{EEF} variations on WAT. (f) Impacts of L_{EEF} variations on power.

competition as well as the redundantly used access transistors; otherwise, the power consumption of SRAM cells, such as 6T

sensitive to PV-1 mainly due to its special read operation. However, the RAT of SCCS-18T and SCCS-18T-EV cells are
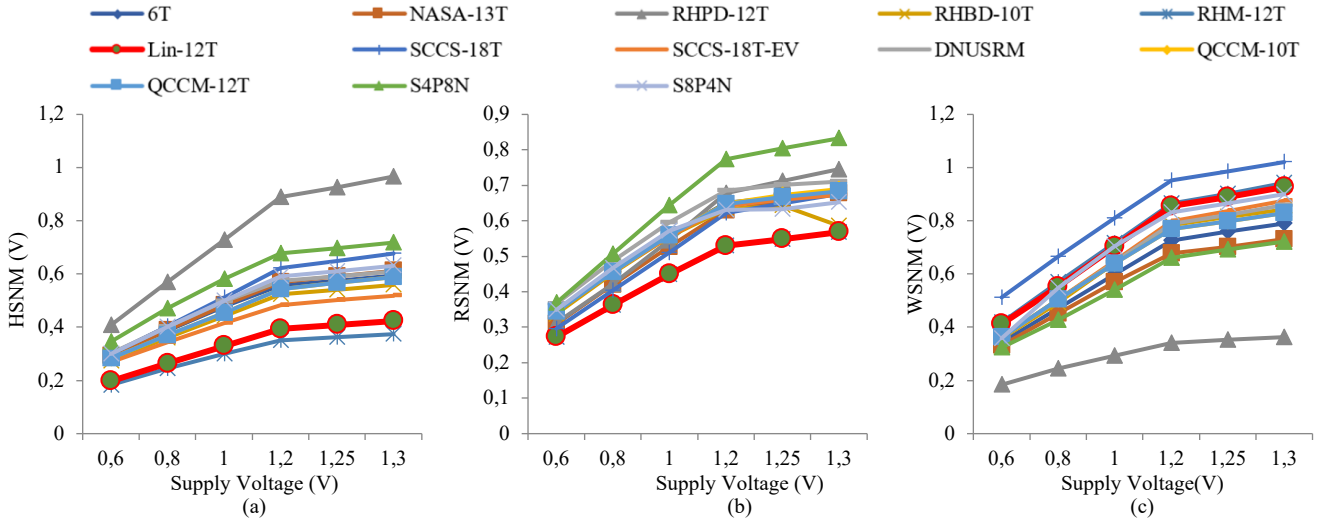
Fig. 16. SNM comparisons under different supply voltages. (a) HSNM. (b) RSNM. (c) WSNM.

less sensitive to PV-1. The WAT of QCCM-10T is more sensitive to PV-1, but the WAT of SRAMs, such as RHPD-12T, S4P8N and S8P4N, has a low sensitivity of PV-1. Moreover, the power of RHBD-10T, SCCS-18T and SCCS-18T-EV are more sensitive to PV-1, but the power of 6T cell has a low sensitivity to PV-1 mainly because the cell only uses 6 transistors.

Figure 15-(d), (e), and (f) present the sensitivity of RAT, WAT, and power of SRAMs to L_{EFF} variations that belongs to another important type of process variations (PV-2). The L_{EFF} was ranged from 22nm to 28nm. It is well-known that, the RAT and WAT increases as the L_{EFF} increases, since the threshold-voltage increases when the channel length increases. Clearly, in comparison with the other hardened SRAM cells, the RAT of the NASA-13T cell is the most sensitive to L_{EFF} variations (PV-2), whereas the RAT of the proposed SCCS-18T-EV cell is less sensitive to that. Also, the WAT of the Lin-12T cell is the most sensitive to L_{EFF} variations, whereas the WAT of the RHPD-12T cell is less sensitive to that. Moreover, the power dissipation of the RHM-12T cell is the most sensitive to L_{EFF} variations, and the power dissipation of the S4P8N, S8P4N, and QCCM-12T cells are less sensitive to L_{EFF} variations. In summary, the proposed SRAM cells have moderate or less sensitivity to PVT variations.

To evaluate stability of SRAMs in normal operations, static noise margin (SNM) needs to be measured. Figure 16 shows the SNM evaluation results under a series of supply voltages. The standard supply voltage was 0.8V. The supply voltage was varied from 0.60V to 1.30V. Figure 16-(a), (b), and (c) present the sensitivity of hold SNM (HSNM), RSNM, and write SNM (WSNM) to supply voltage variations (VVs), respectively. It is well known that the HSNM, RSNM and WSNM generally increase when the supply voltage increases. The SCCS-18T-EV and RHBD-10T cells have a comparable HSNM sensitivity, but the SCCS-18T cell has a higher HSNM sensitivity. The SCCS-18T-EV cell and RHBD-10T cell also have a comparable RSNM sensitivity, but the SCCS-18T cell has a lower RSNM sensitivity. Moreover, the SCCS-18T cell has the largest

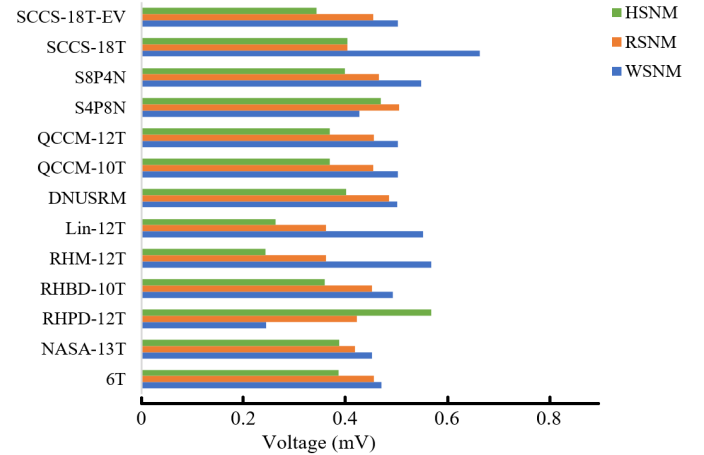WSNM sensitivity among alternative SRMAs, but the SCCS-18T-EV cell has a lower WSNM sensitivity.

Fig. 17. SNM comparison under the supply voltage of 0.8V.

Figure 17 presents the SNMs of alternative SRAMs under the standard supply voltage of 0.8V. First, the HSNM of SCCS-18T is larger than that of other SRAM cells, such as Lin-12T, RHM-12T, S8P4N, QCCM-12T, QCCM-10T, RHBD-10T, NASA-13T and 6T, but smaller than that of the RHPD-12T and S4P8N cells. The HSNM of SCCS-18T-EV cell is larger than that of SRAMs, such as Lin-12T and RHM-12T, but smaller than that of the other alternative SRAM cells. Second, the RSNM of SCCS-18T-EV is larger than that of other cells, such as Lin-12T, RHM-12T, RHBD-10T, RHPD-12T and NASA-13T, but smaller than that of SRAM cells, such as S8P4N, S4P8N, QCCM-12T, QCCM-10T, DNUSRM and 6T. The RSNM of SCCS-18T cell is larger than that of Lin-12T and RHM-12T cells, but smaller than that of the other alternative cells. Third, the WSNM of SCCS-18T-EV is larger than that of other cells, such as RHBD-10T, RHPD-12T, NASA-13T, S4P8N and 6T, but smaller than that of S8P4N, QCCM-10T, QCCM-12T, DNUSRM, Lin-12T and RHM-12T.The WSNM of SCCS-18T is larger than that of the other alternative SRAM cells. In summary, the proposed SCCS-18T and SCCS-18T-EV cells have moderate or less SNMs compared with alternative SRAM

cells.

VI. Conclusions

SRAMs have become severely susceptible to radiative-particle-striking-induced soft errors, such as SNUs and DNUs, as the CMOS technology aggressively scales down. This paper has proposed two novel SRAM cells, namely SCCS-18T and SCCS-18T-EV, with better trade-off between reliability and operation speed. The proposed cells can not only recover from all SNUs as well as part of DNUs because redundant storage transistors have been employed, but can also provide better performance because six parallel access transistors have been used. The proposed cells have moderate or even less sensitivity to PVT variations and the SNM evaluation results are also better compared to alternative SRAM cells. Therefore, the proposed SCCS-18T and SCCS-18T-EV cells can be adequately used for aerospace applications where high reliability and better performance are required.

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