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***Abstract*—Spintronic-based devices like magnetic tunnel junction (MTJ) are promising devices for space applications due to their radiation immunity, nonvolatility, and compatibility with nano-scale CMOS circuits. However, with the advancement of semiconductor technologies, CMOS peripheral circuits have become more vulnerable to soft errors, such as single-node-upsets (SNUs) and double-node-upsets (DNUs). In order to effectively tolerate DNUs caused by radiations and reduce the D-to-Q transmission delay of latches, this paper proposes a nonvolatile DNU resilient latch that mainly comprises two MTJs, two inverters and eight C-elements. Since two MTJs are used and all internal nodes are interlocked, the latch can provide nonvolatility and recover from all possible DNUs. Simulation results demonstrate the nonvolatility and DNU recovery.**

***Index Terms*—Radiation hardening, latch reliability, soft error, recovery, nonvolatile**

I. Introduction

As the dimensions of CMOS transistors scale down, the critical charge and threshold voltage of CMOS transistors are sharply reduced. Radiation effects, especially in the space environment, have become a severe reliability challenge for nano-scale CMOS circuits. CMOS integrated circuits are becoming more and more vulnerable to soft errors, and the reliability has become a critical issue for circuit designers [1].

Single-node-upsets (SNUs) and double-node-upsets (DNUs) are the major types of soft errors. With the rapid scaling of CMOS technologies, these effects dominate the radiative response of CMOS circuits. When a particle with enough energy strikes the drain terminal of an OFF-state transistor in a sequential circuit, it can change the stored data. This undesirable phenomenon is known as an SNU [2-3]. Nevertheless, in advanced nano-scale CMOS technologies, the impact of a particle striking can lead to the state changes of two nodes in a cell, which is called a DNU [4-6].

Spintronic devices, such as Magnetic Tunnel Junction (MTJ), show a great potential to overcome the problem mentioned above due to its nonvolatility, inherent radiation hardening, and compatibility with CMOS circuits [7].

MTJ is immune to particle-strike-induced soft errors because particle strikes cannot change MTJ states. However, CMOS peripheral circuits for reading and writing operations remain vulnerable to particle strikes. Therefore, the reliability of hybrid MTJ/CMOS circuits is a critical problem [8-9].

Benefiting from the feature of the MTJ and the function of the components used in hardened latch designs, this paper proposes a low-delay and DNU-recoverable spintronic retention latch. The proposed latch provides DNU recovery and nonvolatility. The nonvolatility achieved by MTJ guarantees zero standby power without losing information when the circuit is in the Power-OFF state.

The rest of the paper is organized as follows. Backgrounds of spintronic and MTJ-based circuits and the review of previous nonvolatile hardened latch designs are presented in Section II. Section III describes the proposed latch, showing its normal operation and its DNU resilience. The delay, area, and power consumption of the proposed latch are compared with the existing nonvolatile hardened latches in Section IV. Section V concludes this paper.

II. Preliminaries

A. Spintronics

MTJ is the fundamental element of spin-based circuits, which plays an essential role in the power consumption and the radiation immunity of such circuits. Figure 1 shows the schematic of a Spin Transfer Torque (STT) MTJ. It can be seen that an MTJ is mainly formed by two ferromagnetic (FM) layers (called free layer and fixed layer) separated by a thin oxide barrier. The magnetization direction of the fixed layer is fixed, while that of the free layer can change. Depending on the relative magnetization orientation (parallel or anti-parallel) of the two FM layers, an MTJ can represent two different states (the low resistance P state and the high resistance AP state). The P state and the AP state represent logic "0" and "1", respectively.

Based on the above characteristics of an MTJ, the magnetization vector of the free layer can be changed as information storage. Various ways for reconfiguring and writing data in MTJ have been proposed [10-13], depending on the magnetization method, such as spin-transfer torque (STT), voltage-controlled magnetic anisotropy (VCMA), field-induced magnetization switching (FIMS), thermally

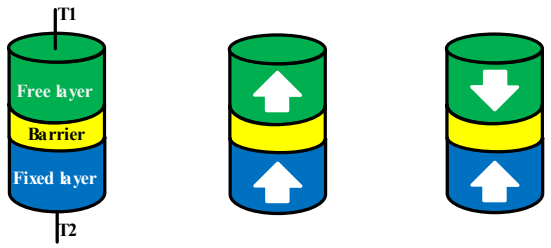

Fig. 1. Schematic of the STT-MTJ. (a) MTJ structure, (b) in the parallel state, (c) in the antiparallel state.

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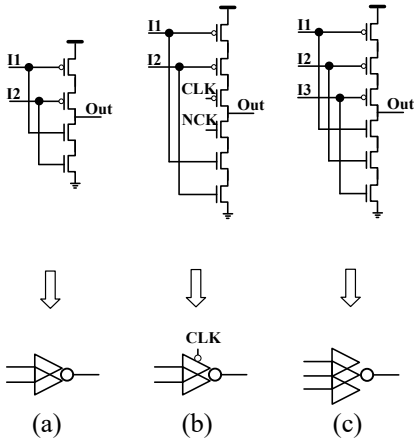

Fig. 2. Different types of C-elements. (a) 2-input, (b) Clock-gating based 2-input, (c) 3-input.

assisted switching (TAS) and spin hall assisted STT (SHE-STT).

TAS and FIMS methods suffer from the disadvantages of instability, low write performance, complex signaling, and high-power consumption; thus, they are seldom used in practical applications. Although the VCMA method can reduce switching delay and power consumption, it requires extra high voltage (e.g., 1.8V for 45nm). The use of complex signaling in the SHE-STT method increases the complexity of routing, which results in a lifetime decrease in an MTJ.

Compared with other methods, the STT method is the most reliable and feasible for MTJ reconstruction due to its lower data interference and lower switching current. This method uses a bidirectional current through the free and fixed layers of an MTJ to change the magnetization direction of the free layer, and provides two different states depending on whether the magnetization direction of the free layer and the fixed layer is consistent. If the magnetization direction of the free layer is the same as that of the fixed layer, this MTJ provides the low-resistance P state; otherwise, it provides the high-resistance AP state.

B. Previous Nonvolatile Latch Design

A C-element (CE) is one of the widely used components of hardened latch designs as shown in Fig. 2. For a CE, if the values of its inputs are the same, it behaves as an inverter; if its input values become different, its output temporarily holds the previous value. For the clock gating (CG)-based CE, its behavior can be also controlled by the clock signal CLK and the negative clock signal (NCK).

This section reviews several MTJ-based nonvolatile latches. Some of them are SNU tolerant and some are DNU tolerant. Figure 3 shows the schematics of the reviewed nonvolatile latch designs.

As shown in Fig. 3-(a), the radiation hardened nonvolatile latch proposed in [15] is designed for tolerating SNUs, mainly comprising four CEs, two inverters and two MTJs. It can fully tolerate SNUs. However, this latch cannot tolerate DNUs and it requires peripheral circuitry to generate signals (e.g., EQ)

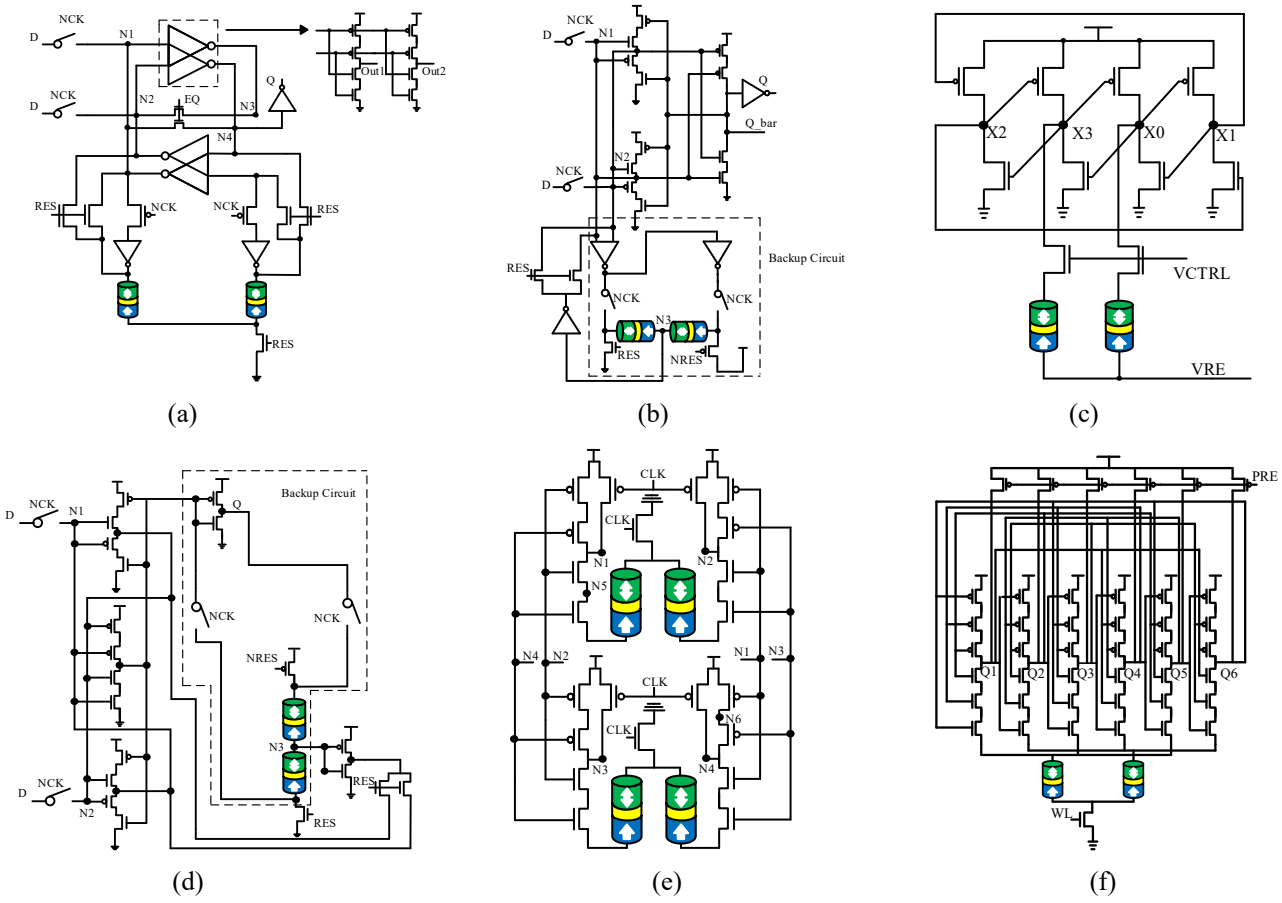

Fig. 3. Schematics of the existing nonvolatile latch designs. (a) design in [15], (b) design in [16], (c) design in [17], (d) design in [18], (e) design in [19], (f) design in [20].

required for the restore operation. These peripheral circuits increase power consumption and area overhead, as well as design complexity.

Fig. 3-(b) shows the schematic of the nonvolatile hardened latch proposed in [16]. It can provide SNU tolerance through feedback loops. However, it cannot tolerate any DNU. Moreover, two inverters used in the backup circuit increase area and power consumption due to the large transistors in the backup circuit.

It can be seen from Fig. 3-(c) that the hardened spintronic latch proposed in [17] can fully tolerate SNUs. It is a DICE [14] -based latch. Obviously, it cannot fully tolerate DNUs. It uses only two NMOS transistors for the backup and restore operations so as to reduce area overhead. However, this also leads to the disadvantage of backing up data to only one MTJ at a time, i.e., only MTJ1 or MTJ2 can be backed up at a time.

Fig. 3-(d) shows the schematic of the hardened nonvolatile latch proposed in [18]. It can also tolerate SNUs through feedback loops. However, it cannot provide DNU tolerance. Moreover, the inverter used in the backup circuit increases area and power consumption due to the large size transistor in the backup circuit similarly to the latch in Fig. 3-(b).

It can be seen from Fig. 3-(e) that the SNU tolerant nonvolatile latch proposed in [19] uses four modified C-elements to store two copies of the values, so that it can tolerate SNUs. Since the latch needs to store two sets of values, it also needs four MTJs to back up and restore the values, which greatly increases power consumption and area overhead.

It can be seen from Fig. 3-(f) that the hardened retention latch proposed in [20] can provide not only SNU tolerance but also DNU tolerance. The circuit uses six CEs to store values stably and one CE to filter errors in the output node. However, it cannot provide DNU resilience.

III. Proposed Hardened Nonvolatile Latch

A. Circuit Structure and Behavior

Figure 4 shows the schematic of the proposed radiation hardened nonvolatile latch. It can be seen that the latch comprises two parts namely DNU Recoverable Latch Part and Nonvolatile Shadow Latch Part. The DNU Recoverable Latch Part consists of four transmission gates (see the switches on the left in Fig. 4), two inverters and eight CEs. The Nonvolatile Shadow Latch Part is mainly composed of six transmission gates and two MTJs. D and Q are the input and the output of the latch, respectively. CLK and NCK are the system clock signal and negative system clock signal, respectively, and N1-N9 are the internal nodes. Note that the switches marked with NCK means that the gate-terminal of the PMOS transistor is connected to NCK and the gate-terminal of the NMOS transistor is connected to CLK. This rule is true for all latches in this paper.

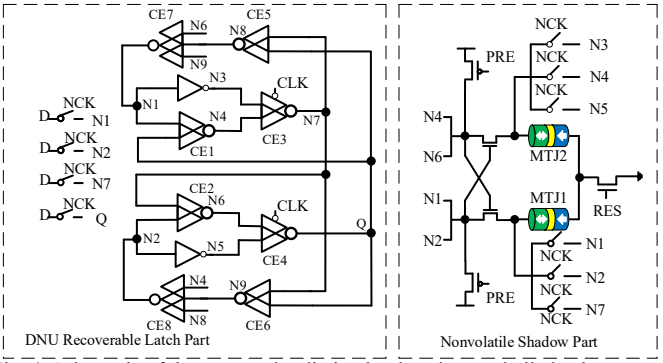

Fig. 4. Schematic of the proposed radiation hardened nonvolatile latch.

When CLK = 1 and NCK = 0, the transmission gates are ON and the latch works in transparent mode. Therefore, nodes N1, N2, N7 and Q are driven by D through the transmission gates and D = N1 = N2 = N7 = Q. When D =1, the NMOS transistors in the inverters and CE1, CE2, CE5 and CE6 can be ON, and hence the inverters and CEs output 0, i.e., N3 = N4 = N5 = N6 = N8 = N9 = 0. Note that the CG-based CE4 whose output is Q cannot output a value in this mode, and Q is only driven by D through the transmission gate between D and Q. Therefore, the latch can avoid current competition at the output (Q) of the CG-based CE to reduce power consumption and D-Q transmission delay. In summary, the latch can work correctly in transparent mode of operation.

When CLK = 0 and NCK = 1, the latch works in hold mode. In this mode, the transistors in transmission gates connected to D are OFF. Simultaneously, the clock-controlled transistors in the CG-based CEs are ON. As a consequence, nodes N1, N2, N7 and Q are no longer driven by D through the transmission gates but instead they are driven by the CEs and the CG-based CEs, respectively. At this moment, all interlocked feedback loops in the latch can be formed to retain values reliably. In summary, the latch can work correctly in hold mode of operation.

When the latch operates in hold mode, there are ten SNU cases in total because an SNU can impact every internal node N1 to N9 or the output Q of the latch. There are two types of SNUs, the first affects one input of a CE, and the second affects the input of an inverter. Let us consider the case where an SNU influences N1, leading to a glitch for an example for the first type. When N1 suffers from an SNU, the generated glitch on N1 propagates to the input of the inverter whose output is N3 and one input of CE1. Therefore, the correct value of N3 is flipped. However, CE1 can intercept the error and output the correct value at N4 so that CE3 can also intercept the error on N3 and output the correct value at N7. Note that the other nodes are not affected. N1 can recover from CE7 since the inputs of CE7 are correct. As a result, N3 can recover through the inverter. Therefore, all transistors in the latch can recover to their original correct states. Moreover, if an SNU affects N4 for the second type of SNUs, CE3 can directly intercept the error so that the inputs of CE1 are still correct and thus N4 can self-recover from the SNU. Therefore, the latch is SNU self-recoverable.

Let us now discuss the DNU self-recovery of the latch. Due to the symmetric structure of the latch, we only need to consider four possible cases, i.e., Case 1 to Case 4 in the following.

Case 1: A DNU impacts two nodes, which are both the input of an inverter and one input of a CE. The representative node-pair is only <N1, N2>. When <N1, N2> is impacted by a DNU, CE1 and CE2 can intercept the error on N1 and N2, respectively. Thus, the values of N4 and N6 are correct so that CE3 and CE4 hold their correct output values (although the

errors at N1 and N2 can propagate to N3 and N5 through inverters). Note that the other nodes are not affected. N1 and N2 can recover from CE7 and CE8, respectively. As a result, N3 and N5 can self-recover through inverters. Therefore, the latch can self-recover from the DNUs in Case 1.

Case 2: A DNU impacts two nodes, one node being both the input of an inverter and one input of a CE and another node being the only input of CEs. There are two types. The first type is that the two nodes are both the inputs of a CE, e.g., CE1. The representative node-pair is <N1, Q>. The second type is that the two nodes are the inputs of different CEs, e.g., CE1 and CE3. The representative node-pairs are <N1, N4>, <N1, N6>, <N1, N7>, <N1, N8>, <N1, N9>, <N2, N4>, <N2, N6>, <N2, Q>, <N2, N8> and <N2, N9>. Due to the symmetric structure of the latch, the representative node-pairs are only <N1, N4>, <N1, N6>, <N1, N7>, <N1, N8>, <N1, N9>, <N2, N4>, <N2, N6>, <N2, Q> and <N2, N9>. Consider the case where a DNU affects <N1, Q> for the first type. When <N1, Q> is impacted by a DNU, N3 and N4 are temporally flipped so that N7 tends to flip. However, errors <N1, Q> cannot spread to N8 and N9. Therefore, CE8 outputs a correct value at N2, i.e., the inputs of CE2 are different so that N6 holds its correct value. As a result, N1 can recover through CE7 and Q can recover through CE4. Therefore, N3 and N4 can recover through the inverter and CE1, respectively. Thus, all other affected nodes can recover from the DNU. In summary, the node pair <N1, Q> can recover from the DNU. Consider the case where a DNU influences <N1, N7> for an example of the second type. When <N1, N7> is impacted by a DNU, N3 is temporally flipped. However, the other nodes are not affected so that N1 can recover through CE7. Thus, N3 can recover directly. Finally, N7 can self-recover through CE3. Therefore, the node pair <N1, N7> can recover from the DNU. In summary, the latch can self-recover from all DNUs in Case 2.

Case 3: A DNU impacts two nodes that are only the inputs of CEs (one node is one input of a CE and another node is one input of another CE). The representative node-pairs are <N4, N7>, <N4, Q>, <N4, N6>, <N6, N7>, <N6, Q>, <N7, N8>, <N7, N9>, <Q, N8> and <Q, N9>. Due to the symmetric structure of the latch, the representative node-pairs are only <N4, N7>, <N4, Q>, <N4, N6>, <N6, N7>, <N6, Q>, <N7, N8>, <N7, N9> and <Q, N8>. We consider the case where a DNU affects <N4, N7> for example. When <N4, N7> is impacted by a DNU, errors cannot propagate to the other nodes. Finally, N4 can recover through CE1 and N7 can recover through CE3. In summary, the latch can self-recover from all DNUs in Case 3.

Case 4: A DNU impacts two nodes that are the inputs of a CE except the node-pairs in Cases 1 through 3. The representative node-pairs are <N4, N8>, <N4, N9>, <N6, N8>, <N6, N9> and <N7, Q>. Consider the case where a DNU affects <N7, Q> for an example. When <N7, Q> is impacted by a DNU, N8 and N9 are flipped. However, N4 and N6 hold their correct values since N1 and N2 are not influenced. Therefore, CE7 and CE8 can intercept the errors and the other nodes are not affected. As a result, N7 and N8 can recover through CE3 and CE4, respectively. In summary, the latch can self-recover from all DNUs in Case 4.

When CLK = 1 and NCK = 0, the Nonvolatile Shadow Part works in backup mode. The current flowing through the MTJs changes the relative direction of magnetization of the free layer and the fixed layer. Then, the values can be stored in the two MTJs. For example, when N1 = N2 = N7 = 1 and N3 = N4 = N5 = 0, the current flows from the free layer of MTJ1 to its fixed layer, and then from the fixed layer of MTJ2 to its free layer. The relative direction of magnetization of the free layer and the fixed layer in MTJ1 is anti-parallel and the relative direction in MTJ2 is parallel so that the state of MTJ1 is AP and the state of MTJ2 is P. The six transmission gates in the Nonvolatile Shadow Part are used to increase the current for the purpose of switching the MTJ state at a lower voltage.

When the power supply is reconnected, the circuit starts to restore values. When PRE = 0, N1, N2, N4, N6 can be charged to VDD. At this time, the circuit does not form any feedback loop (CLK = 1), so that the four nodes cannot be affected by other nodes. When RES = 1, the fixed layer of MTJ1 and MTJ2 connects to the ground. The nodes connected to the MTJ with the P state are discharged faster than the nodes connected to the MTJ with the AP state because the AP state has a higher resistance than the P state. As a result, with the different states of the two MTJs, <N1, N2> and <N4, N6> have different logic states. For example, when MTJ1 is AP and MTJ2 is P, the resistance of MTJ2 is lower than that of MTJ1. Therefore, N4 and N6 are discharged faster than N1 and N2. When N4 and N6 discharge until they are unable to open the NMOS to which they are connected, N1 and N2 stop discharging while N4 and N6 continue to discharge. As a result, N1 = N2 = 1 and N4 = N6 = 0. When CLK = 0, the feedback loops in the circuit are formed, and the other nodes successively obtain their correct values.

B. Simulation Results

The SNU/DNU resilience of the proposed radiation hardened nonvolatile latch was demonstrated by simulations. The simulations were performed by using an advanced 45 nm CMOS technology with the Synopsys HSPICE tool. The supply voltage was set to 1.0 V, and the working temperature was set to the room temperature. The transistor sizes in the latch design are as follows: (a) With regard to the normal CEs and inverters, the PMOS transistors had W/L = 90nm/45nm and the NMOS transistors had W/L = 45nm/45nm; (b) With regard to the CG based CEs, the PMOS transistors had W/L = 120nm/45nm and the NMOS transistors had W/L = 45nm/45nm.

In order to verify the error-free operations of the proposed latch, numerous simulations were conducted without any error injection. Figure 5 shows the simulation results without any error injection of the proposed nonvolatile latch. These results demonstrate the correct operational capability of the proposed radiation hardened nonvolatile latch.

Figure 6 shows the simulation results for the SNU injections of the proposed nonvolatile latch. In order to validate the SNU recovery ability, an SNU with sufficient charge was injected to N1 up to N9 as well as Q, respectively. It can be seen from the figure that any node can be restored to its original correct value, confirming that the latch is SNU self-recoverable.

The simulation results for the key DNU injections for <N1, N2>, <N1, Q>, <N1, N4>, <N1, N6>, <N1, N7>, <N1, N8>,

<N1, N9>, <N2, N4>, <N2, N6>, <N2, Q> and <N2, N9> of the proposed nonvolatile latch are shown in Fig. 7. It can be seen that, at 2.2, 2.4, 2.6, 2.8, 4.2, 4.4, 4.6, 4.8, 6.1, 6.3 and 6.5 ns, two SNUs with sufficient charge were injected to the above-mentioned node pairs to simulate DNUs, respectively.

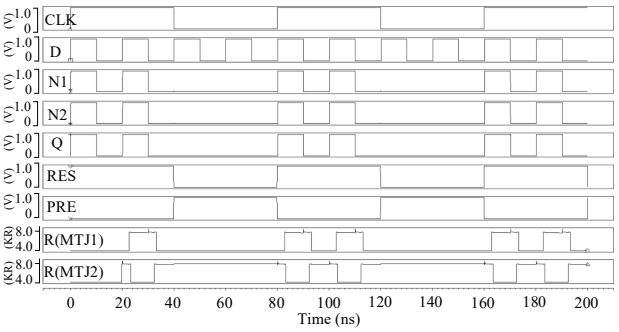

Fig. 5. Simulation results without any error injection of the proposed nonvolatile latch.

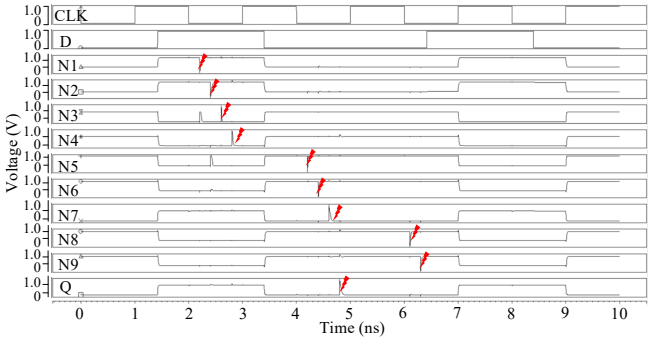

Fig. 6. Simulation results for the SNU injections of the proposed nonvolatile latch.

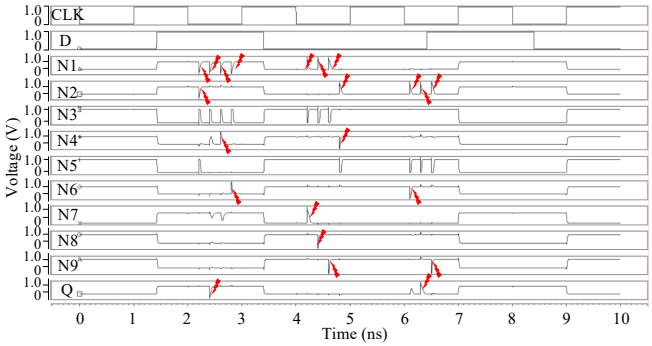

Fig. 7. Simulation results for the key DNU injections for <N1, N2>, <N1, Q>, <N1, N4>, <N1, N6>, <N1, N7>, <N1, N8>, <N1, N9>, <N2, N4>, <N2, N6>, <N2, Q> and <N2, N9> of the proposed nonvolatile latch.

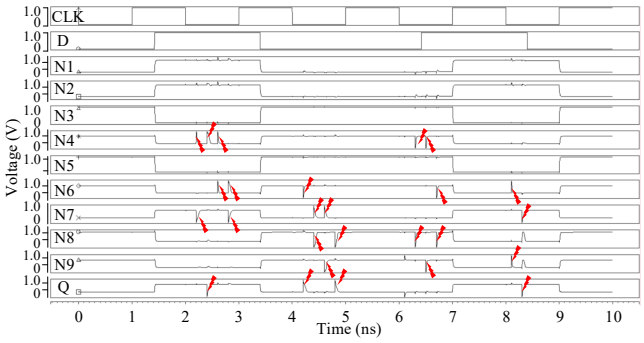

Fig. 8. Simulation results for the key DNU injections for <N4, N7>, <N4, Q>, <N4, N6>, <N6, N7>, <N6, Q>, <N7, N8>, <N7, N9>, <Q, N8>, <N4, N8>, <N4, N9>, <N6, N8>, <N6, N9> and <N7, Q> of the proposed nonvolatile latch.

It is clear that the impacted node-pairs can rapidly recover from DNUs.

The simulation results for the DNU injections at key node pairs <N4, N7>, <N4, Q>, <N4, N6>, <N6, N7>, <N6, Q>, <N7, N8>, <N7, N9>, <Q, N8>, <N4, N8>, <N4, N9>, <N6, N8>, <N6, N9> and <N7, Q> of the proposed nonvolatile latch are shown in Fig. 8. It can be seen that, at 2.2, 2.4, 2.6, 2.8, 4.2, 4.4, 4.6, 4.8, 6.1, 6.3, 6.5, 8.1 and 8.3 ns, two SNUs with sufficient charge were injected to the above-mentioned node pairs to simulate DNUs, respectively. It is clear that the influenced node-pairs can rapidly recover from DNUs.

Note that, in all the above simulations, we used a controllable double exponential current source model to perform all the DNU injections [21]. The worst-case injected charge was up to 45fC. The time constants of the rise and fall of the current pulse were set to 0.1 ps and 3.0 ps, respectively. In summary, the above-mentioned simulation results strongly demonstrate the self-recoverability from SNUs/DNUs of the proposed nonvolatile latch.

IV. Comparison and Evaluation

In this section, the proposed latch is compared with the radiation hardened nonvolatile latch designs reviewed in Section II to further assess its reliability and overhead. For a fair comparison, the reviewed latches were also designed using the same conditions, i.e., the same working temperature, the same supply voltage, and the same CMOS technology.

First, the reliability comparisons among the radiation hardened nonvolatile latch designs are shown in Table I. We can see that the top four latches can tolerate SNUs and have both backup ability and restore ability, but cannot tolerate DNUs. The nonvolatile latch proposed in [18] can provide SNU tolerance and restore ability; however, it cannot tolerate DNUs. It also cannot provide backup ability because it is designed as a pre-charge differential sense amplifier to recover values from the MTJs only. The nonvolatile latch proposed in [20] is also designed as a pre-charge differential sense amplifier so that it cannot provide backup ability but can provide restore ability. It uses many 3-input CEs to form feedback loops so that it can provide DNU tolerance. However, it cannot self-recover from DNUs. Regarding our proposed nonvolatile latch, it can provide backup ability and restore ability. Moreover, it can not only tolerate DNUs, but also recover from DNUs. In summary, the proposed latch can provide better fault tolerance.

TABLE I
Reliability Comparison among the Radiation Hardened Nonvolatile Latch Designs

Latch	SNU Tolerance	DNU Tolerance	DNU Resilience	Backup Ability	Restore Ability
Design in [15]	√	×	×	√	√
Design in [16]	√	×	×	√	√
Design in [17]	√	×	×	√	√
Design in [18]	√	×	×	√	√
Design in [19]	√	×	×	×	√
Design in [20]	√	√	×	×	√
Proposed	√	√	√	√	√

***Note that, there is no existing latch that can provide DNU resilience and nonvolatile function simultaneously.**

Let us now discuss the overhead comparisons among the SNU and/or DNU hardened nonvolatile latch designs. These

designs are compared in terms of D to Q transmission delay, i.e., the average rise and fall delays of D to Q, silicon area that is obtained through the model in [21] and power dissipation. Note that the power dissipation denotes the average power dissipation (dynamic and static).

Table II shows the overhead comparison among the radiation hardened nonvolatile latch designs. It can be seen that the proposed latch has the smallest D to Q transmission delay. This is because there is a high-speed transmission path used from D to Q; and the clock gating is also used at the CE whose output is Q to reduce the current competition at Q. The latch proposed in [20] has the largest delay among these latch designs mainly because there are many elements from D to Q. The latch proposed in [18] needs to store two sets of values so that it needs four MTJs to back up and restore the values. In order to provide completely latch self-recovery from DNUs to obtain better fault tolerance for the proposed latch, slightly more elements are used in the latch in comparison with the other latches. Hence, the proposed latch has larger area and higher power consumption. It can be seen that the area and power consumption of the proposed latch are close to the DNU tolerant latch proposed in [20]. However, the proposed latch has better fault tolerance and smaller delay. Note that the proposed latch can use clock gating to significantly reduce the power consumption at the cost of larger area overhead. In summary, the proposed latch can provide better trade-off between reliability and overhead.

TABLE II
OVERHEAD COMPARISON AMONG THE RADIATION HARDENED NONVOLATILE LATCH DESIGNS

Latch	D-Q Delay (ps)	10^{-4}×CMOS Area (nm^2)	MTJ Counts	Power (μW)
Design in [15]	54.37	10.13	2	19.26
Design in [16]	37.56	9.52	2	12.50
Design in [17]	6.72	4.34	2	11.84
Design in [18]	43.78	8.30	2	12.37
Design in [19]	51.84	6.89	4	16.13
Design in [20]	98.53	15.39	2	18.34
Proposed	3.71	16.87	2	20.46

***Note that, the first-ever DNU resilience with nonvolatile function for the proposed latch is at the cost of indispensable CMOS area and power.**

V. CONCLUSIONS

In this paper, we have proposed a novel high performance (low delay) and DNU self-recoverable nonvolatile latch design. Compared with other SNU/DNU tolerance latches, the proposed nonvolatile latch provides better fault tolerance and has the smallest delay to improve performance. Because there is no MTJ in the main data path of the proposed latch circuit, the MTJ switching delay cannot affect the D-to-Q delay of the proposed latch circuit. Simulation results have demonstrated the backup and restore ability, the DNU recovery and low delay of the proposed latch so that the latch can be applied to high performance and aerospace that require radiation hardening.

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