MCTHSL: 4x4-Device-Matrix-Based Cost-Optimized TNU-Recovery HIS-Insensitive and SET-Filterable Latch for Aerospace Applications

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***Abstract*— This paper proposes a novel 4×4-device-Matrix-based Cost-optimized Triple-node-upset (TNU)-recovery High-impedance-state (HIS)-insensitive and Single-event-transient (SET)-filterable Latch, namely MCTHSL, designed for aerospace applications. The MCTHSL latch comprises a 4×4-device matrix to completely provide TNU recovery and thus it is HIS-insensitive. The input of a Schmitt Trigger (ST) is split to create an input-split ST, namely ISST, to simultaneously provide the functions of a C-element (CE), a SET-filtering device and a delay element. The matrix comprises 15 mutually interlocking 2-input CEs as well as an ISST to store values, recover from TNUs and filter SETs with HIS-insensitivity and cost-optimization. Simulation results demonstrate the above-mentioned features as well as cost reduction (in comparison with state-of-the-art TNU-recovery latches) of the proposed MCTHSL latch.**

I. Introduction

The soft error rate of circuits and systems is rapidly increasing in nano-scale *Complementary Metal Oxide Semiconductor* (*CMOS*) technologies due to the continuous down scaling of transistor feature sizes [1]. *Single-event transients* (*SETs*), *single-node upsets* (*SNUs*), *double-node upsets* (*DNUs*), *and triple-node upsets* (*TNUs*) are typical soft errors. DNUs and TNUs are called *multiple-node-upsets* (*MNUs*). When a particle, such as a neutron, a proton, a heavy ion, an alpha particle, or an electron [2], with enough energy hits the diffusion region of a reverse bias transistor in a combinational circuit, a SET can occur at the output of the impacted gate [3]; when the particle hits the transistor in a storage element, a SNU can occur at the drain of the affected transistor. Moreover, in nano-scale CMOS technologies, aggressively down-scaled transistor sizes and very large-scale integration may cause the strike of a particle to induce single-event charge collection to affect double or triple adjacent nodes, resulting in a DNU or a TNU [4-5]. Unhardened electronic devices are vulnerable to soft errors, making them unsuitable for aerospace applications. Therefore, it is of great significance to design highly reliable integrated circuits that are protected against soft errors for reliable computing in aerospace environements.

For the purpose of radiation hardening of basic storage elements, researchers have mainly focused on the design of flip-flops [5-6], memory cells [7-8], and latches [4, 9-27]. This paper mainly focuses on latch designs. If a latch cannot tolerate node-upsets, node-upsets can lead to data corruption of the latch when it works in hold mode of operation and thus the wrong value kept in the latch may be used by the fan-out elements of the latch. A latch that can tolerate node-upsets may not be able to provide node-upset-recovery. A latch that cannot provide node-upset recovery may suffer from the *high-impedance-state* (*HIS*) problem especially when it uses a *C-element* (*CE*) as its output stage device makes so that its output is floating to an undetermined value when time is flawing. An SET can propagate from the input to the output of an SET-non-filtering latch that works in transparent mode of operation and thus the SET may impact the fan-out elements of the latch. Among the above-mentioned latches, some can tolerate SNUs [9-14, 16, 26-27], some can simultaneously tolerate SNUs and DNUs [15, 17-18, 21, 23-24] and some can simultaneously tolerate SNUs, DNUs, and TNUs [19-20, 22, 25]. Note that some of these hardened latches are SET filterable [13, 16, 18, 22]. Furthermore, although the latches can tolerate some types of node upsets, some of them cannot provide complete recovery from node upsets. The reason is that at least one or more of their nodes cannot recover from node-flipping, though they can still output valid values. Among the SNU-tolerant latches, only some [14, 27] can provide SNU-recovery. Among the DNU-tolerant latches, only some [17-18, 23-24] can provide DNU-recovery. Among the TNU-tolerant latches, only one [25] can provide TNU-recovery; however, its area is large and it cannot filter SETs, making it still unsuitable for robust computing.

Reports in [28] indicated that multiple-bit-upsets are increasing so that MNUs can also increase as technology scales down. Note that it is very difficult to precisely calculate the probability of TNU occurrence since many types of actual parameters are needed. Hence, we qualitatively discuss the requirement of TNU-recovery design. Due to charge-sharing, a TNU can be induced through the strike of a high-energy radiative particle. The detailed reason is that, if an advanced circuit is highly integrated and fabricated with an extremely small process node, e.g., 7 nm, more transistors and nodes would be located much closer, so that the probability of an event like that will severely increase. As mentioned above, HIS and SET issues can also severely impact latch reliability. This motivates us to propose a TNU-recoverable HIS insensitive and SET filterable latch at optimized overhead (area, delay, power).

In this paper, a *4×4-device-Matrix-based Cost-optimized TNU-recovery HIS-insensitive and SET-filterable Latch* (*MCTHSL*) is proposed for aerospace applications. The latch can recover from any possible TNU and thus it is insensitive to HIS. The *input-split Schmitt Trigger* (*ISST*) is created to

simultaneously provide the functions of a CE and a *Schmitt Trigger* (*ST*). The matrix of the latch comprises 16 mutually interlocking 2-input devices, i.e., 15 CEs and one ISST, to store values, recover from TNUs and filter SETs with HIS-insensitivity and cost-optimization. Simulation results demonstrate the TNU-recovery, SET-filtering and cost (area, delay, power) reduction (in comparison with state-of-the-art TNU-recovery latches) of the proposed MCTHSL latch.

The rest of the paper is organized as follows. Section II reviews typical soft-error-hardened latches. Section III describes the structure, working principles, and simulations of the proposed latch. Section IV presents comparative results with existing latches. Section V concludes the paper.

II. Typical Soft-Error-Hardened Latches

In many soft-error-hardened latches, CEs and STs are widely used. Figure 1 shows their structure. Figures 1-(a) to (d) show different CEs and Fig. 1-(e) shows the ST. A CE works as an inverter if its inputs have the same value and as an error-interceptor (i.e., its output enters into HIS and temporarily retains its previous value) if its input values become different. A *clock-gating* (*CG*)-based CE is also controllable by *system clock* (*CLK*) and *negative system clock* (*NCK*) signals. The ST works as an inverter with a large delay due to its hysteresis property. The ST can filter SETs. For example, if input I1 in Fig. 1-(e) is 0 with a positive (i.e., 0-1-0) SET, the correct states of transistors MP1, MP2, MP3, MN1, MN2 and MN3 are ON, ON, OFF, OFF, OFF, ON, respectively, and the drain terminal of MN3 is 1. When the positive SET arrives at I1, all transistors tend to temporarily change their correct states. However, when MN1 tends to turn ON due to the SET, the drain terminal of MN1 has to compete with that of MN3, which needs a period of time. During this period of time, if the SET is not very large, there is no time to pass the wrong value to the ST's output. This means that the SET is masked/filtered.

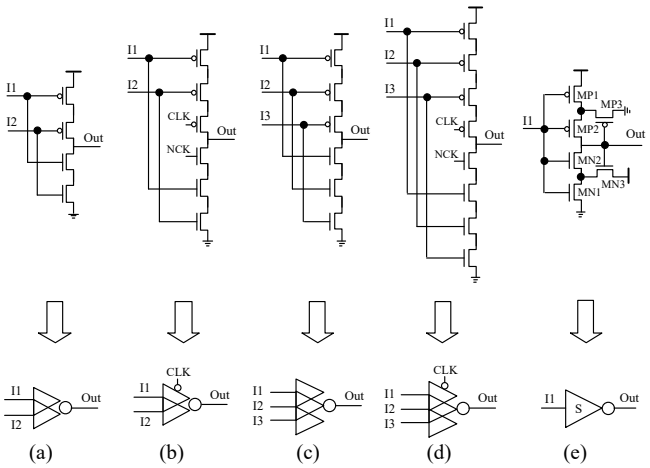

Fig. 1. CEs and ST. (a) 2-input CE, (b) clock-gating based 2-input CE, (c) 3-input CE, (d) clock-gating based 2-input CE, and (e) ST.

Figure 2 shows the structures of existing hardened latches, such as the *Low-cost Soft-Error Hardened* (*LSEH*) [13], *Dual Interlocked storage CEll* (*DICE*) [14], *High performance, Low-cost, and Double node upset Tolerant Latch Enhanced Version* (*HLDTL-EV*) [15], *High Robust and Low Cost* (*HRLC*) [16], *Double-Node-Upset-Resilient Latch* (*DNURL*) [17], *TNU-Tolerant Latch* (*TNUTL*) [19], *Low Cost and TNU completely Tolerant* (*LCTNUT*) [20], *HIS-Insensitive TNU-Tolerant and SET-Filtering Latch* (*HITTSFL*) [22], *Triple-Node-Upset self-Recoverable Latch* (*TNURL*) [25] latch designs. Note that, the switches in Fig. 2 represent the *transmission gates* (*TGs*). For example, each switch marked with NCK means that the gate terminal of the pMOS transistor is connected with NCK and the

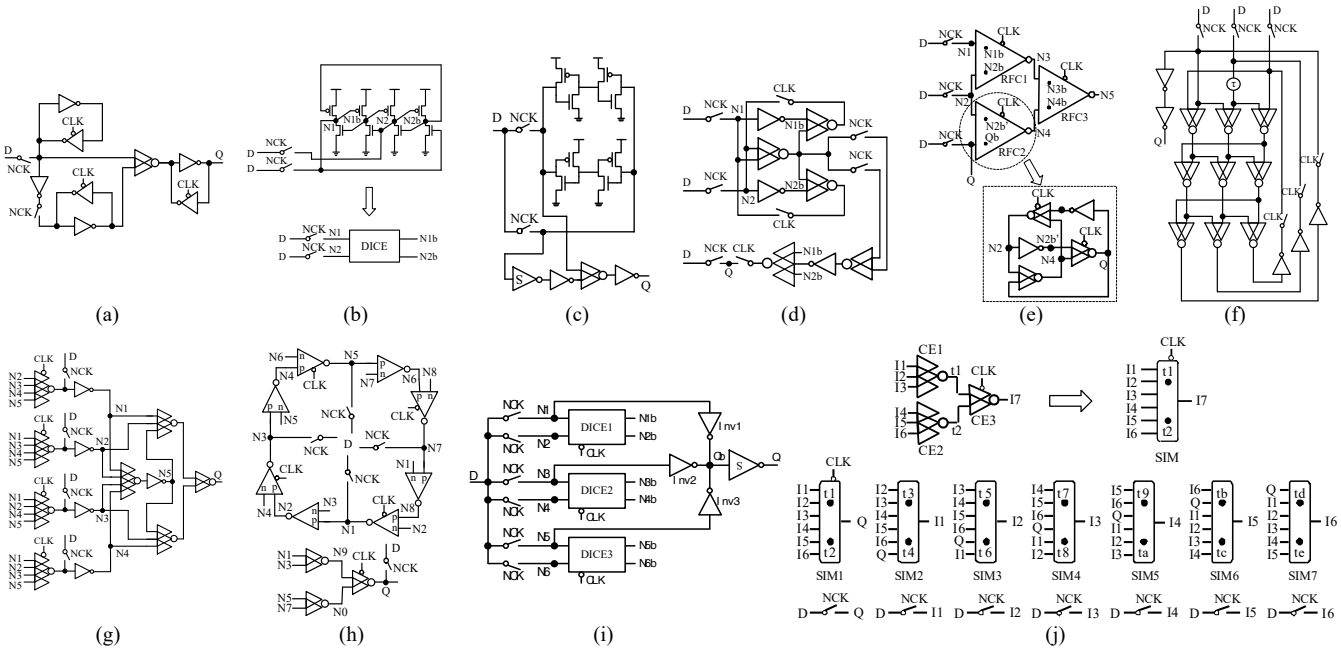

Fig. 2. Existing hardened latches. (a) LSEH [13], (b) DICE [14], (c) HRLC [16], (d) HLDTL-EV [15], (e) DNURL [17], (f) THLTCH [18], (g) TNUTL [19], (h) LCTNUT [20], (i) HITTSFL [22], and (j) TNURL [25].

gate terminal of the nMOS transistor is connected with CLK. This rule applies for all latches in this paper.

The LSEH in Fig. 2-(a) uses two keepers feeding the CE to tolerate SNUs, uses the CE with a delayed input to filter SETs, and uses a keeper at the output to avoid sensitivity to HIS. The DICE in Fig. 2-(b) uses interlocked feedback loops to provide recovery from SNUs; thus it is HIS-insensitive. The HRLC in Fig. 2-(c) uses four input-split inverters to store values, uses an output-level CE to tolerate SNUs, and uses an ST to filter SETs (simultaneously create input delay for the CE to filter SETs). However, these latches cannot tolerate DNUs.

The HLDTL-EV in Fig. 2-(d) uses the top module to provide SNU-recovery and uses a 3-input CE to tolerate DNUs; however, it is sensitive to HIS. The DNURL in Fig. 2-(e) uses three interlocked RFC cells that can provide SNU-recovery to recover from any possible DNU. The THLTCH in Fig. 2-(f) uses nine interlocked CEs to recover from any possible DNU and uses a CE with a delayed input (the delay element marked with τ is employed) to filter SETs. However, these latches cannot tolerate TNUs.

The TNUTL in Fig. 2-(g) uses many multiple-input CEs to tolerate TNUs. However, its overhead is large. To reduce overhead, the LCTNUT in Fig. 2-(h) uses input-split inverters to create a storage module and uses multiple levels of CEs to intercept errors. The HITTSFL in Fig. 2-(i) proposes a novel idea, i.e., triple modular redundancy (TMR) without a voter, to tolerate TNUs. When the latch suffers from a TNU, only the upmost DICE can completely crash so that Qb has a value close to the correct value and then the ST can strength the value to a correct value. The latch can filter SETs through the ST. The last latch uses many interlocked multiple-level-CEs to intercept errors so that it can provide TNU recovery; however, its area, delay and power overhead is large.

III. Proposed Hardened Latch Design

A. Circuit Structure and Behavior

Figure 3 shows the structure of the proposed MCTHSL latch. The latch consists of eight switches/TGs and one 4×4-device matrix that consists of one ISST and 15 interlocking 2-input CEs (i.e., CE1 to CE15). As shown in Fig. 3, the matrix consists of four levels (columns) and each level consists of four devices. It can be seen that the outputs of the devices of each level feed the inputs of the devices of the next level. For each device, its output feeds a single input of the devices in the next level, respectively. In the proposed latch, D is the input, Q is the output, A1 to A4, B1 to B4, C1 to C4 and D1 to D4 are the internal nodes, respectively.

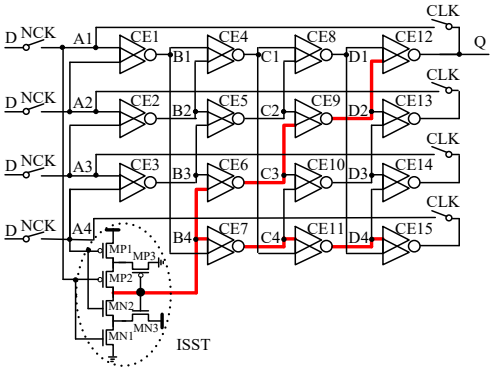

Fig. 3. Structure of the proposed MCHTSL latch. Note that the red bold path is delayed for SET filtering of subsequent CEs.

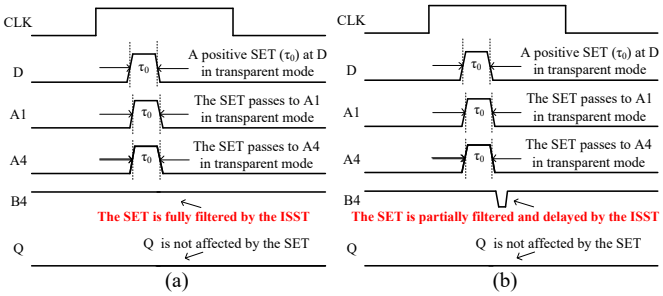

Fig. 4. Positive-SET filtering cases of the proposed MCHTSL latch. (a) Fully filtering of a positive SET pulse, (b) partially filtering of a positive SET pulse.

In transparent mode (CLK = 1 and NCK = 0), the switches connected to D are ON and the other switches are OFF. Hence, the D-value can pass to the internal nodes of the latch but the outputs of the last column of CEs cannot feed A1 to A4 (due to the OFF state of the switches on the right side of Fig. 3). Therefore, the proposed latch can be properly initialized, and Q can be determined by D. Note that, in this mode, a SET (positive or negative) at D can be filtered. Figure 4 shows the positive-SET filtering cases of the proposed MCHTSL latch.

Let us assume that a positive SET arrives at D, so that this SET can pass to A1 to A4. If the SET (width and amplitude) is small, the SET can be fully filtered by the ISST (see B4 signal in Fig. 4-(a)). Because the ISST also behaves as a delay element

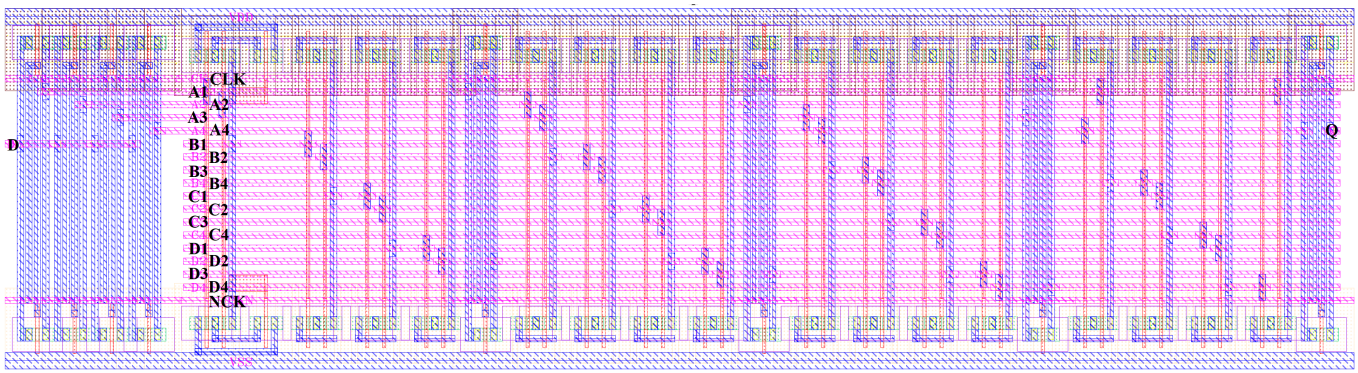

Fig. 5. Layout of the proposed MCHTSL latch design.

due to its larger delay, the red bold path in Fig. 3 is delayed for SET filtering of subsequent CEs. This means that the SET arriving at A1 to A3 (and thus B1 to B3, C1 to C2, and D1) can be filtered by the CEs (such as CE6, CE7, CE9, and CE11) that have inputs with delay differential. If the SET (width and amplitude) is not small, the SET can be partially filtered by the ISST (see B4 signal in Fig. 4-(b)). Because the ISST also behaves as a delay element due to its larger delay, the red bold path in Fig. 3 is delayed for SET filtering of subsequent CEs. This means that the SET arriving at A1 to A3 (and thus B1 to B3, C1 to C2, and D1) can be filtered by the CEs (such as CE6, CE7, CE9, and CE11) that have inputs with delay differential. Note that, if the SET is very large, it cannot be sufficiently filtered.

In hold mode (CLK = 0 and NCK = 1), the switches connected to D are OFF and the other switches are ON. Hence, the outputs of the last column of CEs can feed the inputs of the first column of CEs and the ISST. This means that, using 16 interlocking devices, many feedback loops can be solidly constructed to robustly hold correct values. Note that, in this mode, the latch can recover from any possible TNU. Also note that the ISST has the function of a CE to intercept errors so that we can consider that the latch has 4×4 CEs.

Let us now discuss the TNU-recovery principle of the proposed latch. Clearly, the outputs of each column of devices in the latch cannot be totally flipped when the latch suffers from a TNU. For example, when B1 to B3 are impacted by a TNU, the errors can propagate to C1 and C2 through CE4 and CE5, respectively, then propagate to D1 through CE8 only. However, in this case, there is no device that has two impacted inputs at the bottom of Fig. 3 and thus there is also no CE that has two impacted inputs at the last column of Fig. 3. This means that the outputs of the last column of CEs are correct so that A1 to A4 are correct. Therefore, the TNU error can be removed. Note that, when A1 to C1 (or any combination of the other three nodes) are impacted by a TNU, the same conclusion can be drawn.

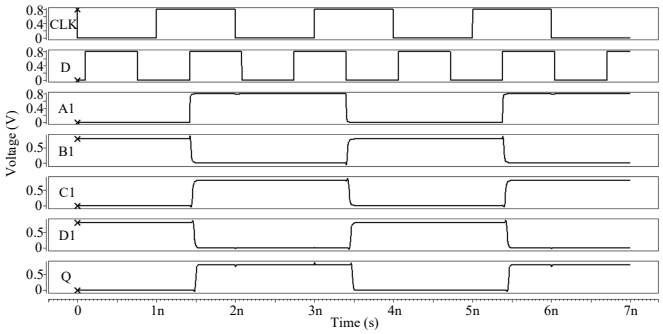

Fig. 6. Simulations for the normal operations of the proposed MCHTSL latch.

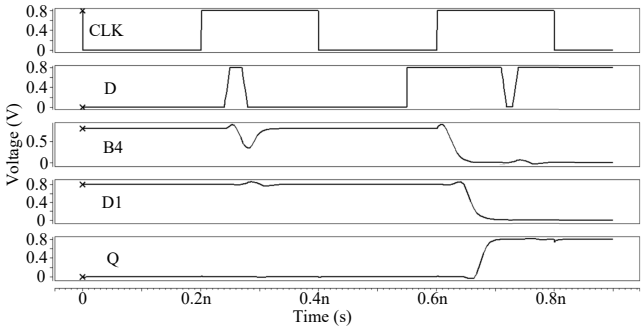

Fig. 7. Simulations of filtering cases for positive and negative SET pulse of the MCHTSL latch.

B. *Simulations*

To verify the correct operations of the proposed MCTHSL latch, extensive simulations were performed with the HSPICE tool from Synopsys. The latch was implemented in an advanced 22 nm CMOS technology with a W/L ratio, i.e., 90nm/22nm, of PMOS transistors and a W/L ratio, i.e., 45nm/22nm, of NMOS

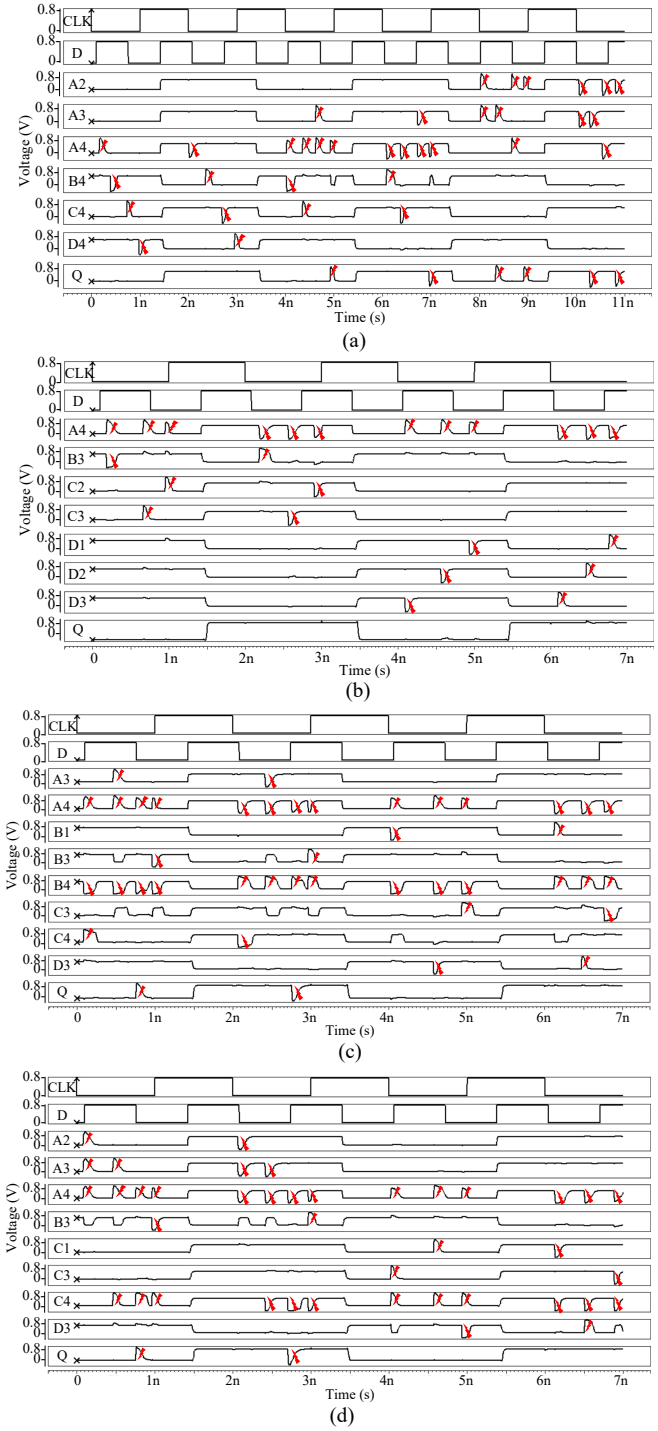

Fig. 8. Simulations of key SNU, DNU, and TNU injections of the latch design. (a) SNU and Case 1, (b) Case 2, (c) Case 3, (d) Case 4.

transistors. The supply voltage Vdd was set to 0.8V, and the working temperature was set to the room temperature. Figure 6 shows the simulations for the normal operations of the proposed MCTHSL latch. It can be seen that D can pass to Q when CLK = 1 and Q can hold the sampled D value when CLK = 0, which demonstrates the correct operations of the latch.

To verify the SNU, DNU, and TNU recovery of the latch, pertinent simulations were performed using the double exponential current source model with the same parameters as in [25]. Due to the symmetrical structure of the proposed latch, representative SNUs (i.e., A4 to D4), DNUs (see Cases 1 to 2 below) and TNUs (see Cases 3 to 4 below) are selected for simulations. It should be noted that A1 = Q in hold mode for the proposed latch.

Case 1: Two nodes from the same row or column; the representative node pairs are <A4, B4>, <A4, C4>, <A1, A2>, <A2, A3>, <A3, A4>, and <A4, A1>. Another scenario is that the single inputs of four devices are impacted; the representative node pairs are <A1, A3> and <A2, A4>.

Case 2: The scenarios except those in Case 1; the representative node pairs are <A4, B3>, <A4, C3>, <A4, D3>, <A4, C2>, <A4, D2>, and <A4, D1>.

Case 3: Three nodes from the same row; the representative node-list is <A4, B4, C4> only. Another scenario is that A4, B4 and another node are impacted; the representative node lists are <A4, B4, A3>, <A4, B4, A1>, <A4, B4, B3>, <A4, B4, B1>, <A4, B4, C3>, and <A4, B4, D3>.

Case 4: Three nodes from the same column; the representative node-list is <A4, A3, A2> only. Another scenario is that A4, C4 and another node are impacted; the representative node lists are <A4, C4, A3>, <A4, C4, A1>, <A4, C4, B3>, <A4, C4, C3>, <A4, C4, C1>, and <A4, C4, D3>.

Figure 8 shows the simulations of the key SNU, DNU and TNU injections of the proposed latch. Note that, the lighting marks in the figure denote injected errors and we used two/three simultaneously injected SNUs to mimic a DNU/TNU. It can be seen from Fig. 8 that, the proposed latch can recover from any key SNU, DNU, and TNU. Therefore, the simulations clearly demonstrate that the proposed latch can provide recovery from any possible SNU, DNU, and TNU.

IV. Comparative Results

For fair comparisons, the typical SET, SNU, DNU and/or TNU hardened latches reviewed in Section II were also implemented under the same conditions (i.e., 22nm CMOS technology, and 0.8V supply voltage and the room temperature) as the proposed MCTHSL latch. Table I shows the reliability and overhead comparison results among the SET, SNU, DNU and/or TNU hardened latches. Note that, in Table I, "Tol." means "tolerant", "Rec." means "recoverable", "Fil." means "filterable", "Ins." means "insensitive", "Area" means the silicon area measured as in [22], "D-Q Delay" means the average of the transmission delays (rise and fall) from D to Q, "CLK-Q Delay" means the average of the delays (rise and fall) from CLK to Q, and "Power" means the average of the power dissipation (dynamic and static), respectively.

Regarding latch reliability, it can be seen from Table I that the LSEH and HRLC latches are SNU-tolerant, SET-filterable and HIS-insensitive but they cannot provide complete SNU-recovery. The DICE latch is SNU-recoverable and HIS-insensitive but it cannot provide complete DNU-tolerance. The HLDTL-EV latch only has SNU/DNU tolerance. The DNURL and THLTCH latches can provide complete DNU-recovery and they are HIS-insensitive (the THLTCH can also filter SETs) but they are not completely TNU-tolerant. The LCTNUT, HITTSFL and TNUTL latches can tolerate TNUs (the HITTSFL is also SET-filterable and HIS-insensitive) but they cannot completely recover from TNUs. The TNURL latch can recover from TNUs but it cannot filter SETs. It can be seen that only the proposed MCTHSL latch can simultaneously provide SNU/DNU/TNU tolerance and recover, SET-filtering and HIS-insensitivity.

Regarding area overhead, it can be seen from Table I that the area of TNURL is the largest mainly because the latch uses many transistors (however, the latch cannot filter SETs). It can be also seen from Table I that, to provide more functions, such as TNU recovery and SET filtering, more area has to be introduced because the radiation-hardening-by-design (RHBD) approach is used for latches to ensure high reliability. The TNUTL

TABLE I
Reliability and Overhead Comparison Results Among the SET, SNU, DNU, and/or TNU Hardened Latches

Latch	SNU Tol.	SNU Rec.	DNU Tol.	DNU Rec.	TNU Tol.	TNU Rec.	SET Fil.	HIS Ins.	10^{-4}×Area (nm^2)	D-Q Delay (ps)	CLK-Q Delay (ps)	Power (μW)
LSEH [13]	√	×	×	×	×	×	√	√	4.16	61.23	47.25	1.20
HRLC [16]	√	×	×	×	×	×	√	√	3.86	43.93	43.76	0.75
DICE [14]	√	√	×	×	×	×	×	√	2.38	7.08	7.15	0.49
HLDTL-EV [15]	√	×	√	×	×	×	×	×	6.53	1.63	1.64	0.77
DNURL [17]	√	√	√	√	×	×	×	√	9.80	3.12	3.12	1.18
THLTCH [18]	√	√	√	√	×	×	√	√	9.50	12.38	12.46	1.58
LCTNUT [20]	√	√	√	×	√	×	×	×	7.13	1.63	1.66	0.67
HITTSFL [22]	√	√	√	×	√	×	√	√	8.91	22.37	25.62	1.37
TNURL [25]	√	√	√	√	√	√	×	√	19.01	5.44	5.47	1.18
TNUTL [19]	√	√	√	×	√	×	×	×	12.18	97.85	97.51	1.35
MCHTSL (Proposed)	√	√	√	√	√	√	√	√	12.18	77.97	77.87	1.37

and the proposed MCHTSL latch have comparable area overhead but the TNUTL latch cannot provide DNU/TNU recovery, SET filtering and HIS insensitivity.

Regarding D-Q delay, for the proposed MCTHSL latch and some existing hardened latches, such as the HLDTL-EV, DNURL, LCTNUT, and TNURL, their D-Q delay is small because there is a high-speed transmission path from D to Q for all of them. Conversely, the LSEH, HRLC, and HITTSFL latches have a large D-Q delay due to the use of many devices from D to Q for all of them. Note that, a SET filterable latch has to introduce more D-Q delay.

Regarding CLK-Q delay, it can be seen from Table I that it is close to the D-Q delay since they are both related to the devices from D to Q. For the proposed MCTHSL latch and some existing hardened latches, such as HLDTL-EV, DNURL, LCTNUT, and TNURL, their CLK-Q delay is small since their D-Q delay is small. Conversely, the latches, such as LSEH, HRLC, and HITTSFL, have a large CLK-Q delay since their D-Q delay is large.

Regarding power dissipation, the THLTCH latch has the highest power dissipation, since the latch has much current competition among internal nodes to ensure complete DNU recoverability and SET-filtering (the latch also uses an extra delay element marked with τ). Note that, when a latch has a large area and/or does not use the CG technique, its power dissipation is high. Since the proposed MCTHSL latch uses redundant area to provide more functions, its power dissipation is not very low.

In summary, from the above comparison and evaluation results we can see that, the proposed MCTHSL latch has high reliability compared with typical latches, low area overhead compared with the TNURL latch, low delay overhead compared with the TNUTL latch, and low power overhead compared with the THLTCH latch.

V. Conclusions and Further Work

With CMOS technology scaling, advanced integrated circuits are becoming highly susceptible to soft errors. This paper has proposed a TNU-recoverable HIS-insensitive and SET filtering latch for reliable computing. The proposed MCTHSL latch comprises a 4×4 device matrix that is constructed from one input-split Schmitt Trigger and 15 interlocking 2-input CEs. Simulation results have demonstrated the SNU, DNU, and TNU-recovery of the proposed latch with moderate overhead.

Generally, a SET filterable latch (e.g., the proposed latch) that has a larger D-Q delay can filter wider SETs. In our further work, we will measure and analyze widths of filterable SETs. Moreover, the impacts of process, voltage, and temperature (PVT) variations on latches will also be considered for further comparisons and evaluations.

References

[1] J. Black, P. Dodd, and K. Warren, "Physics of Multiple-Node Charge Collection and Impacts on Single-event Characterization and Soft Error Rate Prediction," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1836-1851, 2013.

[2] M. Ebara, K. Yamada, K. Kojima, et al, "Process Dependence of Soft Errors Induced by α Particles, Heavy Ions, and High Energy Neutrons on Flip Flops in FDSOI," *IEEE Journal of the Electron Devices Society,* vol. 7, pp. 817-824, 2019.

[3] H. Liang, X. Xu, Z. Huang, et al, "A Methodology for Characterization of SET Propagation in SRAM-based FPGAs," *IEEE Transactions on Nuclear Science,* vol. 63, no. 6, pp. 2985-2992, 2016.

[4] A. Yan, K. Yang, Z. Huang, et al, "A double-node-upset self-recoverable latch design for high performance and low power application," *IEEE Transactions on Circuits & Systems II: Express Briefs*, vol. 66, no. 2, pp. 287-291, 2019.

[5] A. Jain, A. Veggetti, D. Crippa, et al, "Radiation Tolerant Multi-Bit Flip-Flop System with Embedded Timing Pre-Error Sensing", *IEEE Journal of Solid-State Circuits*, vol. 57, no. 9, pp. 2878-2890, 2022.

[6] J. Li, L. Xiao, L. Li, et al, "A Low-Cost Error-Tolerant Flip-Flop Against SET and SEU for Dependable Designs," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 69, no. 7, pp. 2721-2729, 2022.

[7] J. Shah, D. Nairn, and M. Sachdev, "A 32 kb Macro with 8T Soft Error Robust, SRAM Cell in 65-nm CMOS", *IEEE Transactions on Nuclear Science,* vol. 62, no. 3, pp. 1367-1374, 2015.

[8] A. Yan, J. Xiang, A. Cao, et al, "Quadruple and Sextuple Cross-Coupled SRAM Cell Designs with Optimized Overhead for Reliable Applications," *IEEE Transactions on Device and Materials Reliability*, vol. 22, no. 2, pp. 282-295, 2022.

[9] M. Omana, D. Rossi, and C. Metra, "High-performance robust latches," *IEEE Transactions on Computers*, vol. 59, no. 11, pp. 1455-1465, 2010.

[10] S. Mitra, M. Zhang, N. Seifert, et al, "Built-in soft error resilience for robust system design," *IEEE Int. Conf. on Integrated Circuit Design and Technology*, TX, USA, pp. 1-6, 2007.

[11] H. Wang, L. Chen, R. Liu, et al, "An area efficient stacked latch design tolerant to SEU in 28 nm FDSOI technology," *IEEE Transactions on Nuclear Science,* vol. 63, no. 6, pp. 3003-3009, 2016.

[12] W. Wei, K. Namba, Y. Kim, et al, "A novel scheme for tolerating single event/multiple bit upsets (SEU/MBU) in non-volatile memories," *IEEE Transactions on Computers,* vol. 65, no. 3, pp. 781-790, 2016.

[13] R. Rajaei, M. Tabandeh, and M. Fazeli, "Low cost soft error hardened latch designs for nano-scale CMOS technology in presence of process variation," *Microelectronics Reliability*, vol. 53, pp. 912–924, 2013.

[14] T. Calin, M. Nicolaidis, and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology," *IEEE Transactions on Nuclear Science,* vol. 43, no. 6, pp. 2874-2878, 1996

[15] H. Li, L. Xiao, J. Li, et al, "High Robust and Low Cost Soft Error Hardened Latch Design for Nanoscale CMOS Technology," *IEEE International Conference on Solid-State and Integrated Circuit Technology*, pp. 1-3, 2018

[16] Y. Yamamoto and K. Namba, "Construction of Latch Design with Complete Double Node Upset Tolerant Capability Using C-Element," *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, pp. 1-6, 2018

[17] A. Yan, Y. Ling, J. Cui, et al, "Quadruple Cross-Coupled Dual-Interlocked-Storage-Cells based Multiple-Node-Upset-Tolerant Latch Designs," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 67, no. 3, pp. 879-890, 2020.

[18] Y. Li, H. Wang, S. Yao, et al, "Double node upsets hardened latch circuits," *Journal of Electronic Testing,* vol. 31, no.1, pp. 537-548, 2015.

[19] A. Watkins, and S. Tragoudas, "Radiation hardened latch designs for double and triple node upsets," *IEEE Transactions on Emerging Topics in Computing*, vol. 8, no. 3, pp. 616-626, 2020.

[20] A. Yan, C. Lai, Y. Zhang, et al, "Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS," *IEEE Transactions on Emerging Topics in Computing,* vol. 9, no. 1, pp. 520-533, 2021.

[21] K. Katsarou, and Y. Tsiatouhas, "Soft error interception latch: double node charge sharing SEU tolerant design," *Electronics Letters*, vol. 51, no. 4, pp. 330-332, 2015.

[22] A. Yan, Z. Fan, L. Ding, et al, "Cost-Effective and Highly Reliable Circuit-Components Design for Safety-Critical Applications," *IEEE Transactions on Aerospace and Electronic Systems,* vol. 58, no. 1, pp. 517-529, 2022.

[23] N. Eftaxiopoulos, N. Axelos, and K. Pekmestzi, "DONUT: A double node upset tolerant latch," *IEEE Computer Society Annual Symposium on VLSI*, Montpellier, France, pp. 509-514, 2015.

[24] N. Eftaxiopoulos, N. Axelos, G. Zervakis, et al, "Delta DICE: A double node upset self-recoverable latch," *IEEE Int. Midwest Symposium on Circuits and Systems*, Fort Collins, USA, pp. 1-4, 2015.

[25] A. Yan, X. Feng, Y. Hu, et al, "Design of a Triple-Node-Upset Self-Recoverable Latch for Aerospace Applications in Harsh Radiation

Environments," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 56, no. 2, pp. 1163-1171, 2020.

[26] S. Anjan, and B. Maryam, "Robust soft error tolerant CMOS latch configurations," *IEEE Transactions on Computers*, vol.65, pp.2820-2834, 2016.

[27] H. Liang, Z. Wang, Z. Huang, et al, "Design of a Radiation Hardened Latch for Low-power Circuits," *IEEE Asian Test Symposium*, pp.19-24, 2014.

[28] A. Dixit and A. Wood, "The Impact of New Technology on Soft Error Rates," IEEE International Symposium on Reliability Physics, pp. 486-492, 2011.