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Aibin Yan[1,2], Yu Chen[1], Shaojie Wei[1], Jie Cui[1], Zhengfeng Huang[2], Patrick Girard[3], and Xiaoqing Wen[4]

[1]*School of Computer Science and Technology, Anhui University, Hefei, China*
[2]*School of Microelectronics, Hefei University of Technology, Hefei, China*
[3]*Laboratory of Informatics, Robotics and Microelectronics of Montpellier, University of Montpellier / CNRS, Montpellier, France*
[4]*Graduate School of Computer Science and Systems Engineering, Kyushu Institute of Technology, Fukuoka, Japan*

***Abstract*—As CMOS processes continue to shrink, nano-scale CMOS latches have become increasingly sensitive to multiple-node upset (MNU) errors caused by radiation. To tolerate MNU, a novel quadruple-node-upset (QNU) self-recoverable latch is proposed in this paper. The proposed latch is mainly constructed from six blocks of three-level C-elements (TLCEs) and six inverters. With the mutual feedback of the various TLCEs, the proposed latch can recover from any QNU. Furthermore, due to the clock gating methodology and a high-speed transmission path, the proposed latch has lower overhead in terms of power dissipation and transmission delay. Simulation results show that the proposed latch achieves high reliability with moderate overhead compared to typical existing latches.**

***Index Terms*—Radiation hardening, fault tolerance, multiple-node upset, quadruple-node upset.**

I. Introduction

With ever-advancing CMOS technologies, integrated circuits have reached the nano-scale level, greatly reducing their area, delay, and power overheads. However, with the aggressive reduction of transistor feature sizes, integrated circuits have become more susceptible to high-energy particles, such as high-energy neutrons, α rays, heavy ions, and electrons [1]. When a particle collides with a sensitive node in an integrated circuit, it will generate extra charge, resulting in an erroneous transient pulse or node upset, called soft errors [2, 3]. Soft errors include single-node upset (SNU), double-node upset (DNU), triple-node upset (TNU), and even quadruple-node-upset (QNU). Soft errors cause a serious issue for sequential circuits because they can result in bit-flipping in memory elements, such as latches, flip-flops, and static random-access memory (SRAM) bit-cells [4]. As a result, the value stored in storage cells may change. Such value changes of storage cells may have a severe impact on circuit reliability in mission-critical fields (e.g., aerospace and medical fields) and even severely affect the life and health of related personnel.

According to the statistics in [5-7], the probability of the occurrence of MNU generally increases as particle energy increases and technology scaling proceeds. Therefore, in order to provide highly reliable integrated circuits, it is necessary to design storage cells that can tolerate and even recover from MNU. To provide radiation hardening capability, researchers have proposed a series of radiation-hardened circuit structures [8-22]. Some of them use time redundancy, e.g., using delay elements as error-filterable components [8], some use pulse detection technology, such as that in [9], and some use space redundancy, e.g., introducing redundant storage nodes and/or triple-module-redundancy (TMR) along with voting circuits [10-14]. In recent years, with the exploration of deep space, there are more and more cases of MNU, and the demand for a latch that can provide complete MNU self-recoverability is greatly increased [2, 6]. In the 22nm SRAM, the ratio of the total number of MNU to the total number of SNU is as high as 50%, indicating that the influence of MNU is more severe [17]. Although there are many existing radiation-hardened latches, most of them can tolerate only a few node upsets, among which SNU and DNU tolerable latches are the main ones. To the best of our knowledge, only a few latches can completely self-recover from QNU. Although few latches, such as those in [15-17], can completely tolerate QNU, they cannot completely self-recover from QNU.

Note that C-elements (CEs) are widely used in many hardened blocks. Figure 1 shows the structure of CEs. Figure 1-(a) and Fig. 1-(c) show the structure of a 2-input CE and a clock-gating (CG) based on the 2-input CE, respectively. Figure 1-(b) and Fig. 1-(d) show the structure of a 3-input CE and a CG-based 3-input CE, respectively. When the inputs of a CE have the same value, it outputs the reversed value of the inputs. If the inputs of a CE have different values, its output temporarily remains in its original state.

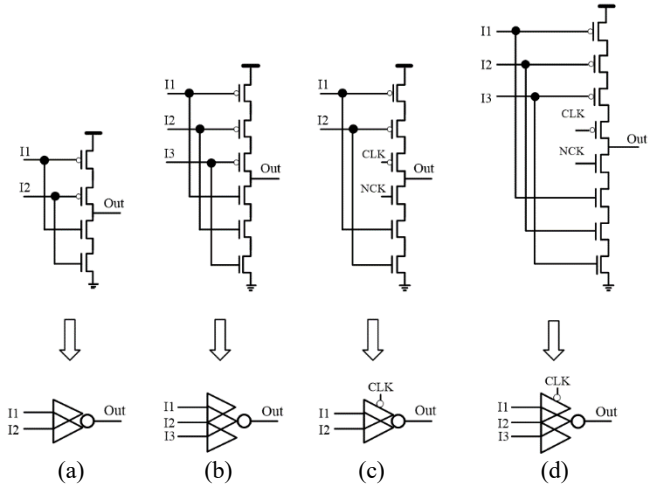

Fig. 1. Structure of C-elements (CEs). (a) 2-input CE, (b) 3-input CE, (c) CG-based 2-input CE, and (d) CG-based 3-input CE.

In this paper, we propose a hardened latch that is composed of six TLCEs, composed of six 2-input CEs and an inverter. The whole structure is highly symmetrical. In any TLCE, when any quadruple nodes are simultaneously affected by a QNU, the proposed latch can self-recover from the QNU. This is because these three-level soft-error-interceptive TLCEs are mutually interlocked to form a highly reliable storage module to store values for the latch. Furthermore, a high-speed path and clock-gating technique are used in the proposed latch to reduce overhead. Simulation results show that the proposed latch has complete QNU self-recoverability with a low transmission delay and low delay-power-area product.

The rest of the paper is organized as follows. Section II introduces typical SNU, DNU, TNU, and QNU hardened latch designs. Section III describes the schematic, working principles, and fault-tolerance verifications for the proposed latch. Section IV presents comprehensive evaluation and comparison results for the proposed and existing latch designs. Section V concludes the paper.

II. Previous Radiation Hardened Latches

In this section, typical existing radiation-hardened latches are reviewed. A transmission gate (TG) is a basic component of latches. Figure 2 shows its schematic and symbol. When NCK = 0 and CLK = 1, TG is switched on and the input value can be transmitted to the output. When NCK = 1 and CLK = 0, TG is switched off and the input value cannot be transmitted to the output. Note that, for all latches in this paper, CLK is the system clock, NCK is the negative system clock, D is the input, and Q is the output. Figure 3 shows the schematics of all reference latches.

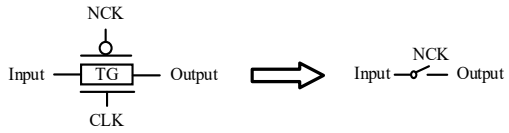

Fig. 2. Schematic of TG.

Figure 3-(a) shows the schematic of RH1 [19], which consists of a memory module, two inverters, a TG, a CG-based 2-input CE, and a buffer. The inputs D and DN charge the latch through two single-pass transistors. The input D is directly connected to the output Q via a buffer and a TG. RH1 can tolerate SNU but cannot recover from SNU. Figure 3-(b) shows the schematic of SHLR [20], which consists of two CG-based 2-input CEs and three input-splitting inverters, forming feedback interlocking loops to recover the original values after a radiation event. An SHLR latch can tolerate and

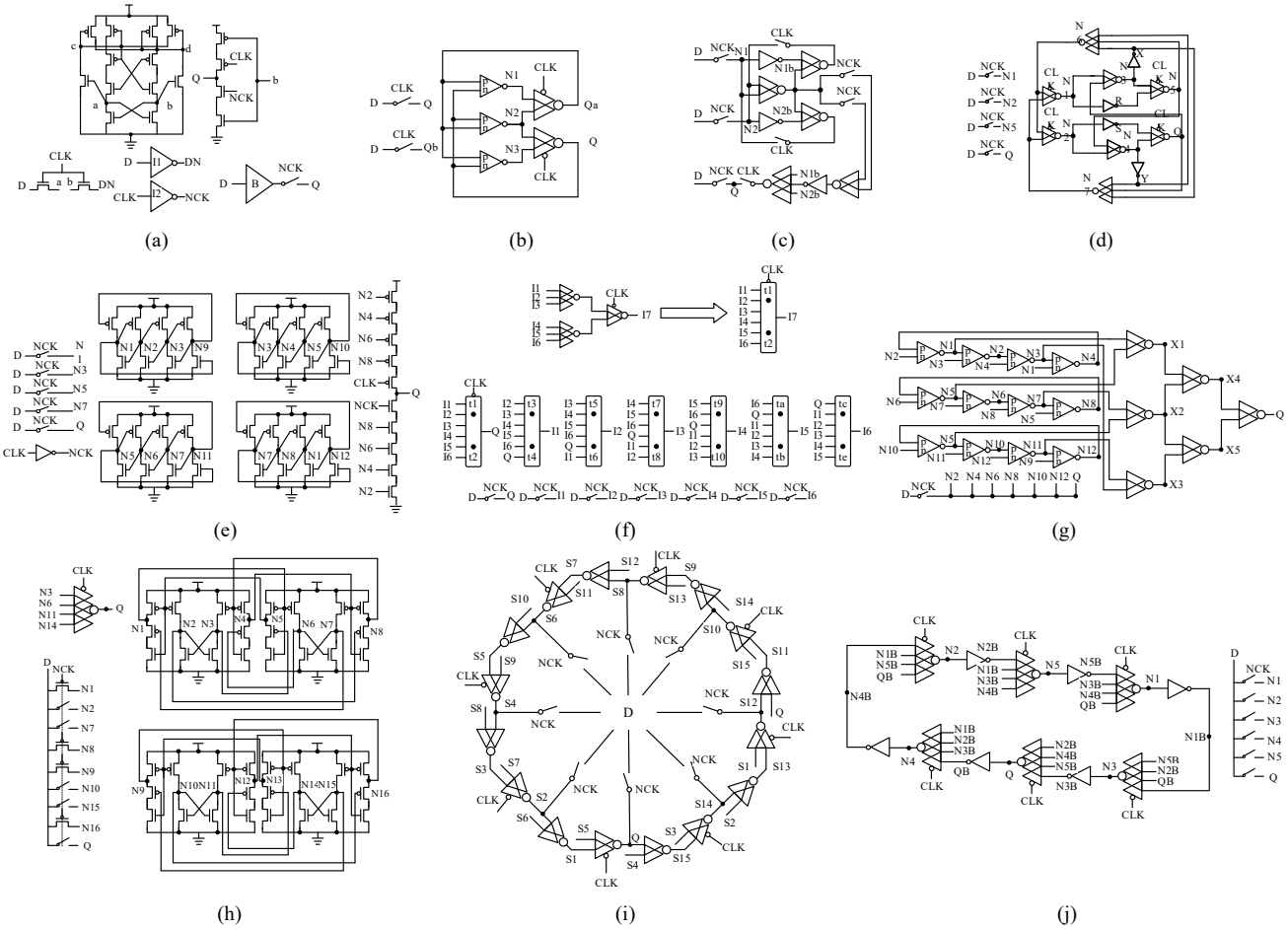

Fig. 3. Schematics of existing hardened latches. (a) RH1 [19], (b) SHLR [20], (c) HLDTL-EV [21], (d) DNUSH [22], (e) TNULH [13], (f) TNURL [14], (g) QNUTL [15], (h) Quad-SIRI [16], (i) HLMR [17] and (j) LCQNUSR [18].

self-recover from SNU. However, SHLR cannot tolerate DNU, TNU, and QNU.

HLDTL-EV is a DNU-tolerant latch [21]. Figure 3-(c) shows its structure. This latch mainly consists of six TGs, an SNU Resilient Cell (SRC), an inverter, a 2-input CE, and a 3-input CE. SRC consists of two TGs, three 2-input CEs, and two inverters. The input D of HLDTL-EV is connected to the output Q by a TG. Although HLDTL-EV can tolerate DNU, it cannot recover from DNU. Figure 3-(d) shows the schematic of DNUSH [22], which consists of four CG-based 2-input CEs, two 2-input CEs, four inverters, two 3-input CEs, and four TGs. DNUSH can both tolerate SNU and DNU, and also can self-recover from them. However, DNUSH cannot tolerate TNU and QNU.

Figure 3-(e) is the schematic of TNULH [13], which is composed of four dual-interlocked-storage-cells (DICEs), a CG-based 2-input CE, and five TGs. Four DICEs form many feedback loops, enabling TNULH to tolerate DNU and TNU. According to the design concept of TMR, the structure is divided into three parts. The input D is directly connected to five nodes by five TGs. Four of four paths are applied to the input nodes of 4-input CE through typical DICEs. TNULH can tolerate TNU, but cannot recover from TNU. Figure 3-(f) shows the schematic of TNURL [14], and the latch is mainly constructed from seven soft-error-interceptive modules (SIMs). In the latch, SIM1 is based on CG. As shown in Fig. 3-(f), SIM1 consists of two 3-input CEs and a CG-based 2-input CE, and the inputs of the CG-based 2-input CE are determined by the outputs of these two 3-input CEs. Other SIM structures are like SIM1, except that the CG-based 2-input CE is replaced with a 2-input CE. It can be seen that the output of each SIM is fed back to one input of any other SIM. TNURL can self-recover from TNU, but cannot tolerate QNU.

Figure 3-(g) shows the structure of QNUTL [15], which is composed of two parts, the left part is composed of three DICEs, and the right part is a three-level SIM. The SIM consists of six 2-input CEs that include a CG-based CE at the output stage. The input of the SIM is connected to six non-adjacent nodes of DICEs. QNUTL can tolerate DNU, TNU, and QNU but cannot recover from DNU, TNU, and QNU. Figure 3-(h) shows the structure of Quad-SIRI [16], which is composed of two Dual Soft-error-immune (Dual-SIRI) modules, five TGs, four PMOS transistors, and a CG-based 4-input CE. Each Dual-SIRI module consists of two SIRI modules. The SIRI is composed of six PMOS transistors and four NMOS transistors. Quad-SIRI can tolerate TNU and QNU, but cannot recover from TNU and QNU.

Figure 3-(i) shows the schematic of HLMR [17], which is composed of eight 2-input CEs and eight CG-based 2-input CEs to form many feedback loops with 16 redundant nodes. Eight TGs are used to initialize the values of internal nodes. HLMR can tolerate QNU, but cannot recover from QNU. Figure 3-(j) shows the schematic of LCQNUSR [18], which is composed of six TGs, six inverters, and six CG-based 4-input CEs. In [18], the author claimed that the latch can recover from QNU. However, it has at least a counterexample that cannot recover. For example, when a DNU occurs in <N1, N5>, the latch cannot recover.

III. Proposed Hardened Latch Design

A. Circuit Structure and Behavior

Figure 4 shows the schematic of the proposed latch, which is mainly composed of six TGs and six TLCEs. The latch contains 6 primary nodes (i.e., N1, N2, N3, N4, N5, and N6) and 36 secondary nodes. As shown in Fig. 4-(a), the TLCE consists of six 2-input CEs and an inverter, and each TLCE has six internal nodes (i.e., X1, X2, X3, X4, X5, and X6). The inputs of each TLCE are the outputs of all other TLCEs. The internal nodes of each TLCE are equivalent to the internal nodes of all other TLCEs. In [14], it has been verified that the three-level SIM module can effectively tolerate DNU and TNU. Since TLCE has almost the same structure as a three-level SIM (except that an inverter is added to the three-level SIM). Therefore, TLCE can also tolerate DNU and TNU. In the proposed latch, six TLCEs form many feedback loops, which allow the latch to recover from any QNU.

In the proposed latch, CLK is the clock of the system and NCK is the negative clock of the system. When CLK = 1 and NCK = 0, the latch works in transparent mode and the TG between its D and Q is switched on. When CLK = 0 and NCK = 1, the latch works in hold mode, and the TG between its D and Q is off. If the latch is affected by radiation at this time, the value stored by the latch may be changed.

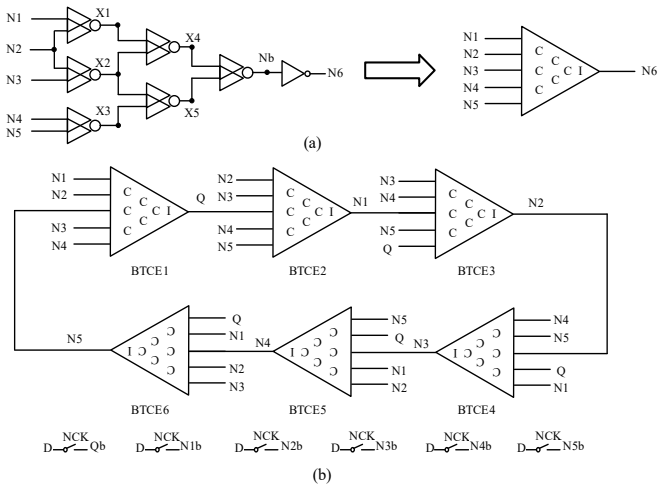

Fig. 4. The proposed latch. (a) TLCE schematic and (b) latch schematic.

In the following, we present the principle that the proposed latch can self-recover from SNU, DNU, TNU, and QNU. When the latch suffers from an SNU, the feature of CE makes the proposed latch tolerant SNU. When the latch suffers from DNU and TNU, the feature of TLCE makes the proposed latch tolerant DNU and TNU. Therefore, the proposed latch can recover from SNU, DNU, and TNU.

There are many combinations of nodes where QNU occurs. We will list typical node-pairs and analyze the principle of QNU self-recovery. In order to show the principle of QNU self-recovery more clearly, we divide the occurrence of QNU into five cases.

Case1: The nodes where a QNU occurs are all external nodes. Assume that the flipped nodes are N1, N2, N3, and N4. In this case, four of the five inputs of two TLCEs (i.e., TLCE1 and TLCE6) in the latch are flipped but their outputs remain

unchanged. Three of the five inputs of four TLCEs (TLCE2, TLCE3, TLCE4, and TLCE5) are flipped, and their outputs are also flipped. The inputs N2, N3, and N4 of TLCE2 are flipped but their error values cannot pass to the nodes of the inner second level (i.e., the internal nodes X4 and X5 of TLCE2). TLCE2's internal nodes X4 and X5 do not change. Therefore, its output (i.e., N1) will output the correct value. Likewise, the output N3 of the TLCE4 can also restore correctly. Note that errors from TLCE3 and TLCE5 can pass to their internal nodes X4 and X5. However, after N1 and N3 recover, only two of the inputs of TLCE3 and TLCE5 are incorrect. Therefore, their outputs (N2 and N4) can recover correctly. Therefore, when QNU occurs in N1, N2, N3, and N4, the proposed latch can recover from QNU. Similarly, if QNU occurs at any four external nodes, the proposed latch can recover correctly.

Case2: The four nodes where a QNU occurs include an internal node and three external nodes. At this time, we only need to consider the case where three external nodes as the inputs of a TLCE, and the flip internal node is also an internal node of this TLCE (all the other cases can be attributed to the TNU or DNU cases). For example, N1, N2, and N3 are flipped, and TLCE5's internal node X3 is flipped. At this time, all the internal nodes and output of TLCE5 are flipped. Then, a total of four external nodes (i.e., N1, N2, N3, and N4) are flipped. The situation is equal to Case1. All the nodes will recover. Therefore, the proposed latch can recover from QNU in this case.

Case3: The four nodes where a QNU occurs include two internal nodes and two external nodes. At this time, we only need to discuss the case where these errors all occur in one TLCE. For example, the internal nodes X2 and X3 of TLCE5, and N1 and N2 are flipped. After that, all the internal nodes of TLCE5 will be flipped. The output (i.e., N4) of TLCE5 will also be flipped. In this case, three external nodes (i.e., N1, N2, and N4) of the proposed latch flip. Since the internal nodes of TLCE2 are unchanged, its output N1 will recover. Similarly, N2 and N4 will recover. Then all inputs of TLCE5 are correct, and the output of TLCE5 will be correct again on the next loop. Therefore, the latch can recover from QNU in this case.

Case4: The four nodes where a QNU occurs include three internal nodes and an external node. In this case, we only need to discuss the case where all the nodes where QNU occurs are in one TLCE (at this time, QNU has the most serious effect on the entire circuit). Then, all the internal nodes of the TLCE are flipped, and its output is flipped as well. For example, if internal nodes X1, X2, and X3 of TLCE5 and N1 are flipped, all internal nodes of TLCE5 are flipped. Therefore, the output of TLCE5 (i.e., N4) flips. Because the value of the internal node of TLCE2 is correct, its output (i.e., N1) will recover. All inputs of TLCE5 are recovered correctly, and then its internal node and output (i.e., N4) are recovered. Therefore, the proposed latch can recover from QNU in this case.

Case5: The four nodes where a QNU occurs are all internal nodes. In this case, we only need to consider the case where all internal nodes where QNU occurs are in one TLCE (at this time, QNU has the most serious effect on the entire circuit). For example, if QNU occurs in the internal node of TLCE1, the output of TLCE1 also flips. However, since the inputs N1, N2, N3, N4, and N5 of TLCE1 are all correct, the nodes where QNU occurs can be recovered correctly. Therefore, if any internal node occurs QNU in this case, the proposed latch can recover. In summary, if QNU occurs at four external nodes, the proposed latch can recover correctly.

B. Simulation Results

The proposed latch was implemented/simulated in Synopsys HSPICE with an advanced 22 nm CMOS technology model. The working temperature of the latch was the room temperature and the supply voltage was 0.8V. Regarding transistor sizes, the PMOS transistors had ratio of W/L = 90nm/22nm, and the NMOS transistors had ratio of W/L = 45nm/22nm.

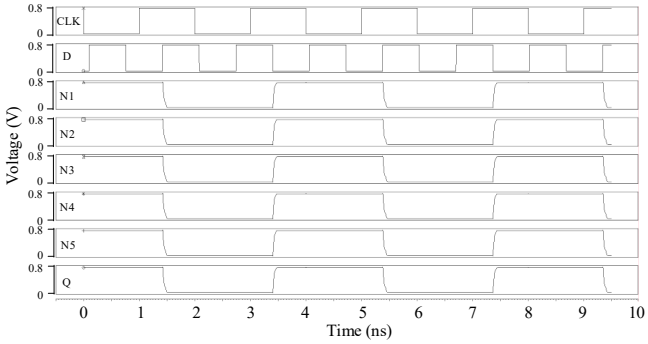

Fig. 5 Simulation result for the error-free operations of the proposed latch.

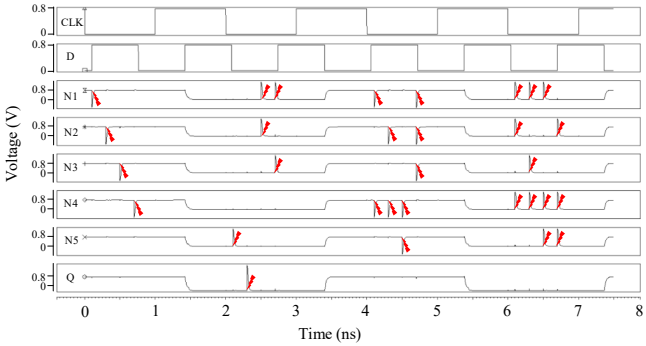

Fig. 6 Simulation results for the key SNU, DNU, and TNU injections of the proposed latch.

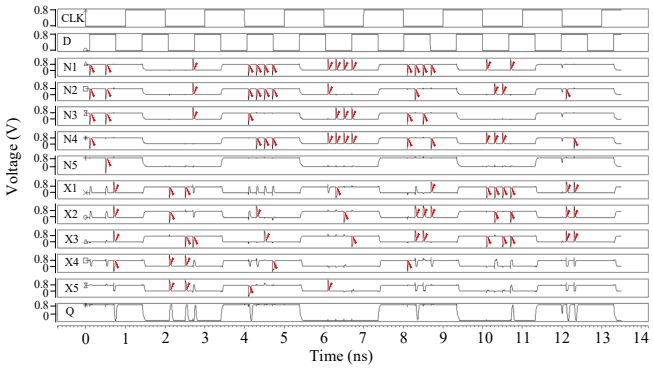

Fig. 7 Simulation results for the key QNU injections of the proposed latch.

Figure 5 shows the simulation result for the error-free case of operations of the proposed latch design. The proposed latch works in transparent mode when the clock signal CLK is high, and the proposed latch works in hold mode when the

clock signal CLK is low. The simulation results show that the state of the output (i.e., Q) of the latch changes along with the input (i.e., D) in transparent mode, and the output of the latch remains unchanged in hold mode. Note that, in the following simulations, we injected SNU, DNU, TNU, and QNU errors when CLK = 0 (i.e., the latch works in hold mode).

TABLE I
STATISTIC RESULTS FOR THE COMPLETE KEY QNU INJECTIONS OF THE PROPOSED LATCH ACCORDING TO FIGURE 7.

Time (ns)	QNU	State	Time (ns)	QNU	State
0.1	N1, N2, N3, N4	Q=1	6.5	N1, N3, N4, X2	Q=0
0.5	N1, N2, N3, N5	Q=1	6.7	N1, N3, N4, X3	Q=0
0.7	X1, X2, X3, X4	Q=1	8.1	N1, N3, N4, X4	Q=1
2.1	X1, X2, X4, X5	Q=0	8.3	N1, N2, X2, X3	Q=1
2.5	X1, X3, X4, X5	Q=0	8.5	N1, N3, X2, X3	Q=1
2.7	N1, N2, N3, X3	Q=0	8.7	N1, N4, X1, X2	Q=1
4.1	N1, N2, N3, X5	Q=1	10.1	N1, N4, X1, X3	Q=0
4.3	N1, N2, N4, X2	Q=1	10.3	N2, N4, X1, X2	Q=0
4.5	N1, N2, N4, X3	Q=1	10.5	N2, N4, X1, X3	Q=0
4.7	N1, N2, N4, X4	Q=1	10.7	N1, X1, X2, X3	Q=0
6.1	N1, N2, N4, X5	Q=0	12.1	N2, X1, X2, X3	Q=1
6.3	N1, N3, N4, X1	Q=0	12.3	N4, X1, X2, X3	Q=1

In order to verify the radiation hardening capability of the proposed latch, we carried out a series of simulations. Firstly, SNU, DNU, and TNU were considered. Figure 6 shows the simulation results for the key SNU, DNU, and TNU injections of the proposed latch. As shown in Fig. 6, when CLK = 0, an SNU was injected on nodes N1, N2, N3, N4, N5, and Q at 0.1ns, 0.3ns, 0.5ns, 0.7ns, 2.1ns, and 2.3ns, respectively. A DNU was injected on node-pairs <N1, N2>, <N1, N3>, <N1, N4>, <N2, N4>, and <N4, N5> at 2.5ns, 2.7ns, 4.1ns, 4.3ns, and 4.5ns, respectively. A TNU was injected on node-lists <N1, N2, N3>, <N1, N2, N4>, <N1, N3, N4>, <N1, N4, N5>, and <N2, N4, N5> at 4.7ns, 6.1ns, 6.3ns, 6.5ns, and 6.7ns, respectively. Note that, the lighting marks in Fig. 6 denote the injected errors. The simulation results show that the states of all nodes injected with SNU, DNU, and TNU can recover in a short time. Therefore, the proposed latch can self-recover from these injected SNU, DNU, and TNU.

Secondly, QNUs are considered. Similarly, to perform the complete simulations, all node-lists in the latch were injected with QNU errors. Figure 7 shows the simulation results for the key QNU injections of the proposed latch. Table I shows the statistical results for the complete key QNU injections of the proposed latch design according to Fig. 7. In Table I, "Time" denotes the injection time, "QNU" denotes the injected QNU on the key nodes, and "State" denotes the correct state of Q. When CLK = 0, a QNU was injected on these node-lists at 0.1ns, 0.5ns, 0.7ns, 2.1ns, 2.5ns, 2.7ns, 4.1ns, 4.3ns, 4.5ns, 4.7ns, 6.1ns, 6.3ns, 6.5ns, 6.7ns, 8.1ns, 8.3ns, 8.5ns, 8.7ns, 10.1ns, 10.3ns, 10.5ns, 10.7ns, 12.1ns, and 12.3ns, respectively. Note that, the lighting marks in Fig. 7 denote the injected QNU errors. The simulation results show that the states of all nodes injected with QNU can recover in a short time. Therefore, the proposed latch can self-recover from these injected QNU. In summary, the simulation results show that the proposed latch can recover from SNU, DNU, TNU, and QNU providing high reliability.

IV. COMPARISONS

We compared the proposed latch with the existing latches, i.e., RH1 [19], SHLR [20], HLDTL-EV [21], DNUSH [22], TNULH [13], TNURL [14], QNUTL [15], Quad-SIRI [16], HLMR [17] and LCQNUSR [18], to prove the superiority of the proposed latch. To make a fair comparison, the reference latches were also designed with the same conditions (i.e., 22 nm CMOS technology, room temperature and 0.8V supply voltage).

Table II shows the radiation hardening capability of all latches in this paper. In Table II, the hardening capability of latches is gradually enhanced from top to bottom. The proposed latch is positioned at the bottom, indicating its robustness among all these latches. It is essential to mention that the author of the LCQNUSR latch in Table II claimed that the latch can recover from QNU. However, our complete verification results showed that the latch cannot recover from QNU.

TABLE II
THE RADIATION-HARDENING CAPABILITY OF ALL LATCHES IN THIS PAPER

Latch Name	SNU Tolerant	SNU Recoverable	DNU Tolerant	DNU Recoverable	TNU Tolerant	TNU Recoverable	QNU Tolerant	QNU Recoverable
RH1 [19]	Yes	No	No	No	No	No	No	No
SHLR [20]	Yes	Yes	No	No	No	No	No	No
HLDTL-EV [21]	Yes	Yes	Yes	No	No	No	No	No
DNUSH [22]	Yes	Yes	Yes	Yes	No	No	No	No
TNUHL [13]	Yes	Yes	Yes	Yes	Yes	No	No	No
TNURL [14]	Yes	Yes	Yes	No	Yes	Yes	No	No
QNUTL [15]	Yes	Yes	Yes	No	Yes	No	Yes	No
Quad-SIRI [16]	Yes	Yes	Yes	Yes	Yes	No	Yes	No
LCQNUSR [18]	Yes	Yes	Yes	Yes	Yes	No	Yes	No
HLMR [17]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Proposed	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table III shows the comparisons among radiation-hardened latch designs. The metrics for comparisons include transmission delay, area, and power consumption. The transmission delay refers to the delay from D to Q, i.e., the average of the rise and fall delays of D to Q. The area is calculated as in [14]. Power consumption is the average of power (dynamic and static).

Using the radiation-hardening-by-design, the latch area and hardening capability are directly proportional. In general, the higher the hardening capability, the larger the area of the latch. In terms of area, the proposed latch has a disadvantage compared to many existing latches discussed in this paper. But, the area of the proposed latch is not the largest in Table III (the proposed latch has the most superior hardening capability). In terms of delay, the proposed latch is moderate compared to the existing latches in this paper. Many latches use a high-speed path from D to Q but their structures are different and have intrinsic properties so that their delay is not the same but small. In terms of power consumption, the proposed latch employs more transistors, resulting in extra power consumption. Therefore, the advantage of enhancing the hardening capability of the proposed latch is at the cost of overhead. In summary, the proposed latch has higher reliability with reasonable additional overhead than the existing latches discussed in this paper, making it suitable for robust computing in harsh radiation environments.

TABLE III
COMPARISONS AMONG RADIATION HARDENED LATCH DESIGNS

Latch Name	10^{-4}×Area (nm^2)	Delay (ps)	Power (μW)
RH1 [19]	4.36	9.00	2.98
SHLR [20]	4.16	3.90	0.70
HLDTL-EV [21]	6.53	1.63	0.86
DNUSH [22]	8.61	3.60	0.89
TNULH [13]	7.72	1.61	0.83
TNUL [14]	21.09	5.39	1.15
QNUTL [15]	9.50	1.63	1.88
Quad-SIRI [16]	10.10	1.63	1.83
LCQNUSR [18]	12.47	2.40	1.34
HLMR [17]	14.26	4.14	0.89
Proposed	16.04	3.67	4.37

V. CONCLUSIONS

Soft errors frequently occur in advanced circuits under the influence of harsh radiation. With decreasing CMOS process sizes, QNU is becoming more likely to occur. In order to achieve high reliability, this paper has proposed a latch with QNU self-recoverability the proposed latch is composed of six TLCEs, each TLCE having a three-level structure and each TLCE being composed of six two-input CEs and an inverter. Compared with typical existing the other latches, the proposed latch has a clear advantage in terms of reliability at the cost of overhead.

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