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***Abstract*—With the rapid advancement of semiconductor technologies, integrated circuits, especially storage elements (e.g., latches) have become increasingly vulnerable to soft errors. In order to effectively tolerate double-node-upsets (DNUs) caused by radiation and reduce the delay and area of latches, this paper proposes a DNU self-recoverable latch with low overhead in terms of power and area. The proposed latch mainly comprises seven 2-input C-elements and two inverters to achieve DNU self-recovery. Simulation results show that the proposed latch can recover from all possible DNUs and that it can reduce delay by 45.71%, power by 29.13%, area by 65.93%, and area-power-delay-product by 87.42% on average compared to typical existing DNU self-recoverable latches.**

***Index Terms*—Radiation hardening, latch reliability, soft error, double-node-upset, self-recovery.**

I. Introduction

In nanometer technologies, the feature sizes of transistors continue to shrink and the critical charge of a sensitive node decreases significantly, making integrated circuits more susceptible to soft errors caused by space radiation [1, 2]. Soft errors are caused by the strike of high-energy particles, such as alpha particles, neutrons, protons and electrons [3]. Soft errors can severely affect the normal operations of memory devices, and even lead to system errors. Previous research results indicate that soft errors fall into three categories, namely single-node-upsets (SNU), double-node-upset (DNU), and single-event transient (SET) [1, 4]. In the CMOS technology, the change of the logical state of a node in a memory cell caused by the strike of a particle is called an SNU. Due to the charge-sharing effect, a high energy radiative particle can cause the logical states of two nodes to change at the same time, resulting in a DNU. In combinational circuits, the particle striking can result in an instantaneous pulse, i.e., an SET, at the output of a logic gate.

Radiation effects account for roughly 45% of the abnormal factors of spacecrafts, with SNU as the major factor, with accounts for about 80% [5]. Therefore, SNU is a severe circuit-reliability problem. In order to mitigate this problem, researchers have proposed a series of methods [6-9]. However, along with the decrease of transistor sizes, the occurrence of DNU becomes more likely. To cope with the problem of DNU, researchers have proposed many hardened latches [10-16]. The double-node charge-sharing (DNCS) latch [10] can tolerate DNU but cannot provide DNU recovery. The double node upset tolerance (DONUT) latch [12] consists of four interlocked DICE units providing DNU recovery. However, there is strong current competition inside a DICE, making the overhead of this latch in terms of power and delay relatively large. The double-node-upset resilient latch (DNURL) [14] consists of three SNU-self-recoverable, frequency-aware and cost-effective (RFC) modules to avhieve DNU recovery. However, the area overhead of this latch is relatively large. In summary, the existing latches have the following major disadvantages.

(1) Some of them cannot completely tolerate DNU since there exists at least one counterexample in which such a latch outputs an invalid value when a DNU occurs.
(2) Some of them cannot provide DNU recovery since there exists at least one counterexample in which when such a latch suffers from a DNU, it can get correct output values but they cannot recover the impacted internal nodes to their correct states.
(3) Existing DNU recoverable latches have large overheads, especially in terms of area and power.

Note that some multiple-node-upset hardened latches have been proposed but they are mainly used for harsh radiation applications [17-18]. This paper proposes a DNU self-recoverable latch with low overhead in terms of power and area. The proposed latch mainly comprises seven 2-input C-elements (CEs) and two inverters to provide DNU self-recovery. Due to the use of fewer transistors, the proposed latch has a smaller area. The use of clock-controlled CEs enables the proposed latch to have low power. Simulation results demonstrate the DNU recovery of the proposed latch and also show that it can reduce delay by 45.71%, power by 29.13%, area by 65.93%, and area-power-delay-product (APDP) by 87.42% on average compared to the existing DNU self-recovery latches.

The rest of the paper is organized as follows. Section II reviews previous radiation hardened latch designs. Section III discusses the circuit structure, working principle and fault tolerance principle of the proposed latch. The area, delay, power and APDP of the proposed latch are compared with typical existing SNU/DNU hardened latches in Section IV. Section V concludes this paper.

II. Previous Radiation Hardened Latch Designs

Transmission gates and CEs are widely used in latch designs for fault tolerance. Figure 1 shows the transmission gate and the different types of CEs. The transmission gate is composed of a PMOS transistor and an NMOS transistor in

parallel. When the clock (CLK) signal is high and the negative clock (NCK) signal is low, its input and output are connected. It is a controllable switching circuit that can transmit both digital and analog signals. For a CE, if its inputs have the same value, it behaves as an inverter. If its input values change to be different, it will temporarily maintain the original output value. Regarding the clock-gating based CE, its behavior can also be controlled by the CLK and NCK signals.

In order to deal with the SNU/DNU problem, many hardened latch designs based on CEs have been proposed. This section briefly reviews typical existing hardened latches, namely high performance SNU tolerant (HPST) [8], RFC [9], DNCS [10], DeltaDICE [11], DONUT [12], non-temporally hardened latch (NTHLTCH) [13], DNURL [14], double node upset self-healing (DNUSH) [15] and highly robust and low delay DNU-recovery latch (HRLD) [16].

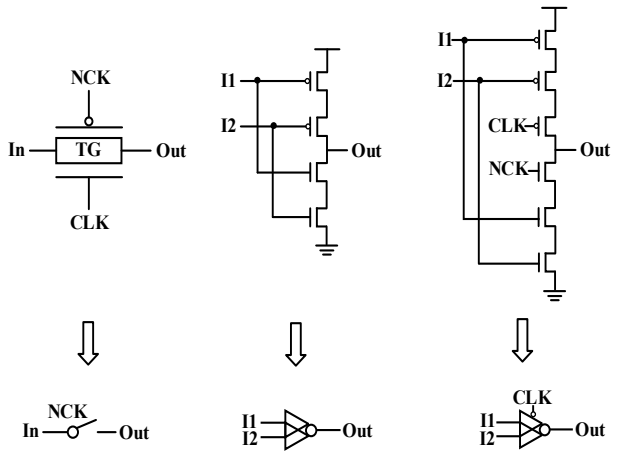

Fig. 1. Components. (a) transmission gate. (b) 2-input C-element. (c) Clock-gating based 2-input C-element.

A. HPST Latch

The HPST latch can tolerate SNU but cannot provide SNU recovery. It will enter the high impedance state at the output node if any input of the output-level CE becomes wrong; thus, its radiation-hardening ability needs to be further improved.

B. RFC Latch

The RFC latch can provide SNU recovery by using three CEs (one normal CE and two clock-gating based CEs) that are interconnected and interlocked. However, if two nodes suffer from a DNU, the latch will retain an invalid value. As a result, the latch is not DNU tolerant.

C. DNCS Latch

The DNCS latch can provide not only SNU recovery but also DNU tolerance. However, when two internal nodes are inverted by a DNU at the same time, the output cannot be recovered to the correct value. As a result, the latch is not DNU recoverable.

D. DeltaDICE Latch

The DeltaDICE latch contains three DICE modules, making it capable of tolerating DNU and providing DNU recovery. However, the internal current competition in DICE is severe, resulting in high power consumption.

E. DONUT Latch

The DONUT latch contains four interlocked modules and thus it can provide DNU recovery. But in transparent mode, due to current competition in feedback loops, this latch suffers from high power like the DeltaDICE latch.

F. NTHLTCH Latch

The NTHLTCH latch can provide DNU recovery through triple interlocked feedback loops consisting of nine 2-input CEs. However, more CEs lead to additional area and power overhead for this latch.

G. DNURL Latch

The DNURL latch uses three RFC modules so that it can provide DNU recovery. However, this latch has a large area because many transistors are used.

H. DNUSH Latch

The DNUSH latch consists of eight CEs forming multiple feedback loops, making it capable of providing DNU recovery. However, this latch also suffers from the problems of large area and delay.

I. HRLD Latch

All internal nodes of the HRLD latch are interlocked with redundancy and thus of its all node-pairs can recover from all possible DNUs. However, this latch also has large overhead in terms of power and area.

III. Proposed Hardened Latch Design

A. Circuit Structure and Behavior

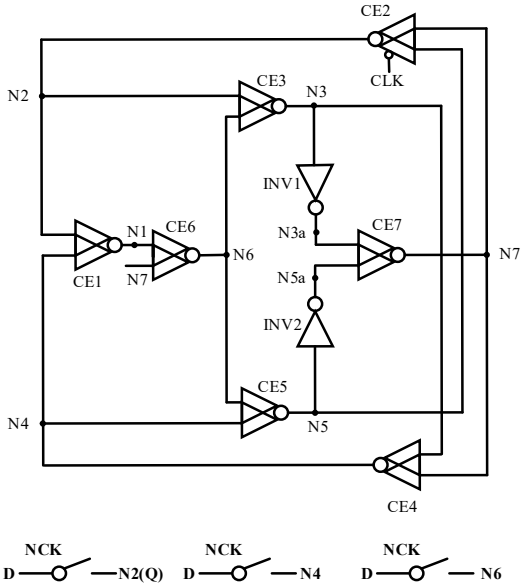

Fig. 2. Schematic of the proposed DSRL latch.

The circuit structure of the proposed DNU self-recovery latch design (referred to as DSRL here after) is presented in

Fig. 2. The figure shows that the latch consists of three transmission gates (TG1 to TG3), two inverters (INV1 and INV2) and seven 2-input CEs (CE1 to CE7). Note that CE2 is based on clock-gating. D and Q are the input and output of the latch, respectively. CLK and NCK are the system clock and negative system clock signals, respectively, and N1 to N7 are the internal nodes. When CLK = 0 and NCK = 1, the output, i.e., N2 (Q), of CE2, is used as the output of the latch; when CLK = 1 and NCK = 0, the output of the first transmission gate TG1 is used as the output of the latch.

When CLK = 1 and NCK = 0, the latch works in transparent mode. At this time, all TGs are ON, N2 (Q), N4, and N6 are initialized to the value of D. The above-mentioned nodes that have been initialized then determine the values of nodes N1, N3, N5, and N7 in Fig. 2 through CEs. Therefore, all nodes are initialized.

When CLK = 0 and NCK = 1, the latch works in hold mode. At this time, all TGs are OFF, N2 (Q) is determined by the output of the second C-element CE2, N4 by the output of the fourth C-element CE4, and N6 by the output of the sixth C-element CE6. The values of nodes N1, N3, N5, and N7 are the values initialized in transparent mode, and nodes N2 (Q), N4, and N6 feed nodes N1, N3, and N5 through three 2-input C-elements, nodes N3 and N5 feed node N7 through one 2-input C-element, and nodes N3, N5, and N7 feed nodes N2 (Q), N4, N6, and so on, forming several feedback loops. Therefore, this latch can effectively store values. In summary, the latch can work properly.

When the latch operates in hold mode, there are totally 21 (i.e., C_7^2) DNU cases. It can be seen from Fig. 2 that CE2 and CE4 are symmetrical and CE3 and CE5 are symmetrical. Thus, we only need to select nodes N2 (Q) and N3 with other nodes to discuss the DNU self-recoverability. Therefore, there are ten key DNU cases, which can be divided into two parts (namely Part I and Part II as follows).

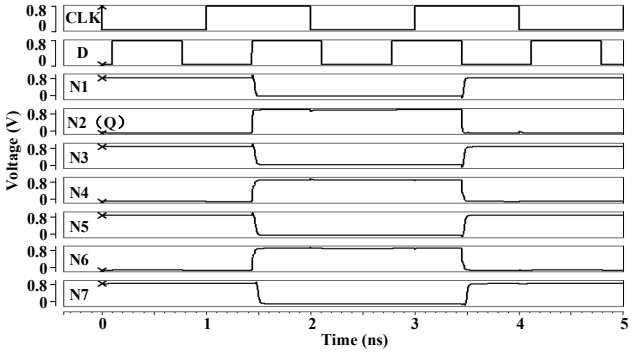

Fig. 3. Simulation results without any error injection of the proposed DSRL latch.

Part I: Two flipped nodes cannot affect other nodes (i.e., the two nodes are not the inputs of the same CE). There are seven node pairs in this case, namely <N1, N2 (Q)>, <N1, N3>, <N1, N6>, <N2 (Q), N3>, <N2 (Q), N7>, <N3, N6>, and <N6, N7>. For example, the node pair <N1, N2 (Q)> is affected by the DNU but the other nodes are not affected. At this time, N2 (Q) can recover to its previous correct value by inputting correct values of N5 and N7 into CE2; N1 can recover to its previous correct value by inputting correct values of N2 (Q) and N4 into CE1. Therefore, this node pair can provide DNU self-recovery. Since other node pairs are similar to <N1, N2 (Q)>, discussions about them are omitted here.

Part II: Two flipped nodes can affect other nodes (i.e., the two nodes are the inputs of the same CE). There are three node pairs in this case, namely <N1, N7>, <N2 (Q), N6>, and <N3, N7>. If the node pair <N1, N7> is affected by the DNU, N1 and N7 are the two inputs of CE6, then N6, which is the output node of CE6, is also affected, while all other nodes are unaffected. At this time, N1 can recover to its previous correct value by inputting correct values of N2 (Q) and N4 into CE1; N7 can recover to its previous correct value by inputting correct values of N3 and N5 into CE7; finally, since both N1 and N7 have recovered their correct values, N6 can recover to its previous correct value.

If the node pair <N2 (Q), N6> is affected by the DNU, N2 (Q) and N6 are the two inputs of CE3, then N3, which is the output node of CE3, is also affected, while all other nodes are unaffected. At this time, N2 (Q) can recover to its previous correct value by inputting correct values of N5 and N7 into CE2; N6 can recover to its previous correct value by inputting correct values of N1 and N7 into CE6; finally, since both N2 (Q) and N6 have recovered their correct values, N3 can recover to its previous correct value. If the node pair <N3, N7> is affected by the DNU, N3 and N7 are the two inputs of CE4, then N4, which is the output node of CE4, is also affected, while all other nodes are unaffected. At this time, N3 can recover to its previous correct value by inputting correct values of N2 (Q) and N6 into CE1; N7 can recover to its previous correct value by inputting correct values of N3 and N5 into CE7; finally, since both N3 and N7 have recovered their correct values, N4 can recover to its previous correct value. In summary, the proposed DSRL latch is completely DNU-recoverable (because all the DNU affected node pairs can self-recover from all DNUs).

B. Simulation Results

In this sub-section, we further verify the self-recovery of SNU/DNU of the DSRL latch. The simulations were performed by using an advanced 22nm CMOS technology with the Synopsys HSPICE tool. The supply voltage was set to 0.8V, and the working temperature was set to room temperature. The transistor sizes in the latch design were as follows: The PMOS transistors had W/L = 90nm/22nm and the NMOS transistors had W/L = 45nm/22nm.

In order to verify the error-free operations of the DSRL latch, extensive simulations were conducted without any error injection. Figure 3 shows the error-free simulation results of the proposed DSRL latch. The results demonstrate that the operations of the DSRL latch are the same as that of the conventional latch. This demonstrates the normal operational capability of the DSRL latch.

Figure 4 shows the simulation results for the SNU injections of the proposed DSRL latch. Aiming at validating the SNU resilience, an SNU with sufficient charge (i.e., 20fC for the worst case) was injected on single nodes of N1, N2 (Q), N3, N4, N5, N6 and N7, respectively. We can clearly see from the figure that any node can recover to its original

correct value, confirming that the latch is SNU self-recoverable.

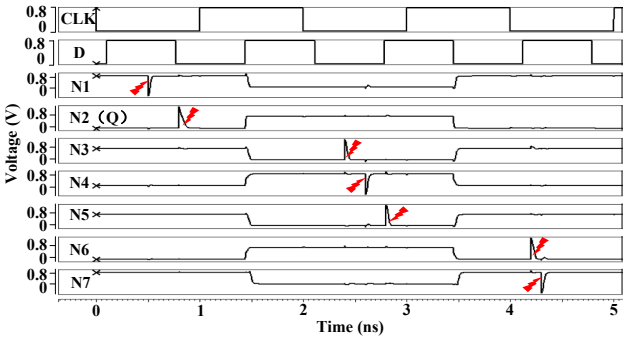

Fig. 4. Simulation results for the SNU injections of the proposed DSRL latch.

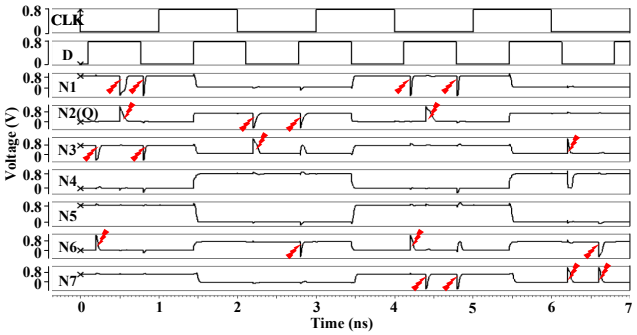

Fig. 5. Simulation results for the key DNU injections for the proposed DSRL latch.

The simulation results for the DNU injections at all key node pairs, i.e., <N1, N2 (Q)>, <N1, N3>, <N1, N6>, <N1, N7>, <N2 (Q), N3>, <N2 (Q), N6>, <N2 (Q), N7>, <N3, N6>, <N3, N7> and <N6, N7>, of the proposed DSRL latch, are shown in Fig. 5. At 0.5ns, 0.8ns, 4.2ns, 4.8ns, 2.2ns, 2.8ns, 4.4ns, 0.2ns, 6.2ns, 6.6ns, two SNUs with sufficient charge were injected at these node pairs to mimic DNU injections, respectively. It can be seen from the figure that the results clearly demonstrate that all the DNU-injected node pairs of the latch can recover from DNUs, respectively.

In summary, the above-mentioned simulation results can clearly verify the self-recoverability from SNUs/DNUs of the proposed DSRL latch. Note that in all the above-described simulations, we used a controllable double exponential current source model to perform all the DNU injections [17]. The time constants of the rise and fall of the current pulse were set to 0.1ps and 3.0ps, respectively.

IV. Latch Comparison and Evaluation

In this section, a comprehensive comparison (in term of overhead and radiation-hardening capability) of the proposed DSRL latch with typical existing DNU hardened latches is performed. To maintain comparison consistency, simulations of all latches were performed using HSPICE with the same conditions (supply voltage as well as operating temperature). The compared latches' transistor sizes were also optimized to match the sizes of the propose latch for a fair comparison.

As shown in Table I, the reliability of the proposed latch is compared with the other latches. The comparison includes four items, SNU Tolerance, SNU Recovery, DNU Tolerance and DNU Recovery. "Tolerance" refers to the ability to block the error caused by the corresponding SNU/DNU to ensure the correct logic value at the output; "Recovery" refers to the ability to not only block the error caused by SNU/DNU to ensure the correct logical value of the output but also enable the internal nodes where the error occurred to recover to their correct states. Table I shows that the HPST latch can tolerate SNU but cannot provide SNU recovery; the RFC latch can provide SNU recovery but cannot tolerate DNU; the DNCS latch can tolerate DNU but cannot provide DNU recovery; the DeltaDICE, DONUT, NTHLTCH, DNURL, RDTL, RHLD and the proposed DSRL latch can provide SNU and DNU recovery. However, in terms of area and power, our proposed latch has clear advantages compared with these existing latches with the same radiation-hardening capability. This will be discussed below.

TABLE I
Reliability Comparisons Among SNU and/or DNU Hardened Latch Designs

Latch	SNU Tolerance	SNU Recovery	DNU Tolerance	DNU Recovery
HPST [8]	Yes	No	No	No
RFC [9]	Yes	Yes	No	No
DNCS[10]	Yes	Yes	Yes	No
DeltaDICE [11]	Yes	Yes	Yes	Yes
DONUT [12]	Yes	Yes	Yes	Yes
NTHLTCH [13]	Yes	Yes	Yes	Yes
DNURL [14]	Yes	Yes	Yes	Yes
DNUSH [15]	Yes	Yes	Yes	Yes
HRLD [16]	Yes	Yes	Yes	Yes
DSRL (Proposed)	Yes	Yes	Yes	Yes

Table II shows the overhead comparison results of the DNU hardened latch designs, including four aspects in terms of delay, area, power, and APDP. Here, power denotes the average power (dynamic and static). Area is calculated using the method in [17]. Delay refers to the transfer delay from D to Q, which is the average of the rise and fall delays of D to Q. APDP was calculated by multiplying D to Q transmission delay, area and power. If the APDP of a latch is small, it means that the comprehensive overhead of the latch is better.

TABLE II
Overhead Comparison Results of the DNU Hardened Latch Designs

Latch	$10^{-4}\times$Area (nm^2)	Power (μW)	Delay (ps)	$10^{-2}\times$ APDP
DNCS [10]	8.60	2.35	65.41	13.22
DeltaDICE [11]	7.10	2.18	16.29	2.52
DONUT [12]	6.36	2.30	19.34	2.83
NTHLTCH [13]	11.37	2.27	13.19	3.40
DNURL [14]	13.93	1.18	4.02	0.66
DNUSH [15]	9.35	1.24	4.03	0.47
HRLD [16]	6.62	2.75	2.50	0.46
DSRL (Proposed)	5.94	0.61	3.00	0.11

Compared to the latches in Table II that can provide DNU tolerance, our proposed latch has the smallest area, power and APDP, and medium or even low delay. (***Area Comparison***)

From the second column in Table II, we can see that the area of both DNURL and NTHLTCH is large, mainly because these latches use more CEs and inverters. However, our proposed latch uses fewer CEs and inverters, making its area the smallest. (***Power Comparison***) From the third column in Table II, we can see that the proposed latch has the lowest power. The power of the HRLD latch is the highest, mainly because there is more current competition inside the latch. The DeltaDICE latch and the DONUT latch have higher power, mainly due to their special structure (the DICE module causes large current contention). Other latches have moderate power.

(***Delay Comparison***) From the fourth column in Table II, we can see that our proposed latch has a smaller transmission delay, which is only slightly larger than the HRLD latch. The reason is that the proposed latch and the HRLD latch have a high-speed transmission path in the D-Q path and use clock gating on the output-level of CE; thus, it reduces the current contention at Q to reduce delay. The delay of the DNCS latch is the largest mainly because it has no high-speed transmission path from D to Q. Other latches have moderate delay. (***APDP Comparison***) From the fifth column in Table II, we can see that our proposed latch has the smallest APDP among DNU hardening latches. This is because our proposed latch has the smallest area and power, and the delay is close to the minimum. Therefore, our proposed latch has the small overhead compared to most of the DNU recovery latches.

To quantitatively discuss the comparison results of the proposed latch with the same type of latches, delay (ΔDelay), area (ΔArea), power (ΔPower), and APDP (ΔAPDP) are calculated by the following equation. Table III shows the relative overhead comparisons of the DNU self-recoverable latch designs compared with ours. We can see in Table III that there is only one positive value and all the others are negative ones. Our proposed latch can reduce delay by 45.71%, area by 29.13%, power by 65.93% and APDP by 87.42% on average compared with other DNU recovery latches. In summary, the proposed DSRL latch have low overhead especially in terms of area, power and APDP.

$$\Delta\,(\%) = (\text{Overhead}_{\text{proposed}} – \text{Overhead}_{\text{compared}}) \,/\, \text{Overhead}_{\text{compared}} \times 100$$

TABLE III
RELATIVE OVERHEAD COMPARISONS OF THE DNU SELF-RECOVERABLE LATCH DESIGNS COMPARED WITH OURS

Latch	ΔArea (%)	ΔPower (%)	ΔDelay (%)	ΔAPDP (%)
DeltaDICE [11]	-16.34	-72.02	-81.58	-95.63
DONUT [12]	-6.60	-73.48	-84.49	-96.11
NTHLTCH [13]	-47.76	-73.13	-77.26	-96.76
DNURL [14]	-57.36	-48.31	-25.37	-83.33
DNUSH [15]	-36.47	-50.81	-25.56	-76.60
HRLD [16]	-10.27	-77.82	20.00	-76.09
Average	-29.13	-65.93	-45.71	-87.42

V. CONCLUSIONS

DNU-recoverable latches are critical to maintaining system reliability in nanometer technologies. In this paper, we have proposed a low overhead and DNU self-recoverable latch design. Compared with typical existing DNU self-recovery latches, our proposed latch has the lowest power and area, and a small delay. As a result, our proposed latch can be applied into safety-critical circuits and systems that both high reliability and cost-effectiveness are highly required.

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