Design of Low-Cost Approximate CMOS Full Adders

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Aibin Yan[1], Shaojie Wei[1], Zhixing Li[1], Jie Cui[1], Zhengfeng Huang[2], Patrick Girard[3], and Xiaoqing Wen[4]

[1]School of Computer Science and Technology, Anhui University, Hefei, China

[2]School of Microelectronic, Hefei University of Technology, Hefei, China

[3]Laboratory of Informatics, Robotics and Microelectronics of Montpellier, University of Montpellier / CNRS, Montpellier, France

[4]Graduate School of Computer Science and Systems Engineering, Kyushu Institute of Technology, Fukuoka, Japan

***Abstract*—The growing demand for data processing has brought severe challenges to computer performance. In order to improve the efficiency of data processing, approximate calculation can be used to replace accurate calculation in imprecision-tolerant applications. In this paper, we propose four approximate full adders with low overhead in term of power, delay and area. The proposed approximate full adders and the approximate full adders existing in the literature are classified into two groups according to their error distances. Simulation results show that the overhead of the proposed approximate full adders in each group is lower than that of the existing approximate full adders. Simulation results also show that, in the first group, the proposed approximate full adders can reduce Power-Area-Delay Product (PADP) by 61.83%, power consumption by 54.15%, area by 44.67%, and delay by 22.78% on average; in the second group, the proposed approximate full adders can reduce PADP by 97.01%, power consumption by 93.43%, area by 24.98%, and delay by 36.14% on average compared with the existing approximate full adders.**

***Index Terms*— Approximate calculation, approximate full adder, data processing, CMOS.**

I. Introduction

Since the beginning of the 21st century, the rapid development of the Internet has led to the exponential growth of information. The speed and scale of information collection and dissemination have reached an unprecedented level. Excessive amount of information brings great challenges to data processing. Nowadays, how to efficiently process massive data has become a crucial issue. Generally, an increase of data processing capability will lead to an increase in power consumption. To maintain the battery standby time, one can increase the battery capacity. However, this cannot reduce power consumption and can lead to an increase in cost and area. Obviously, this is not a good solution. Therefore, researchers are now trying to improve the ability of data processing by using alternative solutions.

In chip design, power consumption and area are important metrics for chip performance evaluation. In order to reduce the power consumption and area of a chip, researchers have proposed many effective solutions, e.g., supply voltage scaling, frequency scaling, transistor downscaling [1-3]. All of the above solutions have both advantages and disadvantages. For example, the power consumption of a circuit can be reduced by lowering the operating voltage of the circuit [1]. However, the downscaling of the metal oxide semiconductor field effect transistor (MOSFET) transistors, cause severe problems, such as current leakage exponential expansion, gate control reduction, short channel effects, and increasing fabrication expenses [1, 4-6].

In addition to the above solutions, related researchers have found that the power consumption and area of a circuit can be reduced by using approximate calculation. Approximate calculation can significantly reduce the overhead of a circuit with a small loss of accuracy. The design of approximate computing circuits has become increasingly mature, and the design of many approximate computing components has achieved high precision and low power. The approximate full adders are the most basic element in the approximate calculation circuits. Therefore, reducing their power consumption and area is very important.

The rise of new nanotechnologies has enabled the realization of approximate full adders in many ways, such as Quantum-dot Cellular Automata (QCA) [7-8], nanomagnetic logic (NML) [9], spin-wave devices (SWD) [10], and advanced Complementary Metal Oxide Semiconductor (CMOS) structure [11]. Therefore, many approximate full adders based on different technologies have been proposed. In [12], an approximate full adder based on the majority logic is implemented by using QCA. In [13], an approximate full adder is implemented by using the nanomagnetic logic. In [14], an approximate full adder with low power is implemented, and the realization of the approximate full adder adopts spin-wave devices. The structure of many full adders is implemented by CMOS, which will be introduced in detail in the second section.

As mentioned above, there are many approaches for implementing approximate full adders, and researchers have designed many approximate full adders. However, most of the existing approximate full adders, especially approximate full adders based on CMOS, have a common problem, i.e., their overhead (in terms of power consumption, area and delay) is large. To reduce the overhead of approximate full adders, four approximate full adders with low overhead are proposed in this paper. In the design of the proposed approximate full adders, for the first time we use the input signal as the clock control signal to implement the addition logic. The performance of the proposed four approximate full adders and existing approximate full adders is evaluated with HSPICE to demonstrate the low cost of the proposed four approximate full adders.

The rest of the paper is organized as follows. In Section II, we introduce typical approximate full adders and their error metrics. In Section III, we introduce the structure and

working principles of the proposed approximate full adders and verify the feasibility of their addition logic. The comparison of simulation results with other approximate full adders is presented in Section IV. Section V concludes the paper.

II. Review of Approximate Full Adders

In recent years, researchers have conducted different studies on approximate full adders [15-18]. Each of the previously proposed approximate full adder has both advantages and disadvantages, which are briefly discussed in this section.

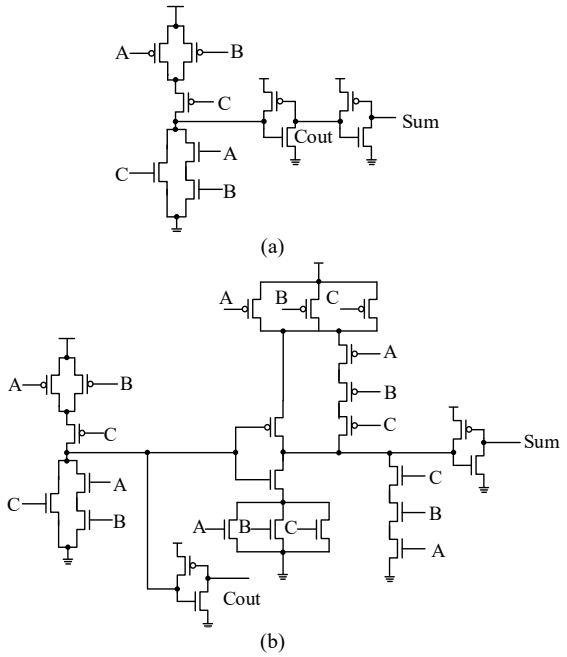

Fig. 1. The structure of the proposed approximate full adders in [15]. (a) Lau1, and (b) Lau2.

A. Error analysis metrics

In this subsection, different error analysis metrics are introduced to evaluate and compare approximate full adders. There are four error analysis metrics of approximate full adders, i.e., error distance (ED), error rate (ER), pass rate (PR), and relative error distance (RED). ED (see Eq. (1)) is equal to the absolute value of subtraction of the exact value (R) and the approximate value (R′) [19].

$$ED = |R - R'| \tag{1}$$

The ratio of the number of incorrect outputs to the total number of outputs is equal to ER (Eq. (2)), and PR is equal to 1−ER [19].

$$ER = \frac{No.\,of\ faulty\ outputs}{No.\,of\ outputs\ combinations} \tag{2}$$

RED is used to examine the errors in both outputs Sum and Cout distinctly (Eq. (3)) [19].

$$RED = \frac{ED_{Cout} + ED_{Sum}}{16} \tag{3}$$

In [20-21], the error analysis metrics are examined in detail.

B. Previous approximate full adders based on CMOS

Two approximate full adders are proposed in [15]. Figure 1 shows their structures. The first approximate full adder (Lau1) consists of 10 transistors, and the second approximate full adder (Lau2) consists of 24 transistors. Both structures have advantages and disadvantages. Lau1 has low delay, power and area. However, the ED of Lau1 is larger than Lau2. Although Lau1 and Lau2 implement approximate addition logic, they still use more transistors and consume more power (under the condition of low error rate).

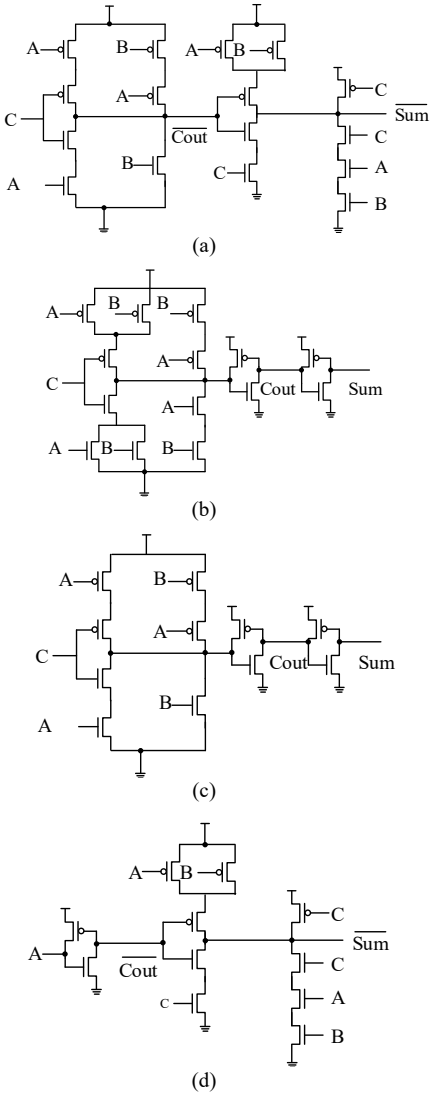

Fig. 2. The structure of the proposed approximate full adders in [16]. (a) MA1, (b) MA2, (c) MA3, and (d) MA4.

Four mirror adder (MA) approximate full adders are proposed in [16]. Figure 2 shows the structure of these approximate full adders The MA approximation full adder is modified from the mirror adder in [19], which produces approximate logic by removing the transistor in the mirror adder. The MA1 approximation full adder is obtained by removing 8 transistors from the mirror adder. The MA2 approximation full adder is obtained by removing 12 transistors from the mirror adder. The MA3 approximation full adder consists of 13 transistors (7 PMOS transistors and

6 NMOS transistors), which is 15 transistors less than the mirror adder. The MA4 approximation full adder also consists of 13 transistors, but MA4 consists of 5 PMOS transistors and 8 NMOS transistors. Four MA approximate full adders save much area and power consumption compared with exact full adders. However, the above MA approximation full adders still have a large number of transistors and consume high power (under the condition of low error rate).

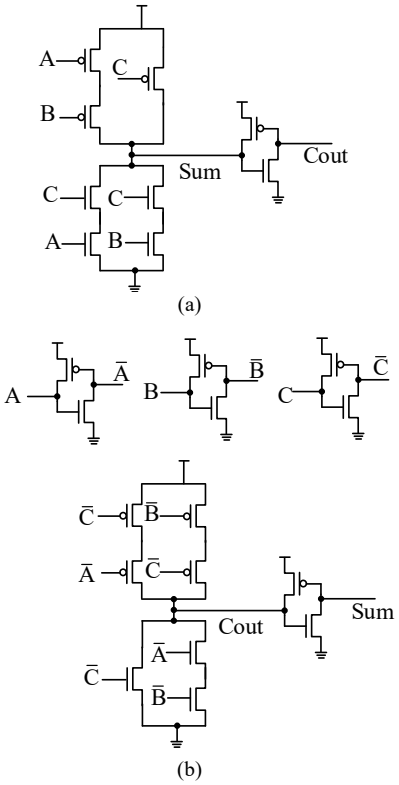

Fig. 3. The structure of the proposed approximate full adders in [17]. (a) FA1, and (b) FA2.

Four approximate full adders were proposed in [17]. Figure 3 shows the structure of the proposed approximate full adders in [17]. The first approximate full adder (FA1) consists of 9 transistors, and the second approximate full adder (FA2) consists of 15 transistors. The third and fourth approximate full adders (i.e., FA3 and FA4, not depicted in Fig. 3) have 9 and 7 transistors, respectively. However, the outputs of FA3 and FA4 are not full swing. Non-full swing output suffers from problems such as the inability to drive loads. Therefore, only FA1 and FA2 will be compared in the comparison section of this paper.

Three approximate full adders were proposed in [18]. Figure 4 shows the structure of the proposed approximate full adders in [18]. The first approximation full adder (AFA1) consists of 8 transistors, the second approximation full adder (AFA2) consists of 18 transistors, and the third approximation full adder (AFA3) consists of 14 transistors. Although the error rate of AFA1 is the same as that of AFA2, AFA1 uses fewer transistors. The structure of AFA3 is similar to that of AFA1, in which an XOR gate is added. However, AFA3 has a larger ED and a higher power and delay than AFA1. Although the three approximate full adders can implement approximate addition logic, they use more transistors and consume high power (under the condition of low error rate).

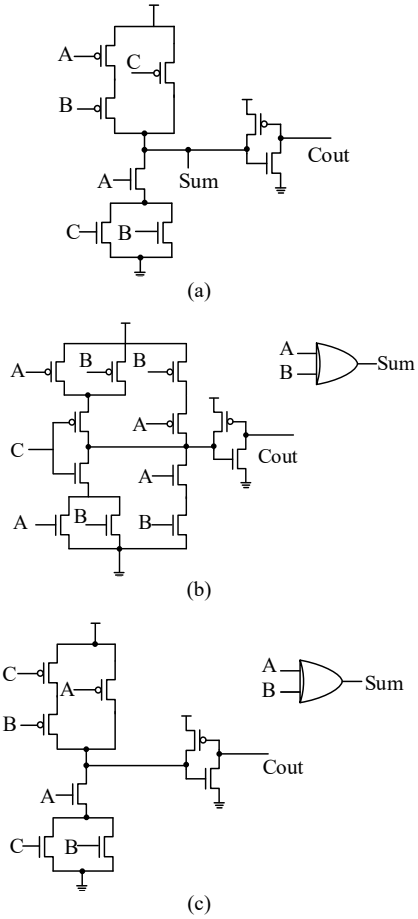

Fig. 4. The structure of the proposed approximate full adders in [18]. (a) AFA1, (b) AFA2, and (c) AFA3.

III. Proposed Approximate Full Adders

In this paper, four low-cost approximate full adders are proposed, i.e., LCAFA1, LCAFA2, LCAFA3, and LCAFA4. Figure 5 shows the structure of the proposed approximate full adders. In this section, we will introduce the principle, structure and simulation results of the proposed approximate full adders.

A. Circuit Structure and Behavior

As shown in Fig. 5, A, B, and C are the inputs of the proposed approximate full adders, Sum and carry out (Cout) are the outputs of the approximate full adders. Figure 5-(a) shows the structure of LCAFA1. LCAFA1 only uses 8 transistors, which saves 12 transistors compared to the MA. Although LCAFA1 uses a small number of transistors, the error rate of LCAFA1 is very small. Therefore, LCAFA1 has low overhead and high reliability. We can see from the structure of LCAFA1 that the output Sum of LCAFA1 is equal to $A \oplus B \oplus C$ and the output Cout of LCAFA1 is equal to C. The equations for the Cout and the Sum of LCAFA1 are as follows.

$$Sum = A \oplus B \oplus C \quad (4)$$

$$Cout = C \quad (5)$$

LCAFA2 consists of 9 transistors. Figure 5-(b) shows the structure of LCAFA2. Compared with LCAFA1, LCAFA2 has a higher error rate. However, compared with the existing approximate full adders, LCAFA2 has lower overhead when the ED is the same. The input C of LCAFA2 generates an opposite data $\overline{C}$ through an inverter. In LCAFA2, C and $\overline{C}$ are used as clock control signals. When C = 0, the transmission gate (TG) of LCAFA2 turns on. Therefore, the output Sum of LCAFA2 is equal to A ⊕ B. When C = 1, the TG of LCAFA2 turns off. Therefore, the output Sum of LCAFA2 is equal to B ⊕ C. The equations for the Cout and the Sum of LCAFA2 are as follows.

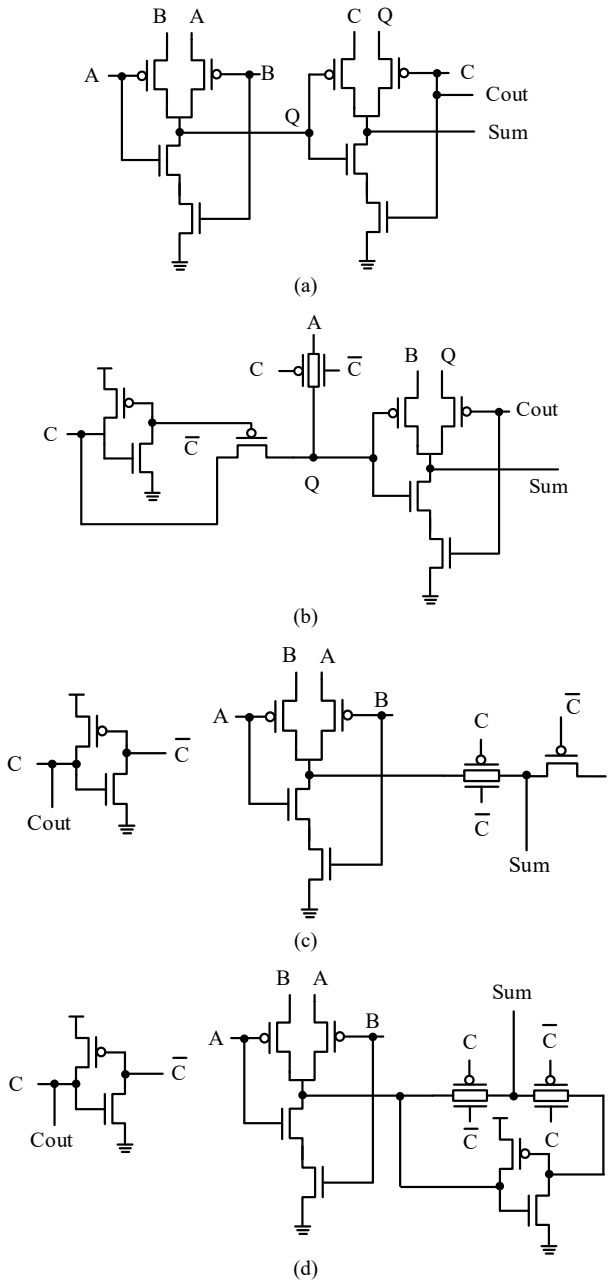

Fig. 5. The structure of the proposed approximate full adders. (a) LCAFA1, (b) LCAFA2, (c) LCAFA3, and (d) LCAFA4.

$$Sum = (A \oplus B)\bar{C} + (B \oplus C)C \quad (6)$$

$$Cout = C \quad (7)$$

LCAFA3 consists of 9 transistors. Figure 5-(c) shows the structure of LCAFA3. As for LCAFA2, the input C of LCAFA3 generates an opposite data $\overline{C}$ through an inverter. In LCAFA3, C and $\overline{C}$ are used as clock control signals to control the opening and closing of the TG. When C = 0, the TG of LCAFA3 turns off. Therefore, the output Sum of LCAFA3 is equal to A ⊕ B. When C = 1, the TG of LCAFA3 turns on. Therefore, the output Sum of LCAFA3 is equal to C. The equations for the Cout and the Sum of LCAFA3 are as follows.

$$Sum = (A \oplus B)\bar{C} + C \quad (8)$$

$$Cout = C \quad (9)$$

LCAFA4 is composed of 12 transistors. Figure 5-(d) shows the structure of LCAFA4, which contains two TGs, i.e., TG1 and TG2. LCAFA4 is the same as LCAFA2 and LCAFA3, and the input C of LCAFA4 also generates an opposite data $\overline{C}$ through an inverter. In LCAFA4, C and $\overline{C}$ are also used as clock control signals to control the opening and closing of TGs. When C = 0, TG1 turns on and TG2 turn off. Therefore, the output Sum of LCAFA4 is equal to A ⊕ B. When C = 1, TG1 turns off and TG2 turn on. Therefore, the output Sum of LCAFA4 is equal to the result of the inversion of A ⊕ B. The equations for the Cout and the Sum of LCAFA4 are as follows.

$$Sum = (A \oplus B)\bar{C} + \overline{(A+B)}C \quad (10)$$

$$Cout = C \quad (11)$$

Table I shows the truth table of the proposed approximate full adders and exact full adders. The circled entries in the truth table denote the instances in which the outputs of the proposed approximate full adders differ from exact full adders.

B. Simulation Results

The proposed approximate full adders were implemented in Synopsys HSPICE with an advanced 22nm CMOS technology model. The working temperature of the proposed approximate full adders were the room temperature and the supply voltage was 0.8 V. For transistor sizes, the PMOS transistors had the ratio W/L = 90nm/22nm, and the NMOS transistors had the ratio W/L = 45nm/22nm.

Figure 6 shows the simulation waveform of the proposed approximate full adders. In Fig. 6, Sum1, Sum2, Sum3, and Sum4 are the outputs (i.e., Sum) of LCAFA1, LCAFA2, LCAFA3 and LCAFA4, respectively. The Cout of LCAFA2

TABLE I
TRUTH TABLE OF THE PROPOSED APPROXIMATE FULL ADDERS AND EXACT FULL ADDERS

Input			Exact full adders		LCAFA1		LCAFA2		LCAFA3		LCAFA4	
C	B	A	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1	○,1	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	○,0	0	1	0	○,0	0	○,0
1	0	0	1	0	1	○,1	1	○,1	1	○,1	1	○,1
1	0	1	0	1	0	1	○,1	1	○,1	1	0	1
1	1	0	0	1	0	1	0	1	○,1	1	0	1
1	1	1	1	1	1	1	○,0	1	1	1	1	1

is Cout2, and the Cout of LCAFA1, LCAFA3 and LCAFA4 are all C. Simulation result shows that the waveforms of the proposed approximate full adders are all close to full swing.

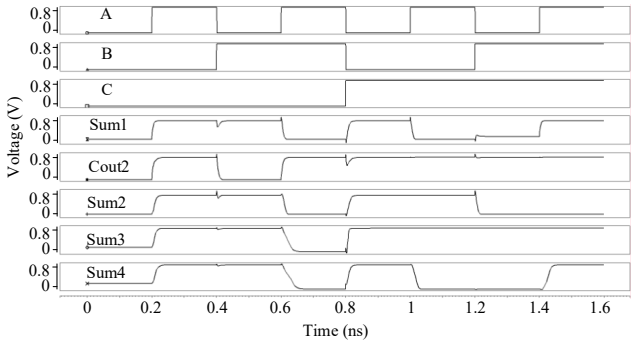

Fig. 6. The simulation waveform of the proposed approximate full adders.

IV. COMPARISONS

To make fair simulations, all the reference approximate full adders, i.e., LAU1, LAU2, MA2, MA3, FA1, FA2, AFA1, AFA2 and AFA3, have also been designed with the same conditions (i.e., 22nm CMOS technology, room temperature and 0.8V supply voltage).

The error analysis metrics for comparisons include ED, ER (Sum), ER (Cout) and RED. The cost analysis metrics for comparisons include delay, area, power, and PADP. The power consumption is the average of power (dynamic and static). The area refers to the sum of the areas of all CMOS in the approximate full adder. The delay refers to the delay from A to Sum, i.e., the average of the rise and fall delays of A to Sum. The PADP metric is calculated by multiplying power, area, and delay. Obviously, among the same type approximate full adder designs (e.g., ED = 2), a smaller PADP is better.

In order to fairly compare the performance of various approximate full adders, the reference approximate full adders and the proposed approximate full adders are divided into two groups according to ED (i.e., the first group with ED equal to 2 and the second group with ED equal to 4).

Table II shows the error analysis metrics of approximate full adders of the first group. The first group has four approximate full adders (i.e., LAU2, MA2, LCAFA1 and LCAFA4) with ED equals to 2. Although the ED of all approximate full adders in the first group is the same, their ER (Sum) and ER (Cout) are not the same. It can be seen that the ER (Sum) of each proposed approximate full adder is equal to 0 so that it makes the Sum of each proposed approximate full adder equals to that of the exact full adder.

Table III shows the cost comparison of the approximate full adders of the first group. Simulation results shows that the proposed first approximate full adder (i.e., LCAFA1) has the lowest power, the smallest delay and area. According to Table III, it can be calculated that, compared with LAU2, LCAFA1 can reduce PADP by 98.64%, power consumption by 93.35%, area by 60.27%, and delay by 48.36%. Compared with MA2, LCAFA1 can reduce PADP by 98.86%, power consumption by 90.18%, area by 50.42%, and delay by 76.58%. Compared with LAU2, LCAFA2 can reduce PADP by 17.53%, power consumption by 29.75%, and area by 40.67%. Compared with MA2, LCAFA2 can reduce PADP by 31.06%, area by 25.21%, and delay by 11.18%. From the comparison results, it can be seen that the proposed approximate full adders can significantly reduce overhead (especially in the case where ED is equal to 2).

TABLE II
ERROR ANALYSIS METRICS OF APPROXIMATE FULL ADDERS OF THE FIRST GROUP

Design	ED	ER (Sum)	ER (Cout)	RED
LAU2 [15]	2	1/8	1/8	2/16
MA2 [16]	2	2/8	0	2/16
LCAFA1	2	0	2/8	2/16
LCAFA4	2	0	2/8	2/16

TABLE III
COST COMPARISON OF APPROXIMATE FULL ADDERS OF THE FIRST GROUP

Design	10×Power (uw)	10^{-4}×Area (nm^2)	Delay (ps)	PADP
LAU2 [15]	9.78	2.97	7.3	212.04
MA2 [16]	6.62	2.38	16.1	253.67
LCAFA1	0.65	1.18	3.77	2.89
LCAFA4	6.87	1.78	14.3	174.87

Table IV shows the error analysis metrics of approximate full adders of the second group. For the second group, the ED of all the approximate full adders equals to 4. Note that AFA3 has an ED of 5 which is close to 4 so that we merge it into the

second group. It can be seen that the ER (Sum) of each proposed approximate full adder in the second group is the smallest, i.e., the output Sum of each proposed approximate full adder is the closest to the real Sum compared with other approximate full adders in the second group.

Table V shows the cost comparison of approximate full adders of the second group. As shown in Table V, there are 9 approximate full adders. Simulation results show that the proposed first approximate full adder (i.e., LCAFA2) of the second group has the lowest power and the smallest delay. According to Table V, it can be calculated that, compared with all the reference approximate full adders in the second group, LCAFA2 can reduce PADP by 97.86%, power consumption by 93.98%, area by 24.98%, and delay by 49.23% on average. Compared with all the reference approximate full adders in the second group, LCAFA3 can reduce PADP by 96.16%, power consumption by 92.89%, area by 24.98%, and delay by 23.05% on average. From the comparison results, it can be concluded that, in the case where ED is equal to 4, the proposed approximate full adders can significantly reduce overhead.

TABLE IV
ERROR ANALYSIS METRICS OF APPROXIMATE FULL ADDERS OF THE SECOND GROUP

Design	ED	ER (Sum)	ER (Cout)	RED
LAU1 [15]	4	3/8	1/8	4/16
MA3 [16]	4	3/8	1/8	4/16
FA1 [17]	4	3/8	1/8	4/16
FA2 [17]	4	3/8	1/8	4/16
AFA1 [18]	4	3/8	1/8	4/16
AFA2 [18]	4	4/8	0	4/16
AFA3 [18]	5	4/8	1/8	5/16
LCAFA2	4	2/8	2/8	4/16
LCAFA3	4	2/8	2/8	4/16

TABLE V
COST COMPARISON OF APPROXIMATE FULL ADDERS OF THE SECOND GROUP

Design	10×Power (uw)	10^{-4}×Area (nm^2)	Delay (ps)	PADP
LAU1 [15]	9.20	1.49	9.85	135.02
MA3 [16]	7.41	1.98	17.3	253.82
FA1 [17]	6.8	1.29	13.2	115.79
FA2 [17]	10.3	2.28	15.2	356.96
AFA1 [18]	6.24	1.18	7.37	54.27
AFA2 [18]	13.14	2.67	10.71	375.75
AFA3 [18]	10.86	2.08	9.24	208.72
LCAFA2	0.55	1.39	6.01	4.59
LCAFA3	0.65	1.39	9.11	8.23

V. CONCLUSIONS

In this paper, we have investigated the design of approximate full adders and have proposed four approximate full adders with low overhead in term of power, area and delay. We have evaluated their performance using HSPICE. Simulation results have shown that the proposed approximate full adders have lower overhead, compared with the typical approximate full adders that have the same error variations.

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