A Low Area and Low Delay Latch Design with Complete Double-Node-Upset-Recovery for Aerospace Applications

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ABSTRACT

In this paper, we propose a double-node-upset recoverable latch that can completely recover from all possible double-node-upsets (DNUs) with low area and low delay. The latch consists of seven 2-input C-elements (CEs) implemented in 22nm complementary metal oxide semiconductor (CMOS) technology, making it area-efficient. The proposed latch employs the clock gating methodology and a high-speed transmission path, enabling it to perform with lower overhead in terms of transmission delay and power dissipation. Simulation results demonstrate that the proposed latch can provide complete DNU recovery. Compared with typical double-node-upset-recoverable latches, the proposed latch can save 89.74% of Area-Delay-Power Product (ADPP) on average.

CCS CONCEPTS

• **Hardware → Circuit hardening; transient errors and upsets; fault tolerance; error correction; redundancy.**

KEYWORDS

Circuit reliability, radiation hardening, soft error, robust computing.

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1 Introduction

With the development of complementary metal oxide semiconductor (CMOS) manufacturing technologies, the feature sizes of transistors continue to shrink. The shrinking of transistor sizes reduces the power consumption and silicon area of integrated circuits. However, the excessive shrinking of transistor sizes can reduce supply voltages and critical charge on circuit nodes, making circuits susceptible to radiations that can lead to soft errors [1]. Soft errors are caused by the hit of high-energy radiative particles, such as high energy neutrons, α rays, heavy ions, and electrons [2]. The collisions of α rays and neutrons, etc., can create electrons and holes (in impacted transistors) that can be collected at the drain of the transistors. The collected electrons and holes can lead to transient voltage disturbance [3]. As a result, the node value of a storage device can be flipped, causing a single-node-upset (SNU) [4].

Nanoscale CMOS storage cells are susceptive to soft errors in radiation environments. Therefore, for radiation hardening of CMOS storage cells, researchers mostly focus on the designs of latches [5-19]. Previously, researchers mainly focused on reliability design against SNUs. However, the continuous transistor shrinking and high integration of circuits have led to the emergence of double-node-upsets (DNUs) due to charge-sharing [20]. In order to mitigate the impact of DNUs on circuit reliability, researchers have done a large amount of work. As a result, many DNU-hardened latches were proposed. However, most of these latches cannot self-recover from DNUs. If a latch cannot self-recover from DNUs, the errors can be accumulated (an SNU-recoverable latch cannot recover from DNUs). Moreover, although some existing latches can self-recover from DNUs, most of these latches have high power consumption, large transmission delay, and large silicon area. Therefore, a low-cost design of DNU-recovery latches is highly required for aerospace applications.

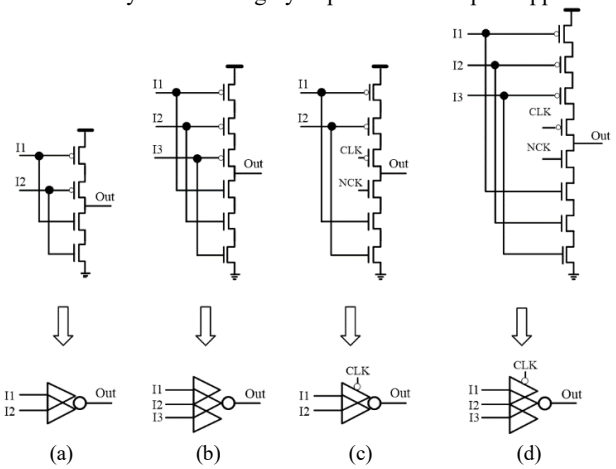

Figure 1: Structure of C-elements. (a) 2-input C-element, (b) 3-input C-element, (c) clock-gating-based 2-input C-element and (d) clock-gating-based 3-input C-element.

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In order to mitigate the impact of SNUs and DNUs on latch reliability, a cost-effective DNU-resilient latch design is proposed in this paper and implemented in a 22 nm CMOS technology. The proposed latch has been simulated with Synopsys HSPICE, and the simulation results demonstrate the DNU recovery as well as the cost-effectiveness in terms of transmission delay, silicon area and power consumption of the proposed latch. The proposed latch has the smallest transmission delay, silicon area and Area-Delay-Power Product (ADPP) than the existing latches that can recover from DNUs.

The rest of the paper is organized as follows. In Section 2, the conventional radiation hardened schemes of latches are reviewed. In Section 3, we introduce the structure, working principles, and reliability verifications of the proposed latch. A comparison of simulation results with other latches is provided in Section 4. Section 5 concludes the paper.

2 Previous Hardened Latches

Among the existing hardened latches, C-elements (CEs) are widely used. Figure 1 shows the structure of CEs. This section reviews typical hardened latches with CEs as main components. Some typical SNU and DNU tolerant latch designs are presented in Fig. 2, such as the high robust and low cost (HRLC) [11], low cost and highly reliable (LCHR) [12], high performance, low-cost, and double node upset tolerant latch enhanced version (HLDTL-EV) [13], dual-input inverter radiation tolerant (DIRT) [14], radiation hardened (RH) [15], double node charge sharing (DNCS) [16], non-temporally hardened latch (NTHLTCH) [17], double node upset self-healing (DNUSH) [18], and high robust and cost effective (HRCE) [19].

As shown in Fig. 2-(a), the HRLC latch is mainly composed of two parts. One part consists of four interlocked input-output-coupled inverters, and the other part consists of a Schmitt trigger inverter marked with S, a 2-input CE, two transmission gates (TG) marked with negative system clock (NCK) and two inverters. The HRLC latch can tolerate SNUs, but the latch is not DNU tolerant, and not SNU/DNU resilient. Therefore, the HRLC latch cannot guarantee high reliability when it suffers from DNUs. As shown in Fig. 2-(b), the LCHR latch employs seven inverters, three TGs marked with NCK,

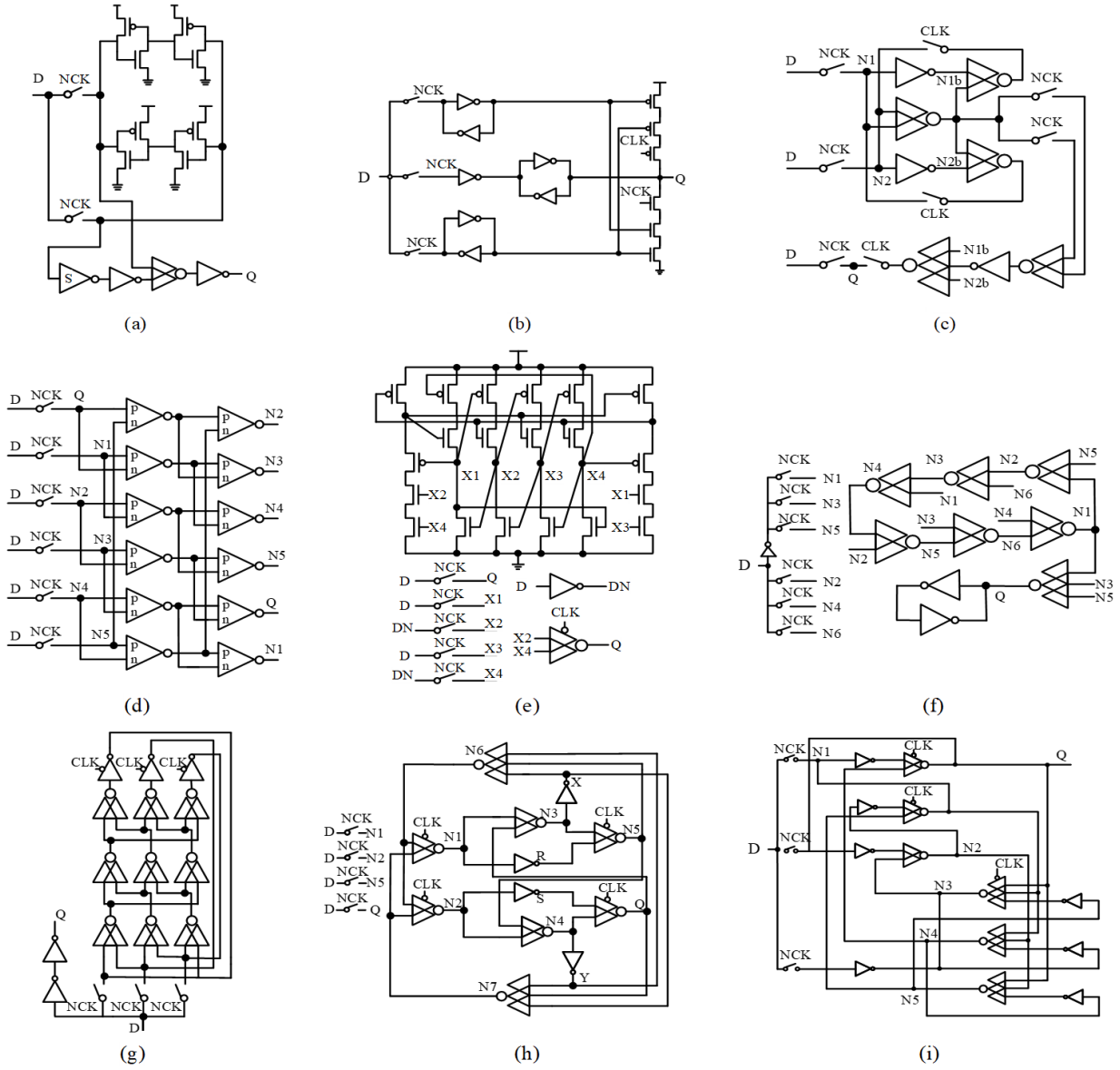

Figure 2: Schematics of existing hardened latches. (a) HRLC [11], (b) LCHR [12], (c) HLDTL-EV [13], (d) DIRT [14], (e) RH [15], (f) DNCS [16], (g) NTHLTCH [17], (h) DNUSH [18], and (i) HRCE [19].

and a 2-input CE to robustly retain values. The LCHR latch can tolerate SNUs, but it is not DNU tolerant/resilient. Therefore, the LCHR latch cannot guarantee high reliability when it suffers from DNUs.

As shown in Fig. 2-(c), the HLDTL-EV latch is mainly composed of two parts. The first part is an SNU Resilient Cell (SRC), and the other part is at the bottom of the latch (this part includes a 3-input CE, a 2-input CE, a TG, and an inverter). The HLDTL-EV latch can tolerate SNUs and DNUs, but it is not DNU resilient. Therefore, the HLDTL-EV latch cannot recover from DNUs. As shown in Fig. 2-(d), the DIRT latch mainly consists of twelve inverters and six TGs. The DIRT latch can tolerate SNUs and DNUs, and self-recover from SNUs, but it is not DNU resilient. Therefore, the DIRT latch cannot recover from DNUs. As shown in Fig. 2-(e), the RH latch is based on an extended dual interlocked storage cell (DICE). It can tolerate SNUs and DNUs, and self-recover from SNUs, but the latch is not DNU resilient. Therefore, the RH latch cannot self-recover from DNUs. As shown in Fig. 2-(f), the DNCS latch consists of six 2-input CEs, a 3-input CE, six TGs, and two inverters. The DNCS latch can tolerate SNUs and DNUs, and self-recover from SNUs. However, the latch cannot self-recover from DNUs.

As shown in Fig. 2-(g), the NTHLTCH latch consists of nine 2-input CEs, three clock gating (CG) based inverters, three TGs, and two inverters. The NTHLTCH latch can tolerate SNUs and DNUs, and self-recover from SNUs and DNUs. However, the latch has a large transmission delay, large area, and high-power dissipation. Therefore, the ADPP of the latch is also large. As shown in Fig. 2-(h), the DNUSH latch consists of four CG-based 2-input CEs, two 2-input CEs, four inverters, two 3-input CEs, and four TGs. The DNUSH latch can tolerate SNUs and DNUs, and self-recover from SNUs and DNUs. However, the latch has a large transmission delay and large area. Therefore, the ADPP of the latch is also large. As shown in Fig. 2-(i), the HRCE latch consists of two CG-based 2-input CEs, a 2-input CE, a CG-based 3-input CE, two 3-input CEs, seven inverters, and three TGs. The HRCE latch can tolerate SNUs and DNUs, and self-recover from SNUs and DNUs. However, the latch has a large transmission delay, high power dissipation and large area. Therefore, the ADPP of the latch is also large. Note that some researchers also proposed latches that are multiple-node-upset tolerant/resilient [5-6] but at the cost of more extra overhead especially in terms of silicon area, power and ADPP.

3 Proposed Hardened Latch Design

3.1 Circuit Structure and Behavior

Figure 3 shows the schematic of the proposed latch. There are seven CEs, three TGs and five inverters in this latch. CEs are the main component of the proposed latch. Among the seven CEs, there are six normal 2-input CEs and a CG-based 2-input CE. Fig. 2-(a) and Fig. 2-(b) show the structure of the 2-input CE and the CG-based 2-input CE, respectively. When the inputs of a CE have the same value, it outputs the reversed value of the inputs. If the inputs of a CE have different values, the CE's output temporarily remains its original state. A CG-based CE can also be controlled by the system clock (CLK) and the NCK signals, simultaneously. In the latch, D is the input, N2 (Q) is the output, and D is connected to N2, N6 and N7b to pre-charge the latch. When CLK is high and NCK is low, all transistors in TGs are ON and the latch is working in transparent mode. Hence, D is propagated to output Q, N6 and N7b through TG1, TG2 and TG3, respectively, and then each node gets the corresponding value. When CLK is low and NCK is high, the latch is working in hold mode. In hold mode, all the transistors in TGs are OFF. At this time, D cannot propagate to Q, N6 and N7b. All CEs in the latch form several feedback loops, and each node maintains the correct values.

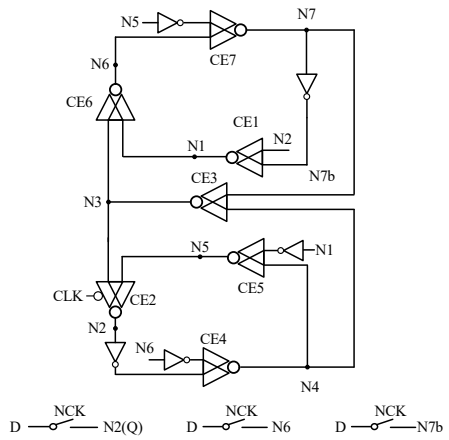

Figure 3: Schematic of the proposed latch. Note that when CLK = 1 all transistors in TGs are ON and the latch works in transparent mode; when CLK = 0 all transistors in TGs are OFF and the latch works in hold mode.

According to the characteristics of CEs, when an input of a CE flips, the output of the CE remains unaffected, which allows the proposed latch to tolerate SNUs. There are multiple feedback loops in the latch. Therefore, the latch has internal feedback rules. When a node in the latch is flipped, since other nodes in the feedback loops are not changed, the node will recover to the correct state. On the other hand, there are two situations in which a DNU occurs in the latch. If two nodes suffering from a DNU are not the inputs of the same CE, according to the characteristics of the CE, the output of the CE remains unaffected. If two nodes suffering from a DNU are the inputs of the same CE, the output of the CE will enter an error state. Both situations are discussed below.

The following is the case where the input and output of a CE suffer from a DNU at the same time, i.e., two nodes are flipped by a DNU (one node is the input of a CE and the other is the output of the same CE). In this case, the CE's output will hold the wrong value and will need recovery from the other formed feedback loop to restore the correct state. Due to the looped structure of the latch, the representative key node-pairs are <N1, N5>, <N5, N7>, <N6, N7>, <N3, N7>, and <N2, N3>.

When <N1, N5> is impacted by a DNU, N1 and N5 are temporally flipped. Since the two inputs N2 and N7 of CE1 are not changed, N1 can recover through CE1. After N1 is restored, both inputs of CE5 are correct, so that N5 can be recovered through CE5. Therefore, <N1, N5> can recover from the DNU. In a similar manner, <N1, N2> can also recover from a DNU.

When <N5, N7> is impacted by a DNU, N5 and N7 are temporally flipped. Since two inputs N1 and N4 of CE5 are not changed, the output of CE5 is recovered to the correct value, then, N5 can recover through CE5. After N5 is restored, both inputs of CE7 are correct, so that N7 can be recovered through CE7. Therefore, <N5, N7> can recover from the DNU. In a similar manner, <N4, N6> can also recover from a DNU.

When <N6, N7> is impacted by a DNU, N6 and N7 are temporally flipped. Since the two inputs N1 and N3 of CE6 are not changed, the output of CE6 is recovered to the correct value, then, N6 can recover through CE6. After N6 is restored, both inputs of CE7 are correct, and thus N7 can be recovered through CE6. Therefore, <N6, N7> can recover from the DNU. In a similar manner, <N1, N6>, <N1, N7>, <N2, N4>, <N2, N5> and <N4, N5> can also recover from a DNU.

When <N3, N7> is impacted by a DNU, N7 and N3 are temporally flipped. Since the two inputs N5 and N6 of CE7 are not changed, the output of CE7 is recovered to the correct value, then N7 can recover through CE7. After N7 is restored, both inputs of CE3 are correct, and thus N3 can be recovered through CE3. Therefore, <N7, N3> can recover from the DNU. In a similar manner, <N3, N4> can also recover from a DNU.

When <N2, N3> is impacted by a DNU, N2 and N3 are temporally flipped. Since the two inputs N4 and N7 of CE3 are not changed, the output of CE3 is recovered to the correct value, then N3 can recover through CE3. After N3 is restored, both inputs of CE2 are correct, and thus N2 can be recovered through CE2. Therefore, <N2, N3> can recover from the DNU. In a similar manner, <N3, N6> can also recover from a DNU.

The following is the case where both inputs of a CE suffer from a DNU at the same time. In the latch, CE1, CE6, and CE7 are symmetrical with CE2, CE4, and CE5. Due to the symmetrical structure of the latch, we only need to discuss the situations where a DNU occurs at the inputs of CE1, CE3, CE6, and CE7, respectively. Therefore, the simultaneous flipping of two inputs of a CE can be divided into four sub-cases, i.e., sub-cases 1 to 4 in the following.

Case 1: The two inputs of CE1 are flipped, i.e., N2 and N7 are flipped. At this time, the output of CE1 will enter an error state. Since the two input nodes N5 and N6 of CE7 are not changed, N7 can return to the correct state. Similarly, the two input nodes N3 and N5 of CE2 are not changed. Thus, N2 returns to the correct state, and then the output of CE1 returns to the correct state. Therefore, <N2, N7> can recover from the DNU. In a similar manner, <N1, N4> can also recover from a DNU.

Case 2: The two inputs of CE3 are flipped, i.e., N4 and N7 are flipped. Due to the characteristics of CEs, the output of CE3 will enter an error state. Since the two input nodes N5 and N6 of CE7 are not changed, N7 can return to the correct state. Similarly, the two input nodes N2 and N6 of CE4 are not changed. Thus, N4 returns to the correct state, and then the output of CE3 returns to the correct state. Therefore, <N4, N7> can recover from the DNU.

Case 3: The two inputs of CE6 are flipped, i.e., N1 and N3 are flipped. When N1 and N3 suffer from a DNU, the output of CE6 will enter an error state. Since the two input nodes N2 and N7 of CE1 are not changed, N1 can return to the correct state. Similarly, the two input nodes N4 and N7 of CE3 are not changed, N3 returns to the correct state, and then the output of CE6 returns to the correct state. Therefore, <N1, N3> can recover from the DNU. In a similar manner, <N3, N5> can also recover from a DNU.

Case 4: The two inputs of CE7 are flipped, i.e., N5 and N6 are flipped. When N5 and N6 suffer from a DNU, the output of CE7 will enter an error state. Since the two input nodes N1 and N4 of CE5 are not changed, N5 returns to the correct state. Similarly, two input nodes of CE6 (i.e., N1 and N3) are not changed. Thus, N6 returns to the correct state, and then the output of CE7 returns to the correct state. Therefore, <N5, N6> can recover from the DNU. In a similar manner, <N2, N6> can also recover from a DNU.

The above description of the working principles of the latch shows that the proposed latch design can provide complete DNU-recoverability. Obviously, the proposed latch design can also provide complete SNU-recoverability.

3.2 Simulation Results

The proposed latch was simulated/implemented in Synopsys HSPICE with an advanced 22 nm CMOS technology model. The working temperature of the latch was the room temperature and the supply voltage was 0.8 V. Regarding transistor sizes, the PMOS transistors had the ratio W/L=90nm/22nm, and the NMOS transistors had the ratio W/L=45nm/22nm.

Figure 4 shows the simulation result for the error-free case of operations of the proposed latch design. The proposed latch works in transparent mode when the clock signal CLK is high, and the proposed latch works in hold mode when the clock signal CLK is low. The simulation results show that the state of the output (i.e., Q) of the latch changes along with the input (i.e., D) in transparent mode and the output of the latch remains unchanged in hold mode. Note that, in the following simulations, we inject the SNU and DNU errors when CLK = 0 (i.e., the latch works in hold mode). Also note that there is no impact in transparent mode when CLK = 1.

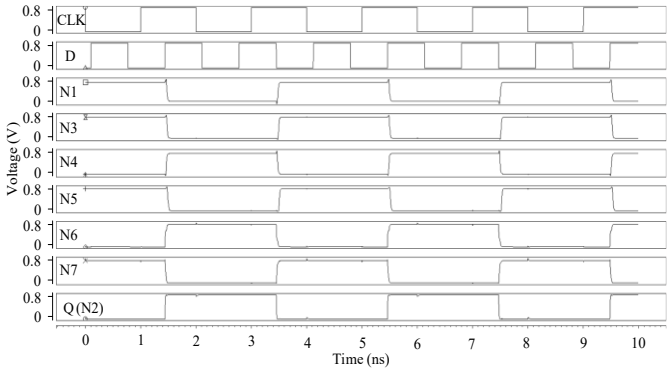

Figure 4: Simulation result for the error-free case of operations of the proposed latch.

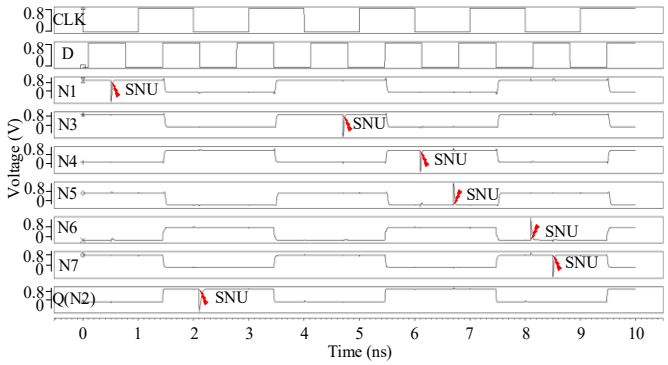

Figure 5: Simulation results for the key SNU injections of the proposed latch.

Let us first consider SNUs. To perform complete simulations, all single nodes of the latch were injected with SNU errors. Figure 5 shows the simulation results for the key SNU injections of the proposed latch. As shown in Fig. 5, when CLK = 0, an SNU was injected on nodes N1, Q, N3, N4, N5, N6, and N7 at 0.3ns, 2.1ns, 4.7ns, 6.1ns, 6.7ns, 8.1ns, and 8.5ns, respectively. Note that, the lighting marks in Fig. 5 denote the injected errors. The simulation results show that the states of all nodes injected with SNUs can recover in a short time. Therefore, the proposed latch can self-recover from these injected SNUs.

Let us now consider DNUs. Similarly, to perform the complete simulations, all node-pairs in the latch were injected with DNU errors. Figure 6 shows the simulation results for the key DNU injections of the proposed latch. Table I shows statistical results for the complete key DNU injections of the proposed latch design according to Fig. 6. In Table I, "Time" denotes the injection time, "DNUs" denotes the injected DNUs on the key nodes, and "State" denotes the correct state of Q. When CLK = 0, a DNU was injected on these node-pairs at 1.1ns, 1.3ns, 1.5ns, 1.7ns, 2.1ns, 2.3ns, 2.5ns, 2.7ns, 4.1ns, 4.3ns, 4.5ns, 4.7ns, 6.1ns, 6.3ns, 6.5ns, 6.7ns, 8.1ns, 8.3ns, 8.5ns, 8.7ns, and 10.1ns, respectively. Note that, the lighting marks in Fig. 6 denote the injected DNU errors (we simultaneously injected two SNUs to mimic a DNU).

The simulation results show that the states of all nodes injected with DNUs can recover in a short time. Therefore, the proposed latch can self-recover from these injected DNUs. In summary, the simulation results show that the proposed latch can recover from SNUs and DNUs providing high reliability (with low cost that will be introduced in the following section).

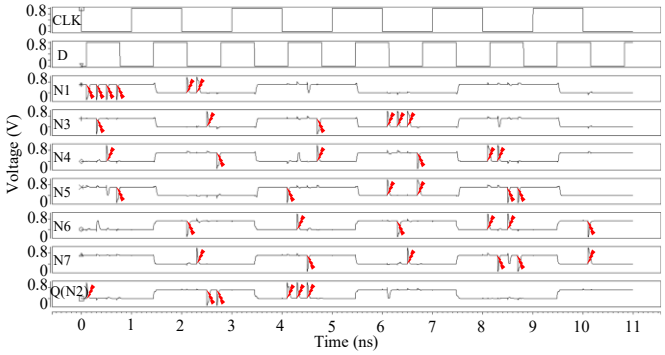

Figure 6: Simulation results for the key DNU injections of the proposed latch.

TABLE I

Statistic Results for the Complete Key DNU Injections of the proposed Latch According to Figure 6.

Time (ns)	DNUs	State	Time (ns)	DNUs	State
1.1	N1, Q	Q=0	4.7	N3, N4	Q=0
1.3	N1, N3	Q=0	6.1	N3, N4	Q=1
1.5	N1, N4	Q=0	6.3	N3, N4	Q=1
1.7	N1, N5	Q=0	6.5	N3, N4	Q=1
2.1	N1, N6	Q=1	6.7	N4, N5	Q=1
2.3	N1, N7	Q=1	8.1	N4, N6	Q=0
2.5	Q, N3	Q=1	8.3	N4, N7	Q=0
2.7	Q, N4	Q=1	8.5	N5, N6	Q=0
4.1	Q, N5	Q=0	8.7	N5, N7	Q=0
4.3	Q, N6	Q=0	10.1	N6, N7	Q=1
4.5	Q, N7	Q=0			

4 Comparisons

To make a fair comparison, the reference latches in Fig. 2, i.e., HRLC, LCHR, HLDTL-EV, DIRT, RH, DNCS, NTHLTCH, DNUSH, and HRCE latch designs, have also been designed and simulated with the same conditions (i.e., 22 nm CMOS technology, room temperature and 0.8V supply voltage).

Table II shows the comparisons among radiation hardened latch designs. The metrics for comparisons include transmission delay, silicon area measured as in [21], power consumption, and ADPP. The transmission delay refers to the delay from D to Q, i.e., the average of the rise and fall delays of D to Q. The power consumption is the average of power (dynamic and static). The ADPP metric is calculated by multiplying area, D to Q transmission delay, and power consumption. Obviously, among the same type latch designs (e.g., DNU tolerant ones), a smaller ADPP is better.

It can be seen from Table II that, compared to the latches such as HRLC, LCHR, and DIRT, SNU and DNU hardening requires more area with the proposed latch design. However, the proposed latch has the smallest transmission delay and the smallest ADPP compared with DNU recoverable latches (NTHLTCH, DNUSH, and HRCE).

As shown in Table II, compared with the HLDTL-EV latch, the proposed latch has a higher power consumption and a larger transmission delay but it can self-recover from SNUs and DNUs. Therefore, the proposed latch is more reliable than HLDTL-EV. Compared with the RH latch, the proposed latch has a higher power consumption and a larger transmission delay, but the RH latch cannot provide DNU self-recoverability. Therefore, the proposed latch is more reliable than the RH. Compared with the DNCS latch, the proposed latch has a lower power consumption, a smaller transmission delay, and a smaller area. However, the DNCS latch cannot provide DNU self-recoverability. Therefore, the proposed latch is more reliable than the DNCS.

Moreover, compared with the bottom three SNU and DNU resilient latches in Table II, the proposed latch is also SNU and DNU resilient. However, the proposed latch has the smallest area, delay and ADPP, which demonstrates the cost effectiveness of the proposed latch.

According to Table II, it can be calculated that, compared with the NTHLTCH latch, the proposed latch can save 90.10% of ADPP, 85.50% of transmission delay, 20.67% of area, and 15.00% of power consumption. Compared with the DNUSH latch, the proposed latch can save 9.09% of ADPP, 20.25% of transmission delay, and 20.67% of area. Compared with the HRCE latch, the proposed latch can save 41.18% of ADPP, 21.81% of transmission delay, 217.91% of area, and 11.11% of power consumption. Therefore, the proposed latch can save 76.74% of ADPP, 68.20% of transmission delay, 19.74% of area, and 0.2% of power consumption on average, compared to the bottom three latches of the same type. In summary, the comprehensive overhead of the proposed latch design is lower when compared to the DNU resilient latches, which validates the cost-effectiveness of our

TABLE II
Comparisons Among Radiation Hardened Latch Designs

Latch Name	**10^{-4}×Area (nm^2)**	**Delay (ps)**	**Power (μW)**	**10^{-2} × ADPP**	**SNU Tolerant**	**SNU Recoverable**	**DNU Tolerant**	**DNU Recoverable**
HRLC [11]	3.86	43.93	0.75	1.27	Yes	Yes	No	No
LCHR [12]	4.75	70.38	1.06	3.54	Yes	No	No	No
HLDTL-EV [13]	6.53	1.63	0.77	0.08	Yes	Yes	Yes	No
DIRT [14]	5.35	6.73	1.12	0.40	Yes	Yes	Yes	No
RH [15]	5.45	1.61	0.83	0.07	Yes	Yes	Yes	No
DNCS [16]	8.60	65.41	2.35	13.21	Yes	Yes	Yes	No
NTHLTCH [17]	8.61	22.00	1.60	3.03	Yes	Yes	Yes	Yes
DNUSH [18]	8.61	4.00	0.96	0.33	Yes	Yes	Yes	Yes
HRCE [19]	8.32	4.08	1.53	0.51	Yes	Yes	Yes	Yes
Proposed	6.83	3.19	1.36	0.30	Yes	Yes	Yes	Yes

proposed latch design.

5 Conclusions

Due to charge sharing, DNU occurrence probability is increasing so that designs of DNU resilient latches have become essential to provide circuit reliability in nanometer technologies. In order to mitigate the impact of SNUs and DNUs on circuit reliability, in this paper, a novel completely DNU-recoverable latch has been proposed. The proposed latch has been implemented in an advanced 22 nm CMOS technology with a high-speed CLK-to-Q path. Simulation results have shown that, compared with the state-of-the-art DNU resilient latches of the same type, the proposed latch has the smallest delay, area, and comprehensive ADPP.

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