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Abstract: This brief presents a continuously regulated current mirror topology capable of providing a wide range of currents with high-precision and speed control features. The circuit combines a non-linear current-mode feedback solution for fast and energy-efficient operation with an input-referred regulated-cascode configuration for precise current mirroring. The proposed implementation has an output current ranging from 100 µA to 2 mA, exhibits a fast response time of ≈100 ns for the full range steps, while ensuring a high power efficiency (>90%) and low current copy errors (<0.5%).

Keywords: CMOS analog design; current mirror; current conveyor; non-linear feedback; high-current drive

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1. Introduction

Processing, amplifying or conveying current signals typically requires both static and dynamic current mirrors. Several performances are shared by both types, but it is clear that dynamic operation brings many more difficulties. Optimizing static and dynamic performances at once leads to conflicting decisions.

Several studies have demonstrated that the relation between static and dynamic performances is bounded by technological constants [1,2]. This specificity is referred to as the speed–power–accuracy trade-off. To quantify the role played by the technology in the design of a dynamic current mirror, the authors in [3] propose a figure-of-merits (1). It combines the bandwidth, the power consumption, and the relative accuracy of the current mirror.

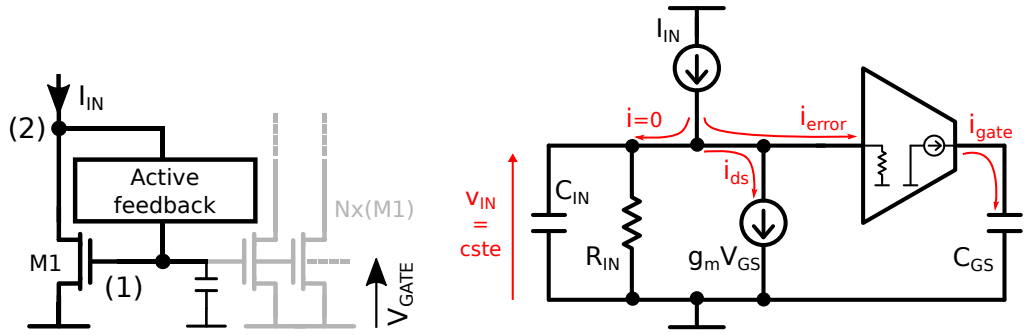
$$\frac{Power}{Bandwidth \times Accuracy^2} \propto C_{OX} A_{VTH}^2 V_{DD} \left(\frac{g_m}{I_{IN}} \right) \quad (1)$$

where C_{OX} is the gate oxide capacitance, A_{VTH} is the process-dependent matching parameter related to the MOS threshold voltage V_{TH}, g_m is the transconductance factor of mirroring devices, and I_{IN} is the input current. The above relation is an illustration of the fact that the global speed–power–accuracy performance does not depend on the size and bias of its devices. In other words, maximizing one of these three performances necessarily implies a cutback to the other. For a certain range of application, for instance whenever high-drive, high-speed or high-accuracy capabilities are required, the limit set by the technology makes it impossible to achieve the target performances.

More advanced current-mirror structures have a large variety, and the literature proposes numerous effective alternative topologies to improve the performances of classical current mirrors [4]. An observation would be that a limited number of published topologies precisely address the issues related to the speed–power–accuracy trade-off, despite the fact

that this trade-off has been frequently studied and is unavoidably encountered in dynamic CMOS current-mirror design.

Using an analysis similar to [3], it can be proven that active-input current-mirror topologies (i.e., feedback between input node and gate voltage in Figure 1a) can improve the speed–power ratio with minimal impact on the overall accuracy. Published in [5] in an early version and lately deployed in various applications [6,7], such structures can overcome under certain conditions the technological limit as long as the power consumption of the feedback circuit can be kept moderately low compared to the current-mirror bias itself.



(**a**) (**b**)

Figure 1. (**a**) General active-input principle. (**b**) Equivalent current-mode version.

In a previous study [8], we have proven that the replacement of the voltage-mode feedback that exists in a standard active-input current mirror by a current-mode circuit (Figure 1b) significantly enlarges the stability domain and increases the maximum speed reachable while offering a supplementary degree of freedom to tune the system response. Unlike transconductance or voltage amplifiers, current-mode circuits are components with low-input impedance capable of absorbing current with minimal variation in their input voltage. It improves the current-mirror input compliance and pushes the input pole towards higher frequencies for a wider stability domain. In Figure 1b, the terms C_{IN} and R_{IN} denote the equivalent input capacitance and resistance, respectively; while these parameters are influenced by transistor characteristics, they are also influenced by the feedback circuit itself and any parasitic elements present at these nodes. The designation "i=0" signifies that due to the extremely low input impedance of the current-mode feedback circuit, there is minimal change in the input voltage V_{IN} (i.e., "cste"). Consequently, no voltage variation across the equivalent input impedance (C_{IN} // R_{IN}) results in a negligible current flow through it.

It has been demonstrated in [8] that by forcing the current-mode feedback to have a non-linear behavior, static specifications can be unbidden from dynamic behavior for a much more power-efficient operation. For instance, thanks to the use of the proposed non-linear current-mode feedback, the speed of a standard diode-connected current mirror has been multiplied by 12.5, while the static power consumed has only increased by a factor 1.4, all with almost no impact on the initial current-copy accuracy or the system stability.

To go further, in this paper, we propose a continuously regulated topology which offers, by means of a second control loop, larger output impedance and better accuracy over wider current ranges, while it still preserves all the benefits of the original non-linear current-mode feedback. Simulation results and a state-of-the art comparison support the use of this topology as a competitive elementary current source for the design of high-performances circuits, capable of providing a wide range of currents (from several dozen µA to several mA) with high-precision along with a high speed/power ratio.

2. Improved Current Mirror with Non-Linear CCII-Based Feedback

2.1. Principles of Operation

Illustrated in Figure 2, the proposed current-mirror topology relies on a gate voltage regulation using non-linear current conveyors (NL-CCII), in combination with an input-

referred output-regulated cascode structure (IRRC), with a reference voltage terminal connected to the input node. This way, it forces the V_{DS} equality of the mirroring devices, boosts the output impedance by the operational amplifier (OPAMP) gain and decreases the intrinsic input branch impedance compared to a classic or high-swing cascode structure which improve the input dynamic range. The originality of this improved topology is the two feedback loops operating simultaneously, regulating both the gate voltage for speed improvement and drain voltages for a precise current copy.

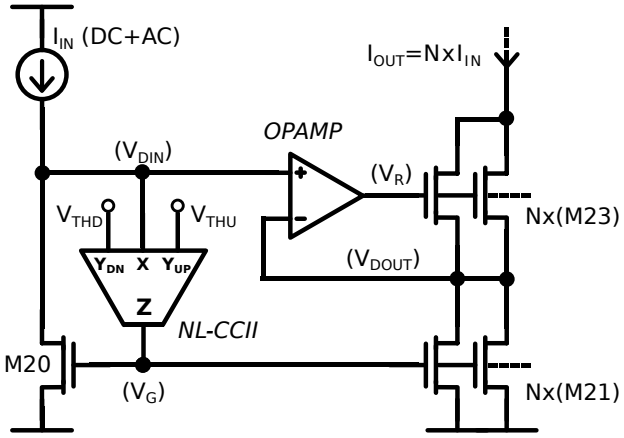


Figure 2. Proposed input-referred regulated cascode current mirror (IRRC) with non-linear CCII-based feedback.

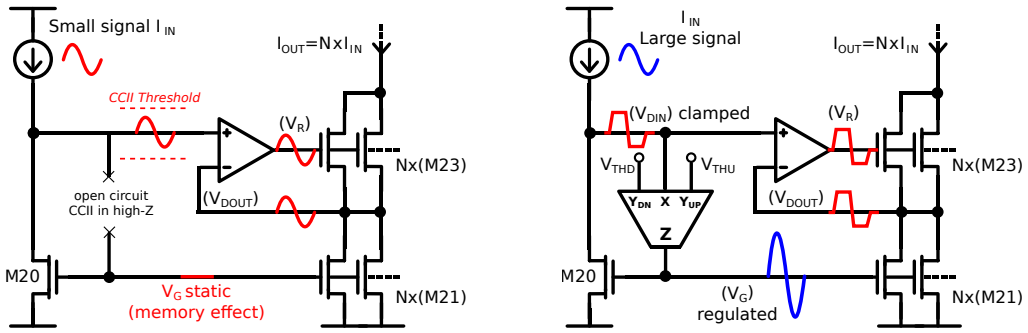
The accuracy of the current mirror is ensured conjointly by (i) large areas for the mirroring devices to minimize mismatch errors, (ii) drain regulation to reduce systematic errors due to asymmetrical v_{ds} modulation in the mirroring pair, (iii) very high output impedance offered by the output regulated cascode configuration, and (iv) an impedance switching mechanism in the CCII that avoids the speed control loop to introduce static error on the output current.

The low power consumption is achieved thanks to (i) the use of low-power topologies for the OPAMP, (ii) the channel length of cascode devices sized close to the minimal dimension which reduces the capacitive load that the OPAMP has to drive, reducing consequently the bias current it requires, (iii) a large current gain or copy ratio for the current mirror to minimize current losses, and (iv) an unbiased non-linear CCII structure that consumes zero power in a steady state. For more details, see Section 2.3.

The dynamic behavior depends on the amplitude of the currents involved and differentiates in two cases: (i) For a small input error current (I_ϵ), only the OPAMP is active (Figure 3a). The induced variation in the input voltage occurs within the range fixed by the two CCII thresholds. Equality between the input current and output current is achieved by modulation of the drain voltage of $M21$. The CCII stays in a high-impedance state, and the gate voltage is constant. The speed is mainly determined by the pole in the OPAMP output. (ii) For a large input current, the input voltage will reach one of the threshold values. The CCII is activated (Figure 2), and its low input impedance forces the input voltage to be clamped close to the threshold. Gate regulation is activated, and the output current follows the input variations according to gate voltage changes. The OPAMP is still active but in this case, the mirror speed is mainly dictated by the speed of the CCII-based control loop. Figure 3 summarizes both the small-signal and large-signal dynamic operation.

This improved structure also offers the possibility for the mirroring devices to operate in the triode region for a very high input-current range. According to the MOS current law in this operating region, we note that with the control of both drain and gate voltages, we are still capable of ensuring an accurate current copy. Highest values for the input current are principally determined by the residual DC offset and output common mode ranges ($OCMR$) of the OPAMP. Technically, with the NL-CCII structure and with mirroring

devices operating in the triode region at a high current level, the gate voltage can go up to values close to the power supply. However, with the input current increasing and the mirroring devices going deeper in the triode region, we can observe a drastic reduction in their output impedance. For drain current modulation due to loads, this output impedance reduction is compensated by the high gain of the output-regulated cascode technique as long as the cascoded devices stay saturated.

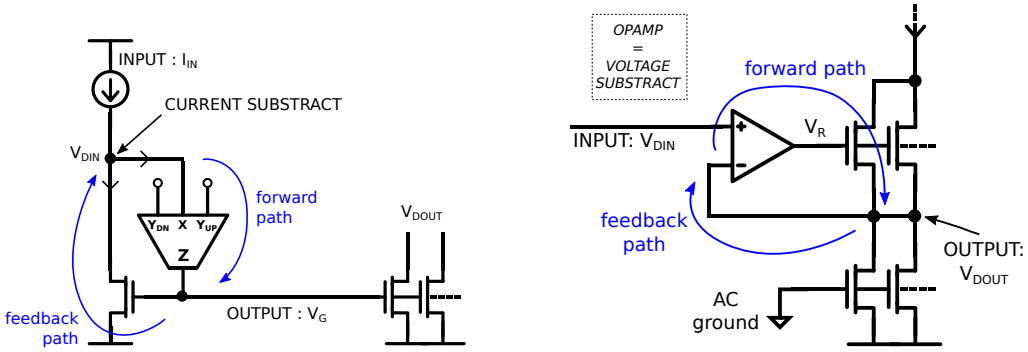


(**a**) (**b**)

Figure 3. Schematized operation of the improved structure. (**a**) Small signal operation. (**b**) Large signal operation.

2.2. System Model

The dynamic behaviour is determined by two feedback loops as depicted in Figure 4. Because they affect weakly dependent quantities and address two different characteristics of the current mirror, they can be treated separately. For the gate-voltage regulation based on such a non-linear current-mode feedback, a theoretical analysis of the dynamic behavior has been proposed in a previous author's publication [8]. The general behavior of classic wide-swing or regulated cascode current mirrors, among others, has been covered in [9]. However, for the sake of clarity, we recall here the main elements.



(**a**) (**b**)

Figure 4. Concurrent closed-loop systems considered. (**a**) For V_{GS} control. (**b**) For V_{DS} control.

The first feedback loop, based on the proposed non-linear CCII is dedicated to the speed control of the current mirror (Figure 4a). We are interested in the dynamic performances during a transient phase; the non-linear CCII is expected to be predominantly active, and the system dynamic will be treated without considering the high input impedance state. The block diagram in Figure 5 is derived from a small signal representation of the system shown in Figure 2. I_ϵ corresponds to the difference between the reference current I_{IN} and the current I_{MOS} absorbed by the transistor at a given moment. A certain amount of I_ϵ is driven by the CCII, the rest charges/discharges the parasitic capacitance on the input node under the voltage V_D developed across the overall input conductance $g_{IN}(V_D)$. Parameters β, g_Z and $g_X(V_D)$ are, respectively, the gain, the output conductance and the input conductance of the CCII. Here, the CCII input conductance depends on the input

voltage. $\tau_X(V_D)$, τ_Z and τ_{CC} represent, respectively, the time constant on the input drain, the time constant on the current mirror gates and the intrinsic time constant of the CCII ($\tau = g_m/C$). The current I_Z represents the current flowing through the CCII output node Z, and the voltage V_G is the voltage across the gate of the current mirror formed by transistors M20 and M21.

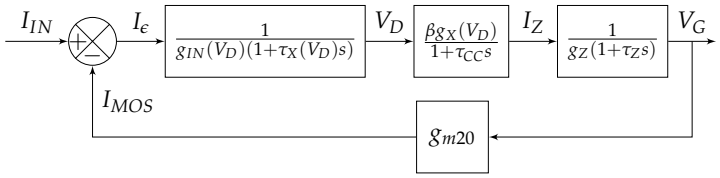


Figure 5. Block diagram modeling the CCII-based feedback solution.

The block with input I_Z and output V_G in Figure 5 represents the process where the current from the CCII's output node Z is converted into a voltage across the gate capacitance of transistors M20 and M21. As a simplified approximation, the time constant τ_Z can be considered as g_Z divided by the parallel combination of C_{GS20} and C_{GS21}, which forms the basis of the near-perfect integrator function. Assuming that the input time constant is negligible compared to the time constant on the gates of the current mirror M20–M21, in short $\tau_X << \tau_Z$, an approximated expression for the closed-loop transfer function is derived in (2).

$$H_{CL} = \frac{\beta}{g_Z + \beta g_{m20}} \frac{1}{1 + \frac{g_Z \tau_Z \tau_{CC}}{g_Z + \beta g_{m20}} s + \frac{g_Z(\tau_Z \tau_{CC})}{g_Z + \beta g_{m20}} s^2} \tag{2}$$

with the natural pulsation

$$\omega_n = \sqrt{\frac{g_Z + \beta g_{m20}}{g_Z \tau_Z \tau_{CC}}} \approx \sqrt{\beta \omega_{CC} \omega_{CM}} \tag{3}$$

Characteristics of the step response can be estimated using classical relations between the frequency domain and time domain behaviors. For instance, for an under-damped second-order system ($m < 0.7$) in the form of (2), overshoot O_V and response time at $n\%$ ($t_{rn\%}$) are approximated by the following expression:

$$t_{rn\%} = \frac{1}{m\omega_n} \ln\left(\frac{100}{n}\right) \qquad O_{V\%} = 100e^{\frac{-\pi m}{\sqrt{1-m^2}}} \tag{4}$$

The second feedback loop is made for high accuracy and high output impedance. It can bee seen as a low-output-impedance voltage amplifier, with unity gain feedback, loaded by a resistance (r_{DS} of M21). Here, we consider that the dominant capacitance is the gate capacitance of M23, and thus, the dominant pole is on the OPAMP output. Drain-to-source capacitance of M21 and input capacitance of the OPAMP are neglected. The amplifier DC offset is included as a voltage source in series with the non-inverting OPAMP input. The block diagram used for the analysis is shown in Figure 6. The parameter A_0 is the open-loop gain of the OPAMP, and the parameter GBW is its gain-bandwidth product. The equivalent conductance g_{DSeq} is defined as $g_{DSeq} = g_{DS21} // g_{DS23}$.

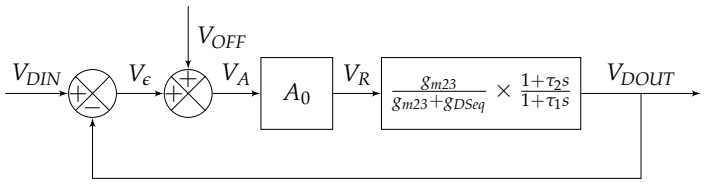


Figure 6. Block diagram modeling the output drain voltage control loop.

The voltage transfer function V_{DOUT}/V_{DIN} for drain regulation of the mirroring devices is given in (5). We observe that the speed of this loop is dominated by the intrinsic speed of the cascode device M23, which support the decision to size cascode devices with minimal channel length for a small gate capacitance and a high transconductance gain.

$$\frac{V_{DOUT}}{V_{DIN}} = G_{CL}\frac{1+\tau_2 s}{1+\tau_1 s} = \frac{A_0}{1+\frac{A_0}{2\pi GBW}s} \times \frac{1+\tau_2 s}{1+\tau_1 s} \tag{5}$$

$$\tau_2 = \frac{C_{GS23}}{g_{m23}} \qquad \tau_1 = \frac{C_{GS23}}{g_{m23}+g_{DSeq}} \tag{6}$$

The expression of the total output impedance seen by the load is displayed in (7). The higher the OPAMP open-loop gain A_0, the higher the output impedance, and the closer the voltage transfer gain is to the unity gain.

$$r_{OUTCM} = r_{DS21} + r_{DS23} + A_0 \times g_{m23} \times r_{DS21} \times r_{DS23} \tag{7}$$

However, the frequency behavior affects in the same proportion the input voltage V_{DIN} and the OPAMP offset voltage V_{OFF}. Hence, the totality of static voltage errors in the OPAMP is reported to the drain voltage of M23 and generates an output current error $I_{OFF} = g_{DS21} \times V_{OFF}$. However, with an offset in the order of 10 mV and an output impedance value for the mirror device of about 1 MΩ, this error current is found to be in the order of the dozen of nA. In the triode region, the output impedance can go down to several kΩ, significantly increasing the error current, but it occurs at large output currents. The relative difference has to be examined to see if the error due to the OPAMP offset starts to dominate the overall error.

2.3. Design Considerations for the NL-CCII and the OPAMP

A schematic of the NL-CCII is presented in Figure 7. This implementation uses self-biased cascoded devices (M3B and M4B) to improve gain linearity and save voltage headroom for a wider current dynamic. The output stage is composed of configurable output current mirrors for a digital control (B0-B7) of the NL-CCII current gain values. Nodes B0–B7 are digital nodes controlled externally, typically by a digital core that will manage the current source. These control bits allow for the tuning of the NL-CCII gain and thus the resulting speed of the system. They can be used to fine-tune the system response or to save power by reducing the NL-CCII gain in applications where fast current waves are not always demanded. Sizes of transistors composing the NL-CCII are given in Table 1.

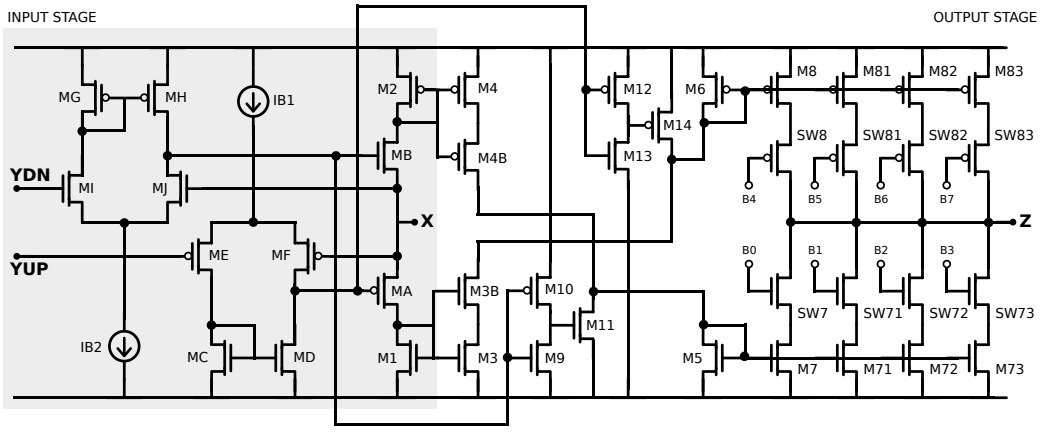


Figure 7. Implementation of the non-linear CCII with configurable current gain for both sink and source output current (2 × 4 bits).

The OPAMP used for the V_{DS} control loop is identical to the OPAMP controlling the transistor MB in the CCII input stage. Differential pairs are biased in moderate inversion under a tail current of 5 µA (IB1 and IB2) and are realized with low V_{TH} devices. To restrict the static consumption to a minimum, while ensuring sufficient output compliance, we opted for a single-stage amplifier with no cascode configuration. More advanced OPAMP topology can replace the single-stage OPAMP in both drain and gate feedback but with a certain increase in the power budget, which is not always justifiable. Techniques that reduce the OPAMP DC offset will also reduce the copy error at a high current level. Techniques that increase its gain-bandwidth product will lead to a higher output impedance when used for drain regulation and sharper transition between the two NL-CCII states when used for gate regulation.

Table 1. Transistors sizing for the NL-CCII.

	W/L µm		**W/L µm**		**W/L µm**		**W/L µm**
M1	3.5/0.25	M2	5/0.25	M5	0.45/0.25	M6	1.5/0.25
M3	3.5/0.25	M4	5/0.25	M7	$2 \times 0.45/0.25$	M8	$2 \times 1.5/0.25$
M3B	12/0.25	M4B	20/0.18	M71	$4 \times 0.45/0.25$	M81	$4 \times 1.5/0.25$
MA	7/0.18	MB	2/0.18	M72	$8 \times 0.45/0.25$	M82	$8 \times 1.5/0.25$
MC	1/1.5	MG	0.5/1.5	M73	$12 \times 0.45/0.25$	M83	$12 \times 1.5/0.25$
MD	1/1.5	MH	0.5/1.5	M9	0.5/4.5	M12	0.5/4.5
ME	2.5/0.5	MI	2/0.5	M10	2.5/4.5	M13	2.5/4.5
MF	2.5/0.5	MJ	2/0.5	M11	0.5/4.5	M14	2.5/4.5

Transistors ME, MF, MI and MJ are low-threshold devices.

The CCII input impedance value depends on the operating regions of MA, MB, M1 and M2, which relate to the input voltage V_D through the comparators. In the high-impedance state, MA and MB are OFF, and the CCII input impedance can be approximated by

$$\begin{aligned} &r_{Xhz} \approx r_{OFFMA} // r_{OFFMB} \\ &\text{for } V_{YDN} < V_D < V_{YUP} \end{aligned} \tag{8}$$

In the low-impedance state, either MA or MB is ON, and the input impedance expresses as

$$\begin{aligned} r_{Xlz} &\approx r_{ONMA} + 1/g_{mM1} \quad \text{for } V_D > V_{YUP} \\ r_{Xlz} &\approx r_{ONMB} + 1/g_{mM2} \quad \text{for } V_D < V_{YDN} \end{aligned} \tag{9}$$

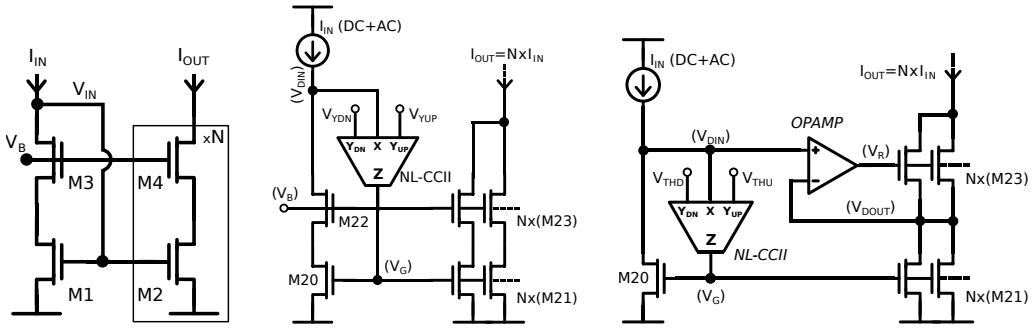
To achieve a better stability margin and better speed, we want to minimize the r_X value for the low impedance state. This is carried out using a large channel width for the switches MA and MB and a large W/L ratio for M1 and M2. Transistors M1 and M2 can be sized to be in weak inversion for low levels of CCII input current, maximizing their transconductance and consequently the input current dynamic. Because there is no static biasing for these current mirrors, the CCII might show significant gain distortion and cut-off frequency variation across the full current dynamic, which can lead to detuned feedback. To limit these effects in the proposed implementation, high-impedance self-biased cascode current mirrors have been used in place of the simple current mirrors M1–M3 and M2–M4. Eventually, to enforce the switching mechanism, the output node is also quickly turned into high impedance using switches controlled by the same signal used for the input. Ensuring that the current stops flowing out of the CCII at the same time, the input stage goes from the low to high impedance state. The duration of the output stage to switch between the high and low impedance state mainly depends on the delay of the inverters M9–M10 and M12–M13 and on current capabilities of the shorting devices M11 and M14.

There are few constraints on the voltage copy error from nodes Y to node X and on the current copy errors from node X to node Z. The voltage copy ensures that voltage at

node X is always within the two threshold values; no precision is required here. As for the current copy, because we are dealing with a closed-loop system with integral action, CCII current-copy errors are compensated by the control loop. Therefore, the design constraint of the CCII internal current mirrors can be relaxed.

3. Simulation Results and Comparison with Reference Structures

To validate the previous assessments, here, we present simulation results of an implementation of the improved input-referred output-regulated cascode current mirror with non-linear CCII-based feedback (Figure 8c). For comparison purposes, we have also implemented the equivalent high-swing cascode current mirrors with both diode-connection (Figure 8a) and non-linear CCII-based feedback (Figure 8b).



(**a**) (**b**) (**c**)

Figure 8. The three evaluated current mirror structures: (**a**) DCO WSCASC CM: diode-connected wide-swing cascode, (**b**) NL-CCII WSCASC CM: non-linear CCII-based wide-swing cascode, (**c**) NL-CCII IRRC CM: non-linear CCII-based input-referred regulated cascode.

The circuits have been designed using the TSMC 0.18 µm standard CMOS process and operate at 1.8 V. In the whole following characterization, the mirroring devices of the three current mirrors presented in Figure 8 are sized with $W_{CM}/L_{CM} = 21.5\,\mu m/18\,\mu m$ and cascode devices with $W_{CM}/L_{CM} = 21.5\,\mu m/0.25\,\mu m$, in order to operate on the edge of the strong inversion at the minimum input current I_{IN} =5 µA. The mirror current gain (or copy ratio) is fixed at $N = 20$, leading to a minimum output current of 100 µA. CCII thresholds are here fixed at 0.6 V and 0.8 V in the NL-CCII IRRC CM for compatibility with test resources that we used but did not address in this publication.

Simulation benches are the following: (i) A measure of the influence of the channel length on the accuracy and bandwidth for the diode-connected current mirror. We look at the speed versus the variability for a small dimension as well as for the maximum dimension authorized by the process rules. (ii) A measure of static performances such as input/output compliances, systematic current transfer errors (no mismatch) and output impedances. (iii) An illustration of the typical dynamic behavior with measurement of the step response and the harmonic response for a full-range input signal. (iv) Statistical measurements to evaluate both static and dynamic performance dispersions.

3.1. CM Sizing and Speed–Accuracy Trade-Off

In this first test, we compare the accuracy and bandwidth of a diode-connected high-swing cascode current mirror (Figure 8a) for a channel length (L_{CM}) ranging from 4 µm to 18 µm (the maximum length allowed by the DRC rules). The operating point is fixed at $I_{IN} = 30\,\mu A$ (current source), $V_{out} = V_{DD}/2 = 0.9\,V$ (voltage source) and $V_B = 1.3\,V$ (voltage source). The (W/L) ratio of mirroring devices is kept constant and chosen such that $V_{IN} \simeq 0.9\,V$ for the considered operating point ($W_{CM}/L_{CM} = 1.2$). The channel width of cascode devices W_{CASC} are kept equal to the width of mirroring devices W_{CM}. Lengths L_{CASC} are taken at the fixed value of 0.25 µm. Figure 9 shows the DC output error distribution for different channel lengths, taking into account systematic errors, process

variations and mismatch errors. Figure 10 is an AC measurement of the current-mirror bandwidth as a function of the channel length L_{CM}.

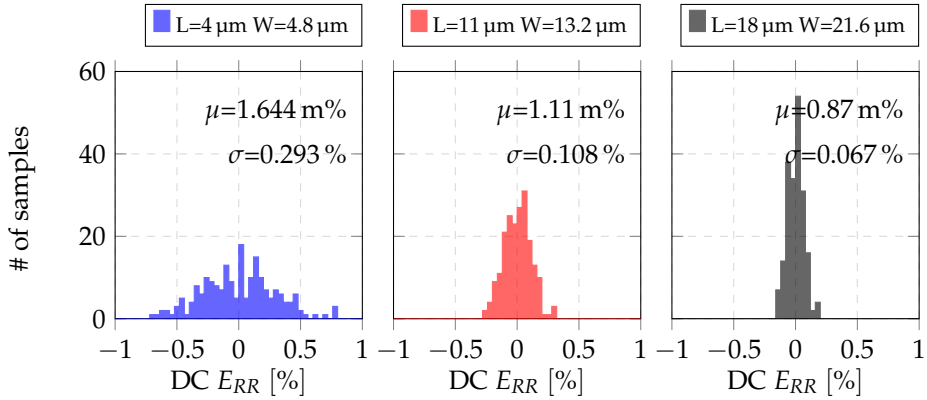


Figure 9. Static output error of the diode-connected wide-swing cascode current mirror (DCO WSCASC CM) at various lengths.

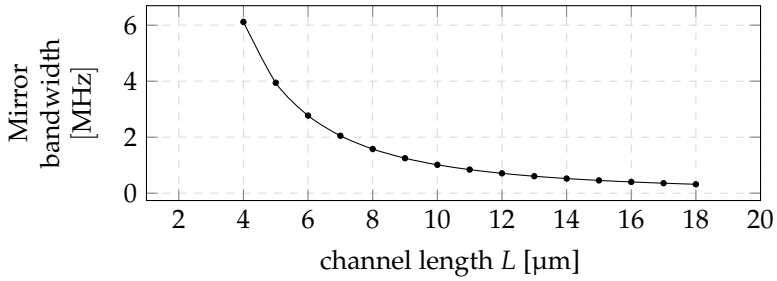


Figure 10. Simulated bandwidth for the diode-connected wide-swing cascode current mirror (DCO WSCASC CM) at various lengths of the mirroring devices. As expected, the bandwidth is decreasing proportionally to $1/L^2$.

As expected, the output error and bandwidth both decrease when the channel length increases. This means that by taking the mirror devices with the maximum length (18 µA), we have spent all of the speed–accuracy budget to minimize the output error [3]. This will be our choice for the next tests. The NL-CCII of the gate-voltage control loop is in charge of speeding up the mirror with minimal impact on error and power.

3.2. Typical Static and Dynamic Behaviour

By looking at static behaviors given in Figure 11, we compare input/output compliances and output impedances. We observe that while all the circuits require approximately the same minimum output voltage for a proper operation in the saturated region ($V_{OUT} > 0.7$ V for I_{OUT} up to 2 mA), the minimum input requirement is drastically different between the diode-connected configuration and the one with NL-CCII-based feedback. Thanks to the input switching mechanism of the CCII, the input voltage is constrained, and the minimum admissible value is actually equal to the upper threshold value (0.8 V). For the considered device sizes, the diode-connected high-swing cascode mirror shows a lower input requirement as long as the input current is under 20 µA. However, the minimum admissible value increases with the input current at a rate of $\approx \sqrt{I_{IN}}$, which significantly reduces the room for the input source to operate at a high current level. In parallel, we observe one of the main advantages of the regulated cascode topology by looking at the output impedance, which shows an increase ranging from $\times 3$ to $\times 50$ when compared to the two other equivalent current mirrors.

We now consider the dynamic behavior of each of the three circuits illustrated by a transient simulation with a full-range signal applied to the input. For time domain

evaluation, the input stimuli is a 3 µs current pulse from 5 µA to 100 µA which leads to an output current pulse of 100 µA to 2 mA. For the distortion performance, we looked at the output current spectrum when the input stimuli is a pure sine wave of 50 µA ± 20 µA at 100 kHz. Observed response times at 0.4 % (Table 2) demonstrate the efficiency of the NL-CCII-based feedback to speed up the current mirror at a minimal power cost.

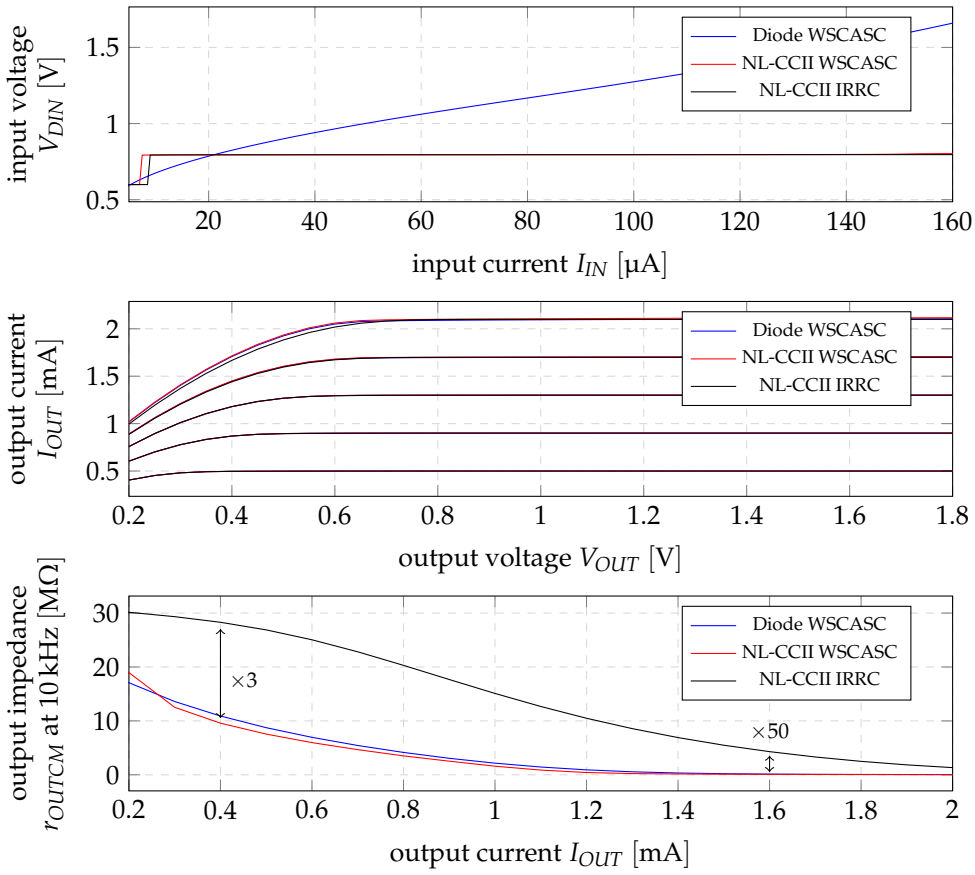


Figure 11. Static characteristics of input voltage versus input current, output I/V curve and output impedance versus output current. $V_B = 1.3$ V. CCII thresholds = 0.6 V and 0.8 V.

Regarding the distortion simulations (Table 3), the NL-CCII IRRC shows better THD (44 dB) and SFDR (46 dB) for the step considered thanks to the drain regulation and the high output impedance offered by the topology. For the same step, the DCO WSCASC mirror, taken as a reference, exhibits a THD of −28 dB and an SFDR of 30 dB. However, when the step amplitude decreases, the effects of noise and distortion generated by the CCII switching mechanism become more important and degrade the THD. The diode-connected configuration generally shows a greater linear response for small signal inputs. Figure 12 shows the results of the long-time transient simulation for which we have calculated the spectrum and measured the THD and SFDR.

Table 2. Response time ($tr_{0.4\%}$) and static power efficiency (PW_{EFF}) for a full range input signal.

	$tr_{0.4\%}$	PW_{EFF} at $I_{OUT} = 100$ µA	PW_{EFF} at $I_{OUT} = 2$ mA
DCO WSCASC CM	1.69 µs	95.2 %	95.2 %
NL-CCII WSCASC CM	244 ns	90.9 %	94.5 %
NL-CCII IRRC CM	71.4 ns	88.9 %	94.1 %

Table 3. THD and SFDR measurements for a sine wave of 50 µA ± 20 µA at 100 kHz.

	THD (dB)	SFDR (dB)
DCO WSCASC CM	−27.8	30.2
NL-CCII WSCASC CM	−35.4	37.24
NL-CCII IRRC CM	−43.7	46.32

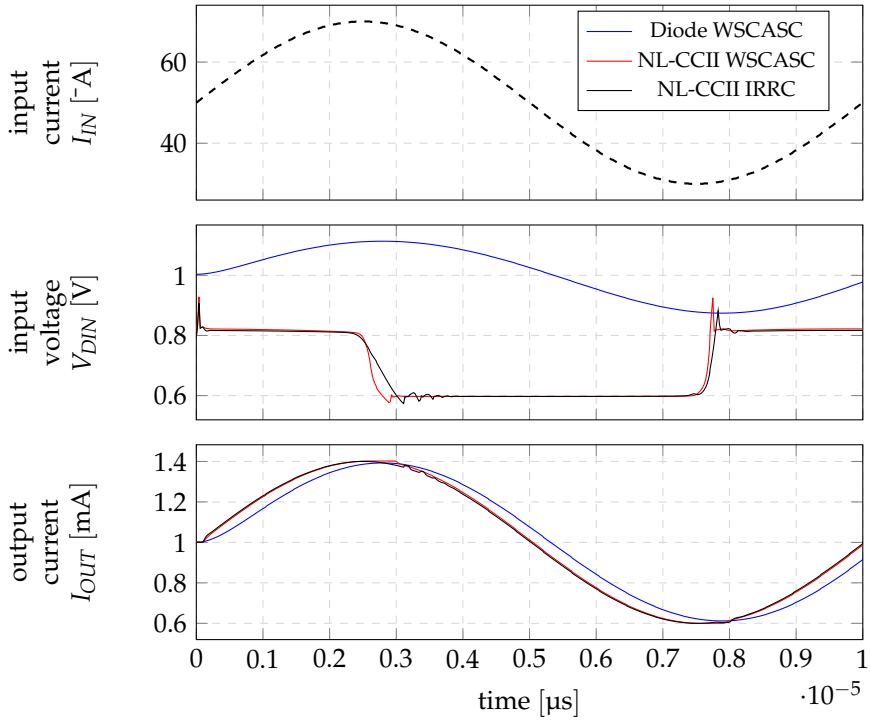


Figure 12. One period of a long time simulation with a harmonic signal. Input current wave has a DC component of 50 µA and a magnitude of 20 µA at 100 kHz.

3.3. Statistical Results and Speed-Power-Accuracy Metrics

Monte-Carlo simulations are performed for statistical evaluations of the overall copy error, the drain mismatch of mirroring devices (absolute difference between drain voltages) and the settling time. The three circuits are stimulated with several steps of various amplitudes, ranging from ±500 nA to ±55 µA while biased at different levels across the input current range, starting from 10 µA up to 110 µA. Stimuli cases are summarized in Table 4.

To evaluate the speed–power–accuracy metrics, the following definitions will be employed: The response time $t_{r0.4\%}$ will be assessed based on the transient response. The static output error E_{RR} is determined by summing the systematic and random errors as follows:

$$\text{DC copy error} = |\mu(E_{RR})| + |\sigma(E_{RR})| \tag{10}$$

Power efficiency is defined as the ratio of the power delivered to the load ($I_{OUT} \times V_{DD}$) to the total power dissipated, including input reference currents and dedicated bias for the feedback circuits:

$$\text{power efficiency} = \frac{P_{LOAD}}{P_{TOT}} = \frac{I_{OUT}}{I_{OUT} + I_{IN} + I_{BIAS}} \tag{11}$$

The bandwidth is estimated as

$$\text{estim. bandwidth} = \frac{1}{2\pi \times \tau} \approx \frac{1}{2\pi \times \frac{t_{r0.4\%}}{5}} \tag{12}$$

Table 4. Stimuli summary.

#	Bias	Step	#	Bias	Step
1	10 µA	±0.5 µA	9	70 µA	±0.5 µA
2	10 µA	±2 µA	10	70 µA	±2 µA
3	30 µA	±0.5 µA	11	70 µA	±20 µA
4	30 µA	±2 µA	12	90 µA	±0.5 µA
5	30 µA	±20 µA	13	90 µA	±2 µA
6	50 µA	±0.5 µA	14	90 µA	±20 µA
7	50 µA	±2 µA	15	110 µA	±0.5 µA
8	50 µA	±20 µA	16	110 µA	±2 µA
			17	60 µA	±55 µA

The static output error and drain mismatch versus input current range characteristics are reported in Figure 13. The curve represents the average values, and error bars show the corresponding standard deviation ($\pm\sigma$). Figure 14 puts in relation the observed response time and its standard deviation with the static power efficiency for each of the 17 stimuli cases. As expected, the NL-CCII IRRC CM exhibits a drain-voltage difference (10–20 mV) slightly greater than the WSCASC configurations (5–10 mV), but looking at the copy error plot, we observe that the NL-CCII IRRC CM still offers the highest accuracy, and the error at 1σ is always lower than 0.2 % for the full input range. Regarding the mirror speeds (Figure 14), we observe larger relative standard deviations (error bars) for both topologies based on the current conveyor. This is explained by the device dimensions constituting the CCII. Transistors are all close to minimal dimensions to reduce the silicon area and achieve a high-speed feedback operation but at the price of large variability. The absolute amount of response time dispersion is a small percentage of the speed which has itself decreased from several µs to hundreds of ns, making this amount almost insignificant.

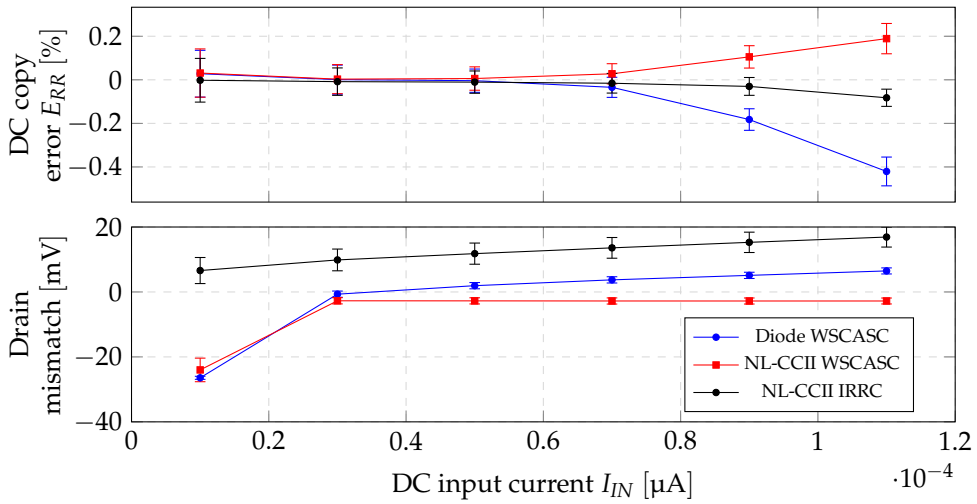


Figure 13. DC current copy error and drain mismatch of mirroring device.

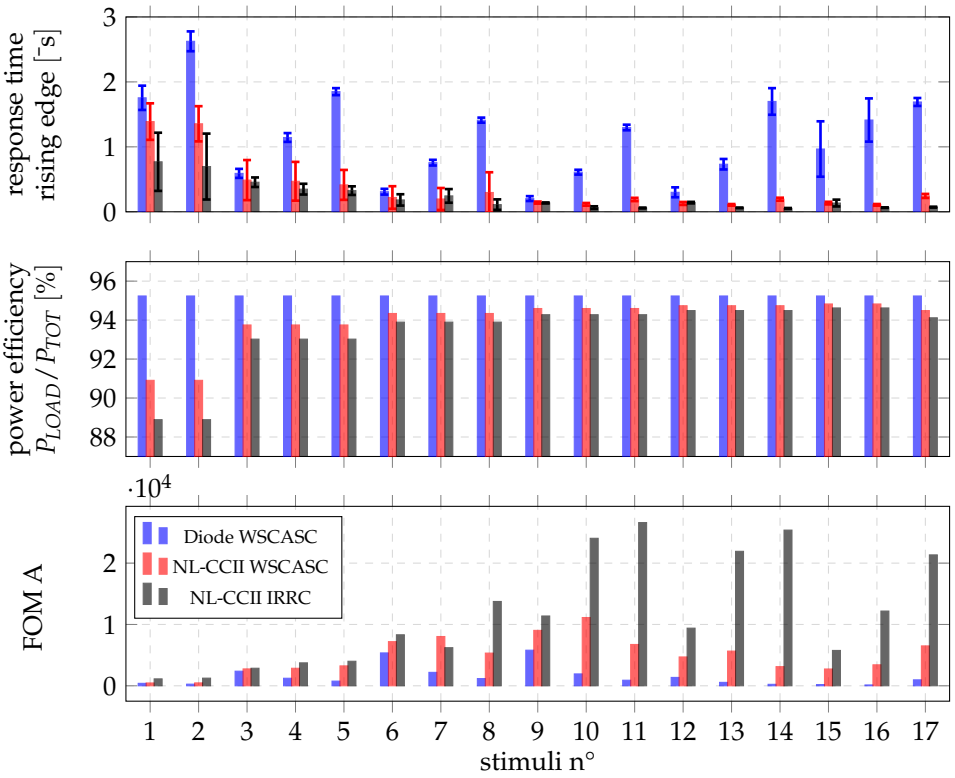


Figure 14. Response time at 0.4 % with error bars representing the standard deviation, power efficiency and evaluation of the FOM A, for each stimuli reported in Table 4.

4. Discussion and Conclusions

In order to quantify the improvements regarding the speed–power–accuracy trade-off, we propose the two generic metrics (FOM A and FOM B) given below.

$$FOM\ A = power\ eff/(resp.\ time \times dc\ error) \tag{13}$$

$$FOM\ B = power\ eff \times bandwidth/dc\ error \tag{14}$$

As shown in Figure 14, in comparison with the equivalent DCO WSCASC and NL-CCII WSCASC current mirrors, the proposed topology exhibits the best score on the FOM A for each simulated stimuli case.

To compare the NL-CCII IRRC CM with other topologies of the advanced current mirror available in the literature, we use the performances observed for the full-range stimuli case. The performance summary and scores for the FOMs are presented in Table 5. According to the scores achieved by the different circuits, the proposed NL-CCII IRRC CM is found to be one competitive structure to achieve a fast and precise response at minimal power while offering high dynamic and high drive capabilities.

Finally, this study demonstrates the advantages of our advanced current-mirror design approach which relies on the combination of a non-linear current mode feedback and drain-voltage regulation. This topology is particularly suitable for applications requiring simultaneously high-speed and high-drive capabilities (from µA to mA in hundreds of ns) but also the maximum current-copy accuracy allowed by the technology.

There is a certain number of topics, not specifically treated in this paper, that may be worth citing to open the discussion on the outcomes: (i) The proposed non-linear current conveyor architecture is one of the successful candidates to implement the current-mode non-linear feedback control, but other solutions can be thought. For instance, very low-voltage applications may require a much simpler implementation with a limited number of devices. On the other hand, for applications with a higher power budget, we might opt for modified versions of high-drive or high-speed current conveyors/amplifiers that reuse

the principle of the input impedance switching mechanism. (ii) To deploy this approach for current source architectures dealing with harmonic signals (sine waves, multi-tonal waves, ...), the design effort on the feedback circuit should focus more on the linearity optimization than the optimization of the static precision. Requirements over the CCII specifications would slightly differ. (iii) The input impedance switching mechanism of the CCII, and the way it is used, presents some similarities with the work carried out in the past on current memory cells. A comment would be that some answers to the points raised above may be found with a deeper investigation of this domain.

Table 5. Performance summary and comparison with previous published work.

Perf	This Work	[10]	[11]	[12]	[13]	[9]	[14]	[15]
Technology (µm)	0.18	0.18	0.18	0.5	0.18	0.18	0.25	0.18
Supply voltage (V)	1.8	1	1	1	0.9	1.8	1	1.5
Min output current (µA)	100	50	0.1	10	0	0	0	
Max output current (µA)	2000	1000	1000	100	60	280	300	
Output error (%)	0.06	2	0.16	0.4	0.3	0.8	5	2.4
Resp. time at 1% (µs)	0.07	0.04		0.07			0.02	
THD (%) FR = Full Range	0.65 @ 36% FR			0.8 @ 50% FR	0.8 @ 50% FR			1
Bandwidth (MHz)	11.15	168	82	140	80	132	398	
Power efficiency (%)	94.12	50	50	30		50	33	40
FOM A	22.7	0.63		1.07			0.33	
FOM B	17.5	4.2	25.6	10.5		8.25	2.63	3.08

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