Low-Resource Fully-Digital BPSK Demodulation Technique for Intra-Body Wireless Sensor Networks

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***Abstract*—In the context of intra-body communication, galvanic coupling has gained significant attention. This communication technique leverages conductivity of biological tissues to use them as a medium for modulated electrical signals. This paper introduces a novel fully-digital demodulation technique for use in galvanic coupling transmission with BPSK-modulated signals at low frequencies (below MHz). The technique relies on an original digital processing algorithm applied on samples collected by an analogue-to-digital converter. The algorithm employs a voting principle among several demodulated data candidates and implement an error detection scheme to offer high robustness and reliability. Moreover, it has been specifically designed to minimise the computational operations and resources required to enable a compact and energy-efficient implementation. Simulations and experiments demonstrate good performance, with a perfect transmission success rate of 100% for signals with a Signal-to-Noise Ratio (SNR) of $-3\,\mathrm{dB}$ or higher, and a success rate that remains higher than 97% for signals with an SNR down to $-7\,\mathrm{dB}$.**

***Index Terms*—Intra-body communication, galvanic coupling, BPSK, demodulation, digital processing algorithm.**

I. Introduction

The field of low-frequency (less than few MHz) and radio-frequency (hundreds of MHz and more) communication has become increasingly important, stimulated by the development of active medical implants and the need for specialised communication techniques for implanted sensor network applications [1]. Among promising low-frequency solutions, Galvanic Coupling (GC) communication has received significant attention [2]. This approach leverages conductivity of biological tissues [3] to use them as a medium for modulated electrical signals [4], transmitted and received through the body using electrodes as interface between electronics and tissues. GC stands as a formidable competitor to the conventional RF communication technique. It offers several distinct advantages such as enhanced security due to its confined transmission channel, elimination of the need for antennas, and power efficiency by avoiding power-intensive RF components.

Conventional signal demodulation relies on the use of dedicated analogue and mixed-signal components such as mixers, filters, PLL resulting in systems that are difficult to implant due to size and consumption constraints. On the other hand, software-defined radio (SDR) is a technology where the analogue components are replaced by an Analog-to-Digital Converter (ADC) and a general-purpose digital processor [5], which offers the advantage of enhanced flexibility and adaptability. Typically in SDR, it is the IF signal that is sampled by the ADC. However, in case of low-frequency modulated signals, conversion to the digital domain can be performed directly on the received signal.

This paper introduces a novel direct demodulation technique tailored for low-frequency Binary Phase-Shift Keying (BPSK) modulated signals, which relies on direct sampling of the modulated signal by an ADC associated with an original digital processing algorithm. The technique is meticulously designed to address the complexities of signal acquisition and demodulation while adhering to stringent size and power consumption requirements, thanks to a low-resource, low-complexity, all-digital processing algorithm.

The paper is organised as follows. The proposed solution is described in Section II, which details the communication format, signal acquisition and digital processing algorithm. Section III is dedicated to the validation of the technique through simulations. Hardware experimental results are then presented in Section IV. Finally, Section V concludes the paper.

II. Proposed Solution

A. Communication Format

In the field of intra-body communication, a consensus regarding the signal transmission frequency and the type of modulation to employ remains elusive. Published works have presented diverse modulation schemes, each with its own distinct characteristics. These include On-Off Keying (OOK) modulation [6], Direct Sequence Spread Spectrum Differential Phase Shift Keying (DSSS-DPSK) modulation [7], Frequency Shift Differential Transmission (FSDT) modulation [8], Pulse Position Modulation (PPM) [9], and Binary Phase Shift Keying (BPSK) modulation [10]. Each of these modulation types comes with its unique constraints, tailored to the specific requirements of the targeted applications, encompassing a

TABLE I
COMMUNICATION FRAME FORMAT

drive Preamble	ID	Frame counter	Data	Postamble
Bits: 1	**3**	**8**	**8, 16 or 24**	**4**

wide range of frequencies, spanning from a few hertz to several megahertz, resulting in a diverse range of data rates.

In our work, we have selected phase modulation due to its superior noise immunity when compared to other modulation techniques. More precisely, we have chosen BPSK modulation, defined with the following parameters:

- F_{c} is the carrier frequency (i.e. the signal transmission frequency),
- $\frac{1}{T_{\mathrm{bit}}} = \frac{F_{\mathrm{c}}}{N_{\mathrm{per}}}$ is the data rate, where T_{bit} is the duration of one bit and N_{per} the number of carrier periods per bit,
- N_{bytes} is the number of transmitted data bytes.

In the context of sensor network applications, the information to be transmitted must be formatted according to a communication protocol. The development of a communication protocol is beyond the scope of this paper. We therefore adopt a very simple protocol using the frame format illustrated in Table I, which comprises five fields:

- the first field is a one-bit preamble that will be used by the demodulation algorithm to resolve phase-induced ambiguity, this preamble being arbitrarily set to 1,
- the second field contains the identifier (ID) of the sensor that sent the data,
- the third field contains the number of frames that compose the message,
- the fourth field is the data payload that contains the actual message delivered by the sensor, with a maximum of 24 bits,
- the last field is a postamble that will be used by the demodulation algorithm to implement error detection, the postamble being set to an arbitrary fixed value (the choice of a 4-bit postamble has been done so that a frame is composed of an integer number of bytes).

This simple format permits to manage up to eight different sensors without specific constraint on the length of the messages delivered by each sensor, thanks to the possibility of multi-frame transmission. With a maximum frame length of 5 bytes, the maximum length for one message is achieved using 256 frames, each containing 24 message bits, i.e. a total of 6114 bits or 768 bytes.

B. Signal Acquisition

The proposed solution relies on the same concept as SDR, i.e. the BPSK-modulated signal is first digitised using an Analogue-to-Digital Converter (ADC) and the resulting signal is processed directly in the digital domain to implement demodulation. A cornerstone of the proposed technique is to use redundant sampling by setting the ADC sampling frequency

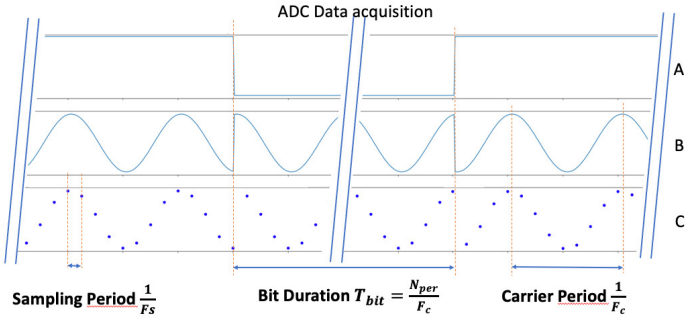

Fig. 1. Time-domain representation of signals. A) initial data to be transmitted, B) BPSK-modulated signal, C) received digitised signal.

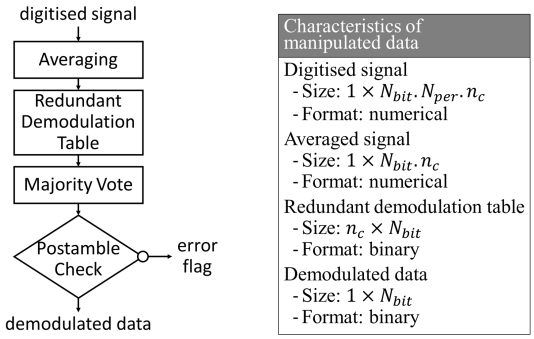

Fig. 2. Flowchart of digital processing algorithm and characteristics of manipulated data.

F_{s} to an exact multiple n_{c} of the carrier frequency F_{c}, with $n_{\mathrm{c}} \geq 2$ to respect Nyquist-Shannon theorem:

$$F_{\mathrm{s}} = n_{\mathrm{c}} \cdot F_c \quad \text{with} \quad n_{\mathrm{c}} \geq 2 \tag{1}$$

Fig. 1 gives the time-domain representation of the BPSK-modulated signal and the received digitised signal.

For N_{bytes} data bytes to be transmitted, the number of captured digital samples N_{s} is given by:

$$N_{\mathrm{s}} = 8N_{\mathrm{bytes}} \cdot N_{\mathrm{per}} \cdot n_{\mathrm{c}} = 8N_{\mathrm{bytes}} \cdot T_{\mathrm{bit}} \cdot F_{\mathrm{s}} \tag{2}$$

C. Digital Processing Algorithm

A dedicated digital processing algorithm has been developed to perform direct demodulation of the signal digitised by the ADC. The bloc diagram of this algorithm is depicted in Fig. 2. It comprises four main steps which are detailed hereafter.

1) Averaging: The signal captured by the ADC is a discrete-time sine-wave with phase inversion occurring only at changes in bit values. Therefore, no phase variation is expected over the N_{per} periods of each bit.

Moreover, because of the redundant sampling with $F_{\mathrm{s}} = n_{\mathrm{c}} \cdot F_{\mathrm{c}}$, only n_{c} unique samples are actually collected over the N_{per} periods of each bit, samples collected in the subsequent periods being only repetitions of samples collected in the first period.

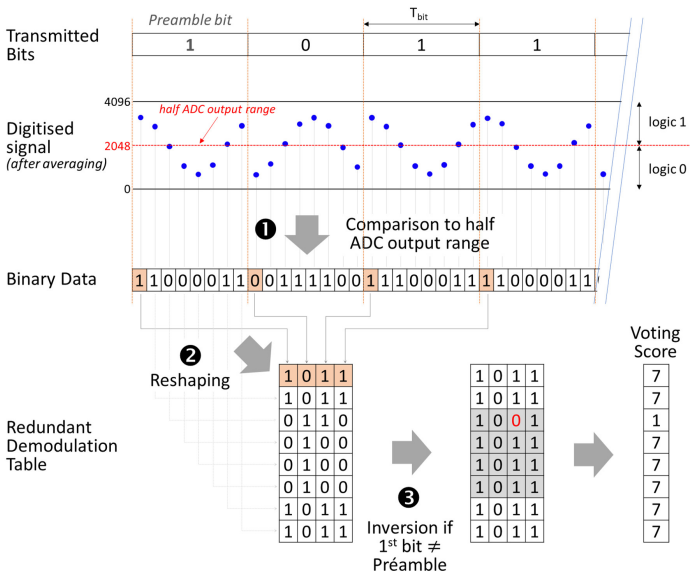

Fig. 3. Illustration of redundant demodulation table construction (n_c=8).

The idea is to take advantage of this repetition to reduce noise by computing, for each bit, the average value $\overline{s}[n]$ of redundant samples:

$$\overline{s}[n] = \frac{1}{N_{\text{per}}} \sum_{m=0}^{N_{\text{per}}-1} s[n - mn_c] \tag{3}$$

Where m is the index of the period among N_{per} period per bit and n is the index of the data sample. This process transforms the original captured signal that contains N_{per} carrier periods for each bit into a signal that contains only one equivalent carrier period for each bit, with n_c unique samples uniformly distributed over the equivalent period. Such a process is frequently used in digital instrumentation and can reduce noise by a factor $1/\sqrt{N_{\text{per}}}$.

2) Construction of Redundant Demodulation Table: The second step of the processing algorithm is to build a redundant demodulation table from the samples obtained after averaging. The principle is illustrated in Fig. 3, with a sampling frequency F_s equal to n_c=8 times the carrier frequency F_c. The digitised signal obtained after averaging is a signal with one period per bit and n_c samples per period, i.e. n_c samples per message bit.

Theoretically, direct demodulation could be performed using only a single sample of each message bit. However, this requires to have the knowledge of the received signal phase or to retrieve it. To avoid this, the idea is to perform the demodulation of each one of the n_c samples corresponding to one message bit. More precisely, the samples are first converted into binary data by comparing their values with half the ADC output range (1 if the value is higher than half the ADC output range, 0 otherwise). These binary data are then reorganised in a redundant demodulation table, where the i^{th} row contains the binary data interpreted from the i^{th} samples of each message bit.

Because samples are distributed over a complete period, they cover different phases of the received signal. Some rows of the table therefore contain the demodulated data directly, while others contain the 2's complement of the demodulated data. This ambiguity can be resolved by checking the preamble. Knowing that the preamble bit is set to 1, all rows of the demodulation table that start with a bit at 0 are simply inverted.

At the end of this process, in case of a perfect received signal, all rows of the demodulation table contain the same data corresponding to the message bits. Obviously in a practical situation, the received signal will be affected by imperfections that might entail errors. In particular, errors are susceptible to occur for the samples that fall in the vicinity of half the ADC output range. This is the case, for example, for the 3^{rd} and 7^{th} samples of each period in the illustration in Fig.4. It is clear that these samples are the more prone to be erroneously interpreted either as a logic 1 or 0, especially in presence of noise. In contrast, all other samples are much less likely to be misinterpreted. We can therefore expect that the majority of the table rows will contain the correct demodulated data.

3) Majority Vote: The next step is to identify which rows of the redundant demodulation table are the more likely to contain the correct demodulated data. For this, a voting score is computed for each row of the demodulation table. At the beginning of the process, all rows have a default score of 1. Rows are then compared two by two and if the data are identical, their score is increased by one, otherwise it remains unchanged. The process is repeated until all comparisons have been performed. In the illustration in Fig. 4, all rows have a final score of 7, except the 3^{rd} one which has a final score of 1. It can be noticed that this row indeed corresponds to samples that fall close to half the ADC output range, with an erroneous interpretation of the third message bit. The final scores are representative of a majority vote, where all rows with the highest voting score are the most likely to contain the correct demodulated data. This majority voting process is one of the key elements in ensuring high reliability.

4) Postamble Check: The last step is an additional step to further enhance the reliability. In most cases, the rows with the highest score after the voting process all contain identical data; demodulation could then be stopped by selecting these data. However, in few cases (especially for long data and/or very noisy signal), rows containing different data may have the same score. In such cases, it is mandatory to have an additional step to choose the demodulated data. This is accomplished by checking the last 4 bits of each candidate rows against the postamble. Whenever there is a match, the data contained in the row are selected. In case no match is found for all candidate rows, the transmission is considered as failed and an error flag is raised; the system may then take corrective action, for example by requesting that the message be resent.

It should be highlighted that in our algorithm, the postamble check has actually a dual function: on the one hand, it finalises the choice of demodulated data and, on the other hand, it performs error detection if no match is found. Error detection is classically implemented using Cyclic Redundancy Check (CRC); the process here is similar except that the check value is a fixed value that does not depends on the message. The advantage is that the check value does not have to be calculated, which limits the number of operations required.

D. Hardware Implementation Considerations

The proposed solution has been specifically defined with the objective of efficient implementation with small size and low power consumption. Indeed, except the amplification of the received signal that remains in the analogue domain, all the processing is carried out in the digital domain.

The processing can be easily implemented in a standard microcontroller, provided that it is equipped with an ADC, which is the case with most current products. As the proposed algorithm is based on direct demodulation, it does not require multiplication of the signal by a sinusoidal function nor recovery of the carrier as in the regular BPSK demodulation techniques, which limits the number of resources involved and therefore power consumption. In addition, it avoids any complex computational operations, the most demanding being averaging, which can be handled efficiently without overusing resources.

III. Simulation Results

In order to evaluate the performance of the proposed technique, a simulation testbench has been developed in Python. It comprises a first function dedicated to the generation of the BPSK-modulated signal. For the experiments presented in this paper, the carrier frequency is set to F_c = 500 kHz [11] and the number of periods per bit to $N_\mathrm{per} = 30$, which corresponds to a data rate of 16.67kbps. The peak-to-peak amplitude of the modulated signal is set at 50% of ADC the full scale. For each simulation run, the signal is generated based on a random message, and includes random noise as well as random phase shift. Potential inaccuracy of the carrier frequency (or sampling frequency) is also considered with the possibility to inject a frequency deviation into the carrier frequency. The noise considered in this simulation comprises white noise and quantization noise. The frame length, noise level and carrier frequency deviation are input simulation parameters that will be varied. The second function performs the quantification of the generated signal, considering an ideal 12-bit ADC model and a sampling frequency F_s = 4 MHz (i.e. $n_\mathrm{c} = 8$). Finally, the last function implements the processing algorithm and delivers the demodulated data or the error flag in case of failed transmission. The simulation parameters are summarised in Table II.

Evaluation of the robustness is based on two metrics:

- Transmission Success Rate (TSR), which is defined as the ratio between the number demodulated frames delivered by the processing algorithm (i.e. without flag errors) and the number of simulated frames,
- Packet Error Rate (PER), which is defined as the ratio between number of incorrect demodulations over the number of demodulated frames.

These metrics are computed on 1,000 random runs performed with the same simulation parameters.

TABLE II
Simulation Parameters

Fixed values	
Carrier frequency F_c	500 kHz
Data rate $1/T_{bit} = F_c/N_{per}$	16.67 kbps
Sampling frequency F_s	4 MHz
Variable values	
Frame length N_{bytes}	3 to 5 bytes
Signal noise level SNR	20 dB to −10 dB
Carrier frequency deviation $\Delta F/F_c$	0 to 0.1%

A. Performance Analysis w.r.t. Noise Level

First investigations were done to evaluate the influence on the noise level on the performance of the technique. Simulations were conducted without carrier frequency deviation, varying the noise level and frame length. Results are summarised in Fig. 4 which depicts the evolution of the transmission success rate versus the signal-to-noise ratio of the signal present at the ADC input, for different frame lengths.

Several comments arise from these results. A first striking outcome is that, despite the random phase of the transmitted signal, it exists a large range of SNR comprised between 20 dB down to −3 dB for which a perfect TSR of 100% is achieved, for all three frame lengths. The success rate then exhibits a gradual deterioration for decreasing SNR values until −7 dB, with a TSR that nevertheless remains higher than 97%. Depending of the application, such a value might be acceptable, given that the system is informed that the transmission was not successful and therefore has the option of requesting re-transmission of the message. Finally, for SNR values below −7 dB, there is a strong degradation, which is all the more significant the longer the frame is.

With regard to the packet error rate computed on demodulated frames, another striking outcome is that a perfect PER of 0% is achieved whatever the SNR level and the frame length. This means that every time the transmission is successful, the processing algorithm ensures correct demodulation of data, demonstrating its high reliability.

Overall, these first results validate the high level of robustness to noise of the demodulation algorithm as well as the efficiency of the error detection scheme.

B. Sensitivity Analysis w.r.t. Frequency Accuracy

Further experiments were conducted to analyse the sensitivity of the proposed solution to a possible inaccuracy in the carrier frequency. Indeed, the demodulation principle relies on knowledge of the carrier frequency and accurate setting of the sampling frequency to an integer multiple n_c of the

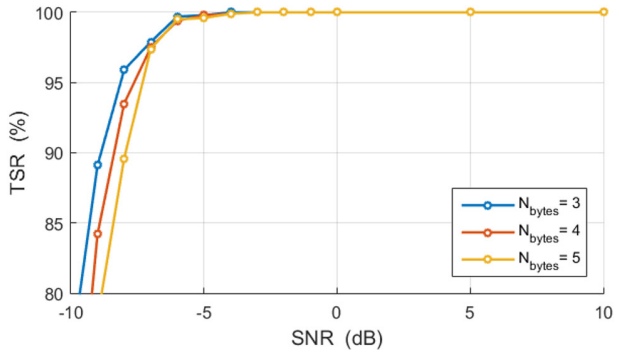

Fig. 4. Impact of Signal to Noise Ratio (SNR) on Transmission Success Rate (TSR), for frame lengths of 3, 4 and 5 bytes.

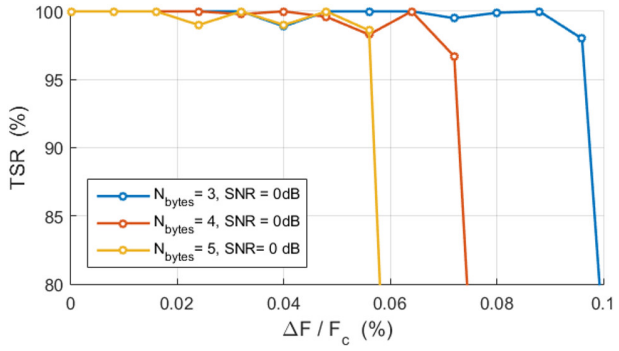

Fig. 5. Transmission Success Rate vs. frequency deviation for different frame lengths, for SNR = 0 dB.

carrier frequency. A deviation of the carrier frequency (or sampling frequency) from its expected value is susceptible to cause demodulation errors. Note that the accuracy of the carrier and sampling frequencies depends on the quality of the components selected for the hardware implementation, an aspect intrinsically linked to their cost.

Simulations were carried out introducing a progressive deviation of the carrier frequency up to 500 Hz (i.e. 0.1% deviation), for different noise levels and frame lengths. Fig. 5 shows the evolution of the transmission success rate as a function of the injected frequency deviation, for an SNR of 0 dB and for the three possible frame lengths. For small deviations, a high level of TSR close to 100% is maintained. However, a strong degradation is observed when the frequency deviation exceeds a certain threshold, this threshold being lower as the frame length increases. Specifically, for the maximum frame length of 5 bytes, the frequency deviation must remain below 0.06%.

To further assess this threshold, Fig. 6 reports the transmission success rate vs. the frequency deviation for different noise levels, in case of 5-byte frames. It can be observed that the noise level has a minor impact on the algorithm's performance. Indeed, whatever the SNR between 20 dB and −3 dB, a transmission success rate higher than 97% is achieved when the frequency deviation remains contained below 0.5%, which

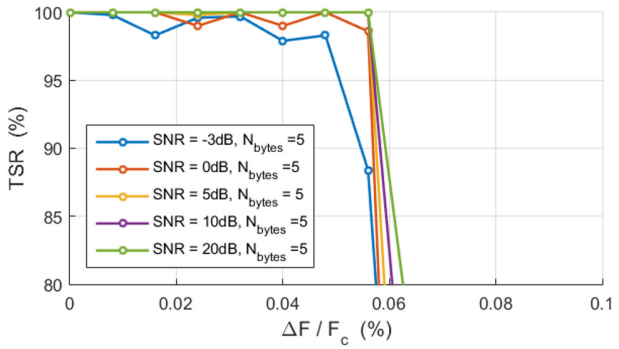

Fig. 6. Transmission Success Rate vs. frequency deviation for different noise levels, for 5-byte frames.

corresponds to a maximum tolerable frequency deviation of about 250 Hz.

These results point out that special attention must be paid to the hardware implementation with regard to the clock used to generate the modulated signal on the transmitter side and the clock used by the ADC on the receiver side. More precisely, to preserve the quality of the demodulation technique a frequency accuracy better than 500 ppm must be respected.

IV. Experimental Validation

The proposed solution has been validated through hardware measurements using the experimental setup illustrated in Fig. 7. It is based on the miniaturised GC transceiver architecture presented in [11], which comprises a Transmitter board (Tx) and a Receiver board (Rx) implemented using off-the-shelf components. The transmitter board consists of a microcontroller, a Direct Digital Synthesizer (DDS) and an operational amplifier (AOP) which permits to amplify the signal generated by the DDS. The received board includes an instrumentation amplifier and an operational amplifier to amplify the received signal, and a STM32L4 microcontroller equipped with a 12-bit ADC.

In the following experiment, the Tx board is used to generate a BPSK-modulated signal according the frame format defined in this paper. Signal parameters are set at the same values than in the simulation study, i.e. the BPSK-modulated signal is generated with a carrier frequency F_c=500 kHz and number of periods per bit $N_{\text{per}} = 30$, with a peak-to peak amplitude of 1.6V which corresponds to half the full-scale of the ADC embedded the Rx microcontroller. The Rx board is used to implement the demodulation technique. The signal delivered by the Tx is directly connected to the input of the 12-bit ADC, which performs its acquisition with a sampling frequency F_s set at 4 MHz. The resulting signal is then analysed by the processing algorithm embedded in the microcontroller. Note that the reference clocks used for the Tx and Rx comply with the frequency accuracy required by the demodulation technique. Interface boards have also been

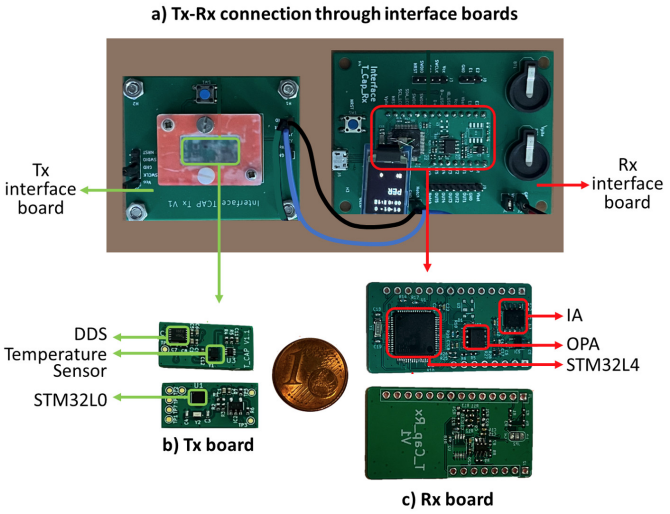

Fig. 7. Experimental setup. a) Tx-Rx connection through interface board, b) both sides of Tx board and c) both sides of Rx board.

developed in order to facilitate Tx-Rx connection and provide easy access to the test results.

The validation test that was conducted is as follows:

- Tx is programmed to send 5-bytes frames with random messages every 10 seconds for 10 hours,
- Rx is programmed to process the transmitted frames and store the demodulated data,
- The demodulated frames are then compared to the transmitted ones to compute TSR and PER metrics.

Note that an initial experiment was carried out to determine the noise level of the signal present at the ADC input on the Rx board. The noise level was measured at 23.7 dB.

The test achieved a TSR of 100% and a PER of 0% for the 3,600 frames processed, validating the principle of the proposed solution and its implementation in a microcontroller.

V. Conclusion

This paper introduced a novel demodulation technique designed for BPSK-modulated signals below the MHz range. The technique relies on signal digitisation by an ADC with a sampling frequency set at an integer multiple of the carrier frequency. The resulting signal is then processed by a dedicated digital processing algorithm, which implement efficient demodulation and error detection based on three main features, namely (i) averaging, (ii) majority voting on a redundant demodulation table and, (iii) postamble checking. The proposed solution was evaluated through both simulation and hardware experiments. Simulation results showed a high level of robustness to noise, with a 100% transmission success rate and a 0% packet error rate over a large SNR range from 20 dB to -3 dB. Hardware experiment on an STM32L4 microcontroller confirmed these results.

Besides efficiency, a key benefit is that it is a fully-digital solution that can be implemented at low-cost on a standard micro-controller; the main limitation resides in the constraint on the carrier and sampling frequencies, which must be set with an accuracy of 500 ppm. More generally, the proposed technique appears as a promising solution low-frequency communication applications, especially in the field of implanted sensor networks.

Future work will focus on optimising the processing algorithm with regard to energy consumption and practical implementation in the context of intra-body communication using galvanic coupling transmission.

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