# Approximate Computing for Test and Test of Approximate Computing

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***Abstract*—Approximate Computing (AxC) is nowadays a well established design and computing paradigm to produce more efficient computation systems by judiciously reducing the computation quality. In particular, AxC has been successfully applied to Integrated Circuits (ICs), in the last years in both ways: AxC for test and the test of AxC integrated circuits. The goal of this extended abstract is to summarizes the main concepts and highlights the research impacts of the work carried out from 2016 to 2021.**

***Index Terms*—Approximate Computing, Testing, Reliability**

## I. Introduction

Approximate Computing (AxC) is nowadays an established computing paradigm which takes advantage of the inherent application resiliency. It is based on the intuitive observation that selectively relaxing non-critical specifications may lead to improvements in power consumption, run time, and/or chip area [1].

AxC has been applied to the whole digital system stack. In particular, at circuit-level AxC has been applied basically in two ways: (i) *over-scaling* and (ii) *functional approximation*. Over-scaling consists in lowering the Integrated Circuit (IC) supply voltage to reduce its energy consumption. If the circuit is systematically designed to benefit from over-scaling, the timing errors are negligible compared to the energy gain. Nevertheless, the energy gain of over-scaling techniques turns out to be small. Therefore, a considerable amount of work has been presented on circuit *functional approximation*: the circuit functionality is systematically changed – thus, some controlled errors are introduced – to achieve energy-efficient circuits. Circuit error can be measured according to different error metrics.

This work focuses on digital Approximate Circuits, regardless of the approach employed to obtain them. Since approximation changes the IC behavior, it is important to revisit test.

On the one hand, the occurrence of a defect in the circuit can lead it to produce unexpected catastrophic errors. On the other hand, some defects can be tolerated, when they do not induce errors over a certain level (i.e., approximation during the test procedure). If properly investigated and managed, this phenomenon could lead to increase the number of circuits passing the test phase. This is usually referred to as *production yield increase*. Indeed, selling acceptably-functioning circuits – that still respect the user requirements, despite the defects – would increase the profit of semiconductor companies. This is especially critical due to the effect of *process variability* on CMOS technologies. Indeed, CMOS technologies at nano-scale have increasingly negative performance in terms of circuit yield and reliability. To take advantage of the opportunity offered by AxICs, conventional test flow should be revisited.

Therefore, *Approximation-Aware testing (AxA testing)* comes into play. We identify three main AxA testing phases:

1) AxA fault classification,
2) AxA test pattern generation,
3) AxA test set application.

Briefly, *fault classification* has to divide faults into *catastrophic* (to test) and *acceptable* (not to test), according to a metric; *test pattern generation* has to produce tests able to cover all the catastrophic faults and, at the same time, to leave acceptable faults undetected; finally, the *test set application* role is to analyze the test outcomes and classify AxICs accordingly, into *catastrophically faulty*, *acceptably faulty*, and *fault-free*. Only AxICs falling into the first group will be rejected. Ultimately, this leads to a yield increase compared to the conventional test flow.

## II. Impact of the Research

In this work carried out from 2026 to 2021, we thoroughly investigated the three AxA testing phases. Moreover, we reviewed and evaluate the existing AxA testing techniques in our seminal paper [1]. We proposed new metrics to accomplish the evaluation, and we perform extensive experiments to measure the effectiveness of state-of-the-art techniques. Obtained results show good maturity of fault classification and test pattern generation approaches, while some problems emerge concerning test set application techniques. In fact, only under specific conditions, existing test set application techniques achieve satisfactory results. The impact of this

research works inspired others test related paper such as [2], however outcomes also lead to investigate the use of AxC to fault tolerance and reliability of integrated circuits and systems [3], [4]. Accordingly to Google Scholar, those papers reaches more 100 citations proving the value of the research work

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