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Producing a Bidirectional ATPG Compliant Verilog-HDL Memory Model of SRAM Memory

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***Abstract*—This paper proposes a methodology to produce a digital Verilog-HDL netlist of an SRAM memory, based on an initial SPICE model. The digital model considers the bidirectional nature of the memory, and is ATPG-compliant, allowing the generation of test patterns, and fault simulation.**

***Index Terms*—Memory testing, Automatic Test Pattern Generation (ATPG), Memory model, SRAM.**

I. Introduction

Modern components such as System On Chip (SoC) have increasing performance requirements for calculation, which consequently requires more memory capacity, leading to a significant increase of the embedded memory size and density. The increasing integration densities of memories is achieved by approaching the limits of the technology, which makes them more prone to defects that can impair their correct functioning [1]. It is therefore important to test memory components to reduce the defective-parts-per-million (DPPM) measure. Common test methods for testing memory components are based on the use of March algorithms [2], using Functional Fault Models (FFMs). However, this methodology could become insufficient considering the increasing complexity of the memories. Novel test solutions for digital circuits have emerged to anticipate this problem, such as the Cell-Aware (CA) test, which relies on a post-layout transistor-level approach [3], and based on a structural consideration of the circuit to be tested. Moreover, the CA methodology has been proposed in the field of memory testing, and more specifically, for the testing of SRAM memories [4].

In order to apply such test methodology to memory components, an accurate digital model of the memory that closely respects the architecture and the behavior of its analog model has been produced [4]. Moreover, in order to generate test patterns and to run a fault simulation, the digital model must comply with digital test tools such as Automatic Test Pattern Generator (ATPG) to allow the generation of test patterns. This paper proposes a methodology to produce a bidirectional ATPG-compliant Verilog-HDL model of SRAM memory, based on an initial analog model (SPICE netlist).

II. Proposed Methodology

The proposed flow (Fig. 1.) is based on [4], and proposes an extension to allow bidirectionality in the digital model of the SRAM memory. The additional bidirectionality consideration allows all the sub-circuits of the memory model, such as write driver and sense amplifier, to be represented in a single model, which remains compatible with digital test tools.

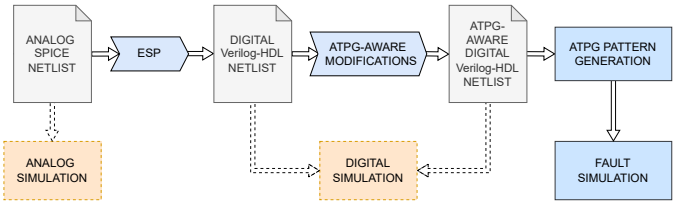

Fig. 1. Flow for producing a bidirectional ATPG-compliant Verilog-HDL netlist from a SPICE netlist.

The initial hierarchical SPICE netlist is converted to a Verilog-HDL digital equivalent netlist using a functional verification tool. The obtained digital netlist is then adapted to preserve its intrinsic bidirectional behaviour, while the top model's ports remain only input and output ports. The analog and the digital netlists can be simulated to verify their functional equivalence throughout the production process.

To evaluate the proposed methodology, a reduced analog (SPICE) memory model of SRAM that includes the necessary modules that ensure its correct functioning has been designed (Fig. 2.). The model consists of the elementary modules that represent an SRAM memory: one memory cell (in 6-Transistors (6T) topology) to carry the information, one precharge circuit to charge and equalize the memory bitlines for read and write operations, one sense amplifier to read the information from the memory cell, and one write driver to force a value in the memory cell.

In order to maximize the simplification of the analog memory model, only one memory cell is used, allowing the memory model to operate without a row decoder and a column decoder. The row decoder is a combinational circuit that is already compliant with an ATPG. Therefore, its removal is not a real concern for the purpose of this proposed methodology. Using a one-cell SRAM memory model also allows to remove the column decoder, which simplifies the model.

The reduced analog SRAM memory model is simulated using analog simulation tools (Fig. 3.). Read and write operations are performed to ensure its behavioral correctness.

The hierarchical SPICE transistor-level description of the memory model is then converted to a first hierarchical Verilog-HDL netlist, respecting construction (Fig. 2.). The conversion

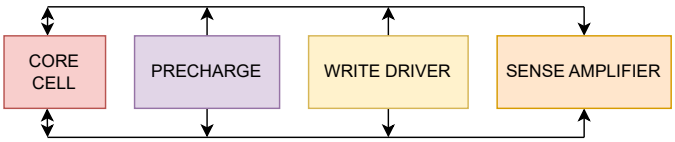

Fig. 2. High level schematic representation of the reduced SRAM memory model.

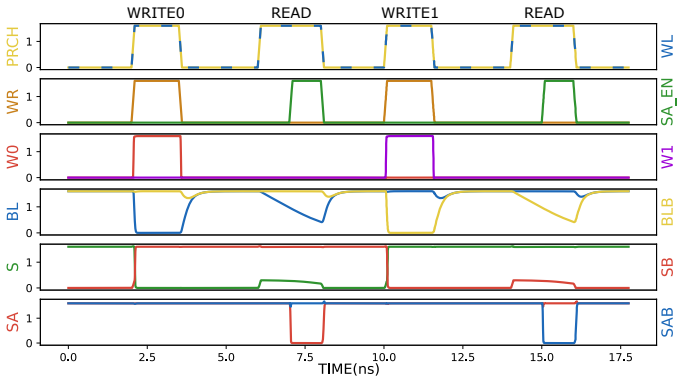

Fig. 3. Analog simulation of the reduced SPICE model of SRAM memory.

is performed using a functional verification tool named ESP.

Modifications are then performed on the generated Verilog-HDL netlist to ensure that its functional simulation results match with the analog simulated results (Fig. 3.). Most of the modifications are related to modules ports directions, and adjusting the digital primitives' drive strength to represent the analog intra-module and inter-modules interactions.

Considering the digital domain imposes the use of discrete values such as '1' or '0', the amplification role of the digital sense amplifier module is simplified with a set of two *bufif1* primitives. These primitives transmit the bitlines' digital values to the output ports of the sense amplifier module, depending on the input control value.

In order to preserve the bidirectional nature of specific SRAM memory sub-circuits, such as the core-cell, *tranif(0/1)* primitives are used in the digital domain to conserve the bidirectionality. However, these digital primitives are not defined for the considered ATPG. A possible solution is to replace the undefined primitives with substitution modules that uses ATPG defined primitives such as MOS, to mimic as close as possible the undefined primitives behavior (Fig. 4.).

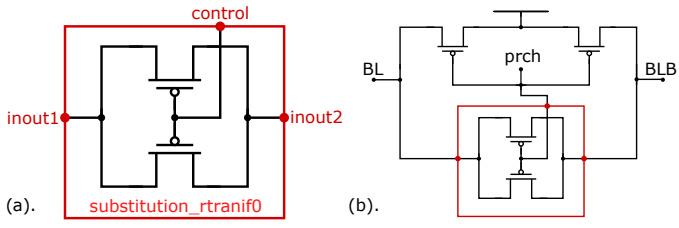

Fig. 4. (a) Module to substitute the Verilog-HDL *tranif0* primitive. (b) Precharge sub-circuit using the substitution module.

These substitution modules use a set of two digital resistive MOS transistors to represent *rtranif(0/1)* primitives. The first module uses two digital resistive *RpMOS* to represent the *rtranif0* primitive (Fig. 4. (a)). And the second module uses two digital resistive *RnMOS* transistors to represent the *rtranif1* primitive. For both modules, the two digital resistive MOSs are controlled by a shared control input port, and each of the transistors are mapped in a complementary unidirectional manner, connecting together the two inout ports of their respective substitution module.

These substitution modules, which are built using ATPG defined primitives, are used to replace the core-cell's access transistors, and the pre-charge's equalizer transistor in the digital ATPG-aware memory model, which were represented with *tranif1* and *tranif0* primitives, respectively. This design, using primitive substitutions, coupled with drive strength adaptations, allows the ATPG-aware digital model (that embeds a write driver and a sense amplifier) to be simulated (Fig. 5.) and to be processed by an ATPG, allowing a fault simulation.

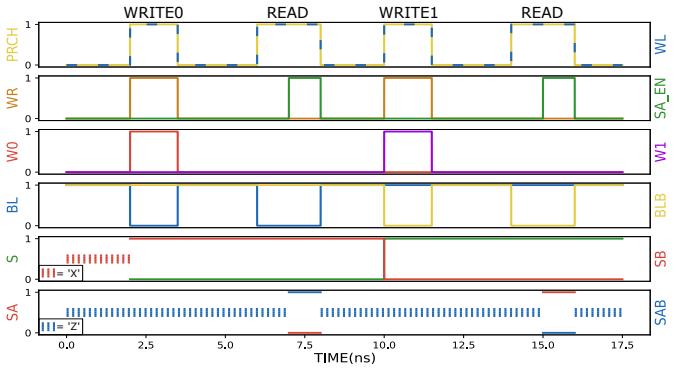

Fig. 5. Digital simulation of the reduced Verilog-HDL model of SRAM memory.

III. Conclusion

This paper proposes a methodology to produce a bidirectional ATPG-compatible digital memory model, based on an initial SPICE model of an SRAM memory. The resulting digital model can be simulated to ensure its functional equivalence with the analog model, and can be processed by an ATPG to generate test patterns and to run a fault simulation.

An ideal application for this proposed methodology would be to produce digital bidirectional ATPG-compatible models for other components, or other types of memory such as Magnetic Random Access Memories (MRAMs), in order to apply the CA methodology to emerging technologies.

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