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Cost-Effective Analytical Models of Resistive Opens Defects in FinFET Technology

Gustavo Aguirre, Freddy Forero, Victor Champac, *Senior Member, IEEE*, Michel Renovell, Florence Azais, Mariane Comte, and Jean-Marc Galliere

***Abstract*— FinFET technology has become an attractive candidate for high-performance and power-efficient applications. However, its susceptibility to defects increases due to the complexity of the process fabrications and smaller feature sizes. This article proposes compact and low-cost analytical models to evaluate the delay increase in FinFET-based circuits due to resistive open defects. The models rely on electrical simulations to precharacterize the circuit library. Analytical expressions are developed for the three types of resistive opens that may occur in FinFET-based logic cells using multifin and multifinger structures. These types of resistive opens include: a resistive open at the drain or source of the transistors (RODS), a resistive open affecting the gate of a single transistor, and a resistive open affecting the gates of both nMOS and pMOS transistors. Compact analytical models are also developed to evaluate the delay increase due to the resistive open defects under process variations. Independent and correlated process variations are taken into account. The analytical models have been validated against SPICE electrical simulations. The proposed analytical models can be used to evaluate the detectability of resistive open defects, significantly reducing the cost of dealing with different defect sizes. Potential applications of the developed analytical models are delineated. This work allows us to have higher quality and reliable electronic products.**

***Index Terms*— Analytical models, FinFET technology, delay, resistive opens, test.**

I. Introduction

FinFET technology has turned into an attractive candidate for high-performance and power-efficient applications. A FinFET transistor is constructed by wrapping a metal gate around a silicon fin, thus making the transistor channel. The wrapping of the fin results in a stronger electrostatic control over the transistor channel, hence improving short-channel effects behavior [1]. Manufacturing defects, encompassing bridges and opens, occur during the complex fabrication process of semiconductor devices. Within the FinFET process, the prevalence of such defects amplifies owing to the highly scaled geometries and intricate manufacturing procedures involved, as highlighted by Sawicki [2]. Hence, testing FinFET-based circuits becomes challenging, and studies have been conducted on tests for defects in FinFET technology.

Subtle unique defect behaviors appear in FinFET technology, which conventional fault models cannot fully explain. The more extensive use of multifin and multifinger structures, adding parallel current paths, in FinFET-based circuits make some defects more nondetectable or hard to detect [3], [4], [5], [6].

This article proposes compact and low-cost analytical models to evaluate the delay increase in FinFET-based circuits due to resistive open defects. The analytical models are proposed for normal process conditions and process variations. These models encompass three types of resistive opens encountered in FinFET-based logic cells using multifin and multifinger structures, including those affecting drain/source regions, single transistor gates (SROs), and both nMOS and pMOS transistor gates. Some of the considered open defects are unique to FinFET technology. Potential applications of the developed analytical models are delineated.

The rest of the article is organized as follows: Section II reviews the state of the art in research relevant to this article. Section III discusses resistive open defects in FinFET logic gates and their delay modeling. Section IV presents the analytical models to estimate the gate delay increase due to resistive opens under nominal process conditions. Section V presents the analytical models to estimate the gate delay increase due to resistive opens under process variations. Section VI presents the precharacterization cost of the proposed analytical models. Section VII outlines the proposed analytical models' potential applications. Finally, Section VIII presents this work's conclusions.

II. State of the Art

As mentioned in the introduction, the more widespread use of multifin and multifinger structures in FinFET-based circuits adds parallel current paths, leading some defects to be more difficult to detect or even undetectable [3], [4], [6]. Bhoj et al. [3] have developed fault models for opens and shorts in FinFET gates. In [4], it is shown that defects on a different number of fins result in different faulty behaviors and that one single defect may affect multiple correlated gates. Open defects nondetectable by a Boolean-based test and hard to detect by a delay-based test have been studied in [5] and [6]. More recently, a new defect mechanism, named b-open defect, in FinFET technology has been found [7]. The behavior of

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this new defect mechanism should be taken into account to achieve higher defect coverage. In [8], resistive open defects in embedded cells under variations are studied. Machine learning procedures are used to classify a circuit as marginal due to defects or just slow due to variations. The inputs to the procedure are delay tests at different voltages and frequencies.

Fault simulation approaches are also crucial for high-quality electronic products. Li et al. [9] have proposed a circuit-level fault model for resistive opens. The fault models are easy to implement in fault simulation. Czutro et al. [10] have proposed a simulator for small-delay faults caused by resistive open defects that could occur in CMOS technology. They present a small-delay fault simulation methodology to calculate a realistic coverage of resistive open faults based on the probability of occurrence of low-resistance interconnect open defects. The delay fault sizes are mapped into corresponding values of resistive opens using a straightforward equation that calculates the delay increase due to the open. Yamazaki et al. [11] have proposed an efficient simulation method for small delay faults, and they use the simulator to diagnose resistive open faults. Chugh and Karanam [12] have proposed making advanced fault simulations to assure quality in safety-critical applications. They present a solution integrating functional verification and fault simulation into a single flow.

III. Resistive Opens in FinFET-Based Logic Gates and Their Delay Modeling

A. Causes of Open Defects

A resistive open defect is defined as the unintentional partial absence of material in a connection, which can be modeled as a defect resistor between two circuit nodes that are meant to be connected. Interconnects, contacts, and vias are particularly susceptible to such open defects [13]. The causes of these defects have been discussed in various studies, including [6], [13], [14], [15], and [16].

Measurements to characterize the possible resistance values of resistive open defects have been conducted in semiconductor technology [17]. Defective opens with resistances greater than 10 MΩ ($R > 10$ MΩ) are classified as strong opens, while those with resistances less than 10 MΩ ($R < 10$MΩ) are classified as weak opens. While weak opens allow the circuit to function, they cause degraded performance, often manifesting as signal delay.

Known sources of open defects are: 1) erosion and dishing due to the chemical mechanical polishing (CMP) [14]; 2) the presence of undesirable particles during the lithographic process [15]; 3) incomplete interconnect or via etch [13]; and 4) Optical proximity effects an lens imperfections in the optical system, and others.

Fig. 1(a) illustrates an open in the CB layer (CB layer is used to connect the gate fingers) caused by a spot defect [15]. A dust particle blocks the passage of light to the photoresist during exposure. As a consequence, oxide remains in the trench due to the unexposed photoresist, which causes an open during the metal deposition as illustrated in Fig. 1(a). A missing material in the spacer and a broken line due to incorrect patterning etching of the poly [16] translate to open defects as illustrated in Fig. 1(b).

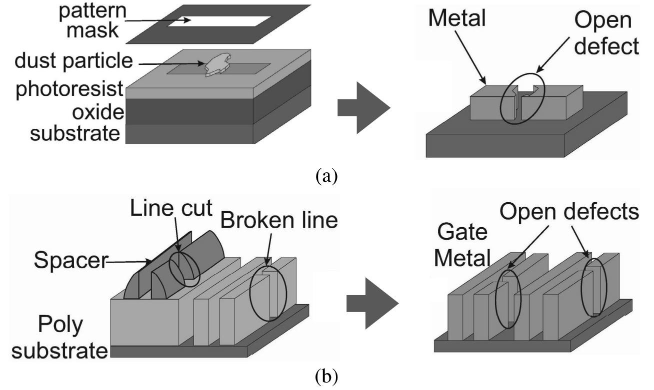

Fig. 1. Causes of open defects in FinFET technology. (a) Open due to an opaque particle. (b) Open due to a spacer-cut and a poly-broken line of the SADP finger process.

B. Resistive Opens in FinFET Technology

FinFET-based logic gates are designed with multiple fins and multifingers configurations to achieve desired drive strengths. In multifinger structures, the fins are intersected by metal gates, referred to as fingers, which are interconnected with another layer. Considering the utilization of multifin and multifinger structures, three types of resistive opens may occur. The following nomenclature is used throughout the article.

1) *P:* Number of pMOS fins connected in parallel.
2) *N:* Number of nMOS fins connected in parallel.

To simplify the discussion, we depict the three resistive open topologies using synthetic schematics for the inverter gate (see Fig. 2). N parallel n-fins are represented by an equivalent transistor denoted as nMOS$_N$, while P parallel p-fins are represented by an equivalent transistor denoted as pMOS$_P$. The index k_n (k_p) indicates the number of disconnected n-fins (p-fins) in the equivalent transistor, whereas the index $N - k_n$ ($P - k_p$) indicates the number of nondisconnected fins in the equivalent transistor.

1) *Resistive Open at the Drain/Source of the Transistors:* This defect affects a transistor's source (or drain), as depicted in Fig. 2(a). Only one network is affected, with a subset of fins k_p within this network being disconnected.
2) *Resistive Open at a SRO:* This defect affects the gate of a single transistor as depicted in Fig. 2(b). Only one network is affected, with a subset of fins k_p within this network being disconnected.
3) *Interconnect Resistive Open (IRO):* This defect affects the gate of both the n and p networks as depicted in Fig. 2(c). The defect results in the disconnection of a subset k_n and k_p fins.

The behavior of certain resistive opens, particularly interconnect resistive opens, can be influenced by their location, as this determines the capacitance values at the ends of the defect [18]. Our work, however, focuses on resistive opens within logic cells, commonly referred to as intragate resistive

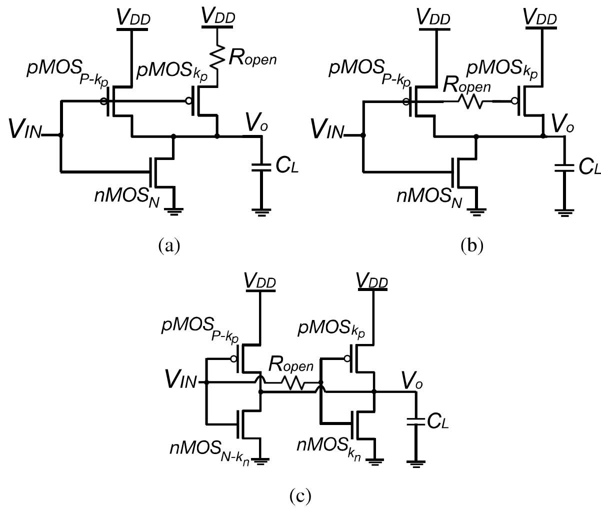

Fig. 2. Types of resistive opens for an inverter gate designed with multifins and multifingers. (a) RODSs. (b) Resistive open at a SRO. (c) IRO.

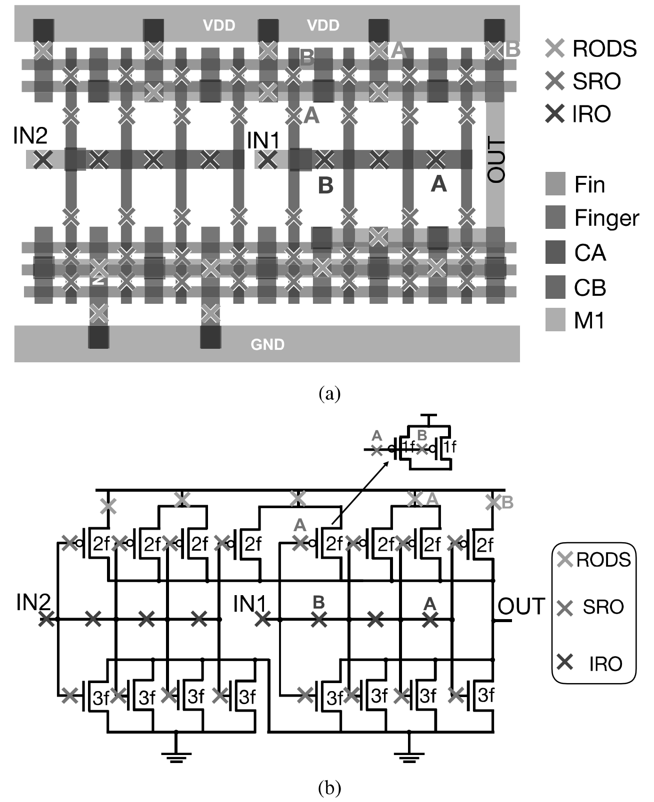

Fig. 3. Multifin/multifinger two-NAND gate with resistive open defect locations. (a) Layout of the two-NAND gate. CA layer is used to connect the drain–source of the fins. CB layer is used to connect the gate fingers. (b) Alike-layout schematic of the two-NAND gate.

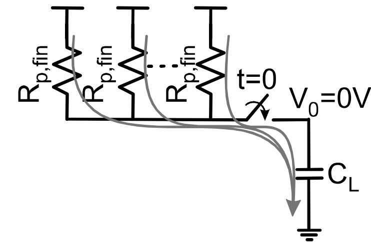

Fig. 4. RC model for the two-NAND gate with a rising output transition.

opens [19]. Due to the 3-D structure of FinFET transistors, defects affecting only a single network within a gate and disconnecting a subset of fins have been observed [3], [4], [5], [6]. These defects lead to reduced drive strength, resulting in small delays. Consequently, small delays pose a greater risk in FinFET technologies compared to planar technologies [6]. Open defects affecting both the nMOS and pMOS networks within a gate have been analyzed in detail in [5].

The layout of a multifin/multifinger two-NAND gate used throughout the article is shown in Fig. 3(a). An alike-layout schematic of the two-NAND gate is shown in Fig. 3(b). Each input utilizes four fingers, with each finger comprising three parallel nMOS fins and two parallel pMOS fins. In total, the two-NAND gate includes 12 nMOS fins ($N = 12$) and eight pMOS fins ($P = 8$) per input.

The layout of the two-NAND gate (see Fig. 3) was designed using an in-house layout and extraction tool [5]. The dimensions of FinFET transistors and middle-of-the-line (MOL) interconnect structures are based on Intel's 14-nm FinFETs technology [20]. The logic cells are simulated with the industrial SPICE BSIM-CMG standard FinFET Compact Model [21] using a predictive 14 nm PTM-MG bulk model [22]. Within the layout and also in the schematic circuit, various markings signify potential locations of different types of resistive opens: green marks denote potential RODS defects, blue marks highlight potential SRO defects, and red marks indicate potential IRO defect locations.

Certain internal open locations in parallel fins are not depicted in the two-NAND gate schematic. It can be observed that single-resistor open (SRO) defects, indicated by blue marks, can impact the gate of up to three parallel fins. IRO defects, which affect both the nMOS and pMOS networks, can impact one, two, three, or all four nMOS and pMOS networks. While some open defect locations are specific to the particular layout design, the resistive opens studied here are applicable to other layout designs and multilevel MOL structures. In the layout, certain defect locations to be analyzed in this article are marked. The colors of the letters A and B correspond to different types of open defects.

C. Delay Modeling

Fig. 4 illustrates an RC model for the two-NAND gate [see Fig. 3(a)] during a rising output transition. The rise propagation delay of the RC network depicted in Fig. 4 can be approximated by the following equation [23], [24]:

$$D_{\text{rise}} = \ln(2) R_{p,\text{fin}} C_L / P \tag{1}$$

where $R_{p\text{fin}}$ denotes the resistance of one pMOS fin and C_L represents the load capacitance.

Expressions analogous to (1) can be derived for the falling propagation delay and for various types of logic gates.

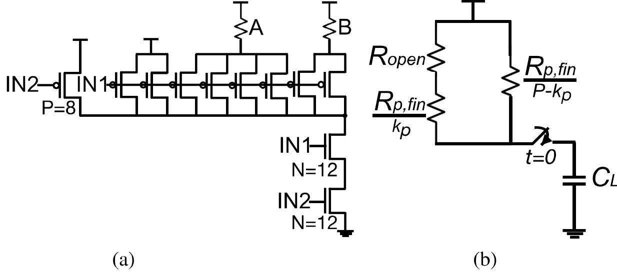

Fig. 5. Two-NAND gate with possible RODS defect locations and its RC model. (a) Two-NAND gate with possible RODS defect locations. (b) RC Model for a NAND gate with an RODS defect.

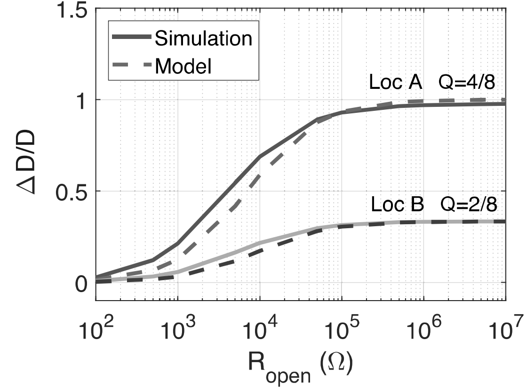

Fig. 6. Analytical model versus SPICE simulation for the normalized delay increase due to a RODS defects.

Upon rewriting (1) in terms of $R_{p,\text{fin}}$, the following expression is obtained:

$$R_{p,\text{fin}} = \frac{P D_{\text{rise}}}{\ln(2) C_L}. \tag{2}$$

Equation (2) with a SPICE electrical simulation can be used to calculate the resistance of a single pMOS fin. The process involves simulating an inverter logic gate along with its load capacitance using SPICE, and measuring the rise propagation delay time (D_{rise}). This obtained value of D_{rise} is then utilized within (2) to calculate the resistance of a single pMOS fin. A similar methodology can be applied to ascertain the resistance of a single nMOS fin.

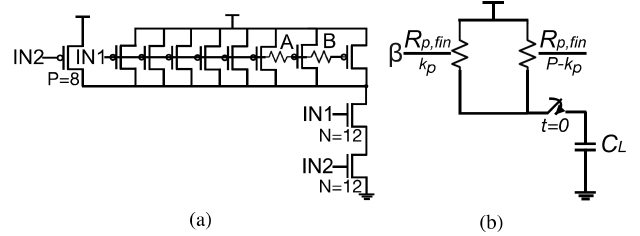

Fig. 7. Two-NAND gate with possible SRO defect locations and its RC model. (a) Two-NAND gate with possible SRO defect locations. (b) RC Model for a NAND gate with an SRO defect.

IV. Analytical Models for Resistive Opens at Nominal Process Conditions

A. Resistive Open at the Drain/Source of the Transistors

Fig. 5(a) depicts a simplified schematic of the two-NAND gate [see Fig. 3(a)], illustrating two potential locations of a RODS defect. Open location A affects four pMOS transistors, whereas open location B affects two pMOS transistors. For the same value of resistance of the open, the delay increase for location A surpasses that of location B due to the higher number of affected transistors in location A.

An RC model illustrating a NAND gate with a RODS defect for a rising output transition is presented in Fig. 5(b). Here, R_{open} denotes the resistance value of the open defect, $R_{p,\text{fin}}/k_p$ signifies the equivalent resistance of the k_p fins affected by the open, and $R_{p,\text{fin}}/(P - k_p)$ represents the equivalent resistance of the $(P - k_p)$ fins nonaffected by the open.

From the RC model [depicted in Fig. 5(b)], the normalized delay increase ($\Delta D/D$) for a rising output transition of the NAND gate with an RODS defect is expressed as follows:

$$\frac{\Delta D}{D} = \frac{Q}{1 + R_{p,\text{fin}}/k_p R_{\text{open}} - Q} \tag{3}$$

where $Q = k_p/P$ represents the ratio between the number of affected fins (k_p) and the total number (P) of parallel fins.

Fig. 6 illustrates the delay increase obtained from SPICE simulations alongside that derived using (3). The delay increase is presented for defect locations A and B (see Fig. 5), corresponding to $Q = 4/8$ and $Q = 2/8$, respectively. It can be observed that the curve obtained with (3) has a good agreement with the SPICE simulation curve.

B. Resistive Open at a Single Transistor Gate

Fig. 7(a) illustrates a simplified schematic of the two-NAND gate [see Fig. 3(a)], depicting two potential locations of an SRO defect. This type of defect induces a delay in the signal reaching the gate(s) of the affected transistors. The magnitude of the delay increase depends on the open's resistance value (R_{open}). Consequently, the affected transistors exhibit delayed turn-on compared to the nonaffected transistors, resulting in an increased delay for the affected gate.

An RC model for a NAND gate with an SRO defect for a rising output transition is depicted in Fig. 7(b). Here, $R_{p,\text{fin}}/(P - k_p)$ represents the equivalent resistance of the fins nonaffected by the SRO defect. The impact of the resistive open in the affected transistors is represented by a resistance $R_{p,\text{fin}}/k_p$ multiplied by a β factor. The fundamental concept underlying this model is that the output is charged with a defect-free current provided by the nondefective transistors alongside with a defective current contributed by the transistors affected by the open. The β factor signifies the extent to which the equivalent resistance of the affected transistors increases. This factor increases as the open's resistance value increases.

From the RC model [see Fig. 7(b)], the normalized delay increase ($\Delta D/D$) for a rising output transition of the NAND gate with an SRO defect is expressed as follows:

$$\frac{\Delta D}{D} = \frac{k_p/P - k_p/\beta P}{1 + k_p/\beta P - k_p/P} = \frac{Q - Q/\beta}{1 + Q/\beta - Q} \tag{4}$$

where $Q = k_p/P$ represents the ratio between the number of affected fins (k_p) and the total number of fins (P).

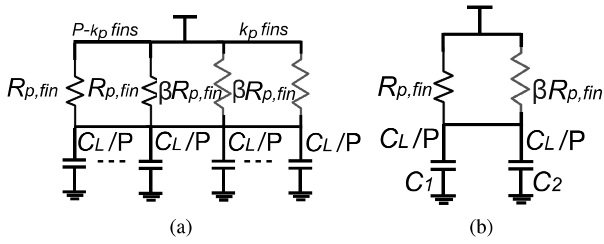

Fig. 8. RC models of the charging networks modeling β for the SRO defect. (a) RC model. (b) Simplified RC model comprising single defect-free and defective RC branches.

Estimation of the β Factor: Fig. 8(a) illustrates an RC model of the charging network of the two-NAND gate with a resistive open at a SRO. In this model, the NAND gate comprises k_p defective pMOS fins and $P - k_p$ defect-free pMOS fins. Defect-free charging branches ($R_{p,\text{fin}}$) are used for the pMOS fins nonaffected by the open, while defective charging branches ($\beta R_{p,\text{fin}}$) are used for the pMOS fins affected by the open (SRO defect). The total load capacitance (C_L) is divided by P, which is the total number of parallel pMOS fins for the input of interest in the NAND gate. The RC network has a resistance equal to the parallel of all the branch resistances that charges a capacitance equal to C_L. The RC network encompasses a resistance equivalent to the parallel of all branch resistances, which charges the total capacitance C_L.

The defective fin possesses a resistance of $\beta R_{p,\text{fin}}$, leading to a potentially different delay compared to the defect-free branches. However, within the context of the entire RC network, achieving different delays for individual branches is not feasible, as they collectively contribute to a single delay. To ensure uniform delays across the branches, the load capacitance associated with defect-free branches must exceed that of the defective branches. This observation will be used in subsequent analyses.

A simplified RC model comprising a single defect-free RC branch and a single defective RC branch is depicted in Fig. 8(b). As previously discussed, capacitance C_1 must be larger than the capacitance C_2. The combined capacitances C_1 and C_2 sum up to $2C_L/P$ as shown in the following equation:

$$C_1 + C_2 = 2C_L/P. \tag{5}$$

It is noteworthy to mention that the delay of the entire RC reduced model aligns with the delay of the RC as a whole model when $\beta = 1$. The following relationship can be deduced from the simplified circuit [see Fig. 8(b)], ensuring that the defect-free and defective branches maintain the same delay:

$$\ln(2)(R_{p,\text{fin}}C_1) = \ln(2)(\beta R_{p,\text{fin}}C_2). \tag{6}$$

Solving for C_1 from (5) and substituting it into (6), yields the following equation:

$$C_2 = \frac{2C_L/P}{1+\beta}. \tag{7}$$

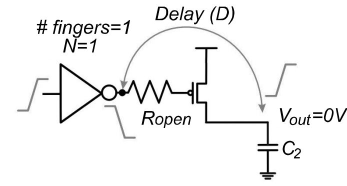

Fig. 9. SPICE characterizing circuit to compute β.

Solving for β in the right term of (6) for a single pMOS fin, the β factor is obtained

$$\beta = \frac{D}{\ln(2)R_{p,\text{fin}}C_2}. \tag{8}$$

The characterizing circuit depicted in Fig. 9 is used to derivate the β factor. This circuit configuration comprises a minimum-sized inverter, a resistance R_{open} representing the SRO defect, a pMOS fin device, and a capacitance C_2 connected at the drain of the pMOS fin. The purpose of this characterizing circuit is to estimate the overall delay impact of the SRO defect (R_{open}). In SPICE simulation, a rising transition is applied at the inverter input, and the propagation delay (D) is measured between the inverter output and the drain of the pMOS fin. The obtained value of D is subsequently utilized in (8) to compute the β factor.

It is important to note that the value of C_2 is initially unknown in the characterizing circuit (see Fig. 9). Therefore, an iterative process is employed to determine the final value of C_2 and, consequently, C_1. The iteration process begins with a simulation of the characterizing circuit using an assumed value of $C_2 = C_L/2$ (see Fig. 10). The resulting propagation delay is then utilized in (8) to compute the β factor. Subsequently, the obtained β factor is employed to calculate a new value of C_2 using (7). This new value of C_2 is compared with the one used in the simulation. If the difference between the two C_2 values exceeds a certain threshold ϵ, the new C_2 value is utilized in the characterizing circuit for another simulation. This iterative process is repeated until the difference between the C_2 value used in the simulation and the newly computed value from (8) falls below a specified threshold ϵ. The last determined value of C_2 is then employed to compute the final β factor using (8).

Fig. 11 illustrates an example of the iteration process utilizing the characterizing circuit depicted in Fig. 9. In this example, $R_{\text{open}} = 650$ kΩ and $C_L/P = 5.76fF/8 = 0.72fF$ are utilized. The dots on the blue curve represent the C_2 values utilized for the simulations with the characterizing circuit, while the dots on the red curve are obtained using (7). The intersection point between these curves corresponds to the correct values of β and C_2 for the simplified RC circuit [see Fig. 8(c)] under the specified conditions of $R_{\text{open}} = 650$ kΩ, $C_L = 8fF$, and $P = 8$.

The β values were obtained using (8) in conjunction with the characterizing circuit (see Fig. 9), which utilizes a single fin. However, it is crucial to acknowledge that the resistive open may affect more than one fin, resulting in an increased input gate capacitance and, consequently, a higher delay. To account for the delay difference between that obtained

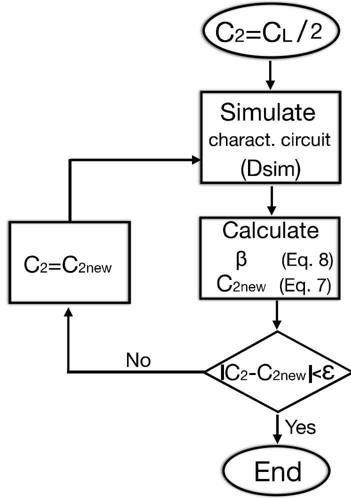

Fig. 10. Flow diagram to compute β iteratively.

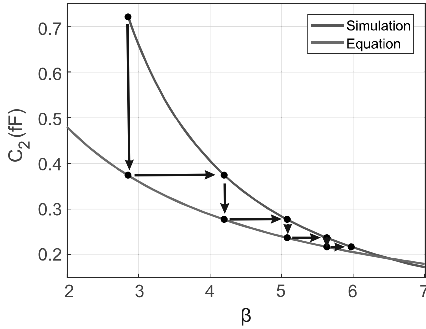

Fig. 11. Example of the iteration process using the characterizing circuit shown in Fig. 9.

with the characterizing circuit and the actual affected k-fins, a correction factor (f) is introduced

$$f = \frac{C_{\text{trans}}}{C_{\text{def}}} \tag{9}$$

where C_{trans} is the input gate capacitance of a single fin used in the characterizing circuit, and C_{def} is the sum of all the input gate capacitances of the fins affected by the defect.

Finally, the obtained β values with (8) are multiplied by the correction factor f.

Fig. 12 depicts the delay increase obtained from SPICE simulations and that derived from the proposed modeling strategy applying the correction factor f to β. The delay increase is presented for defect locations A and B (see Fig. 7), corresponding to $Q = 2/8$ and $Q = 1/8$, respectively. It can be observed that the curve obtained using (4) exhibits good agreement with the curve derived from SPICE simulation results.

C. IRO

The interconnect resistive open defect affects both the nMOS fins and the pMOS fins, resulting in an inverter configuration, as illustrated in Fig. 13(a). When IN2 = 0 and there is a falling input transition at IN1, this defect induces a delay in the signal reaching the gates of the affected fins, and

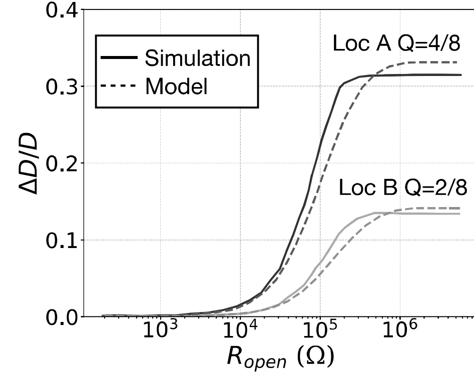

Fig. 12. Analytical model versus SPICE simulation for the normalized delay increase due to SRO defects.

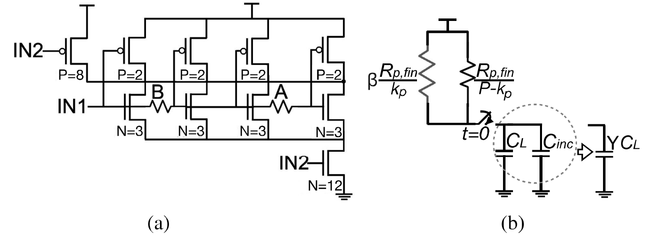

Fig. 13. Two-NAND gate with possible IRO defect locations and its RC model. (a) Two-NAND gate with possible IRO defect locations. (b) RC Model for a NAND gate with an IRO defect.

as a consequence, the affected nMOS and pMOS fins behaves as follows.

1) The affected pMOS fins experience delayed turn-on compared to the nonaffected pMOS fins.
2) The affected nMOS fins encounter delayed turn-off relative to the nonaffected nMOS fins.

The delay of the defective gate increases as the resistance of the defect increases. Furthermore, the gate delay rises as the number of affected nMOS fins and pMOS fins increases.

The RC model of the interconnect resistive open for a rising output transition is depicted in Fig. 13(b). Here, $R_{p,\text{fin}}/k_p$ represents the equivalent resistance of the pMOS fins affected by the defect, while $R_{p,\text{fin}}/(P - k_p)$ represents the equivalent resistance of the pMOS fins unaffected by the defect. The effect of the defect is included as follows.

1) First, to model the increase in the delay for turning on the affected pMOS fins, the resistance $R_{p,\text{fin}}$ is multiplied by a factor β.
2) Second, to account for the increase in the delay for turning off the nMOS fins, a capacitance C_{inc} is added to the load capacitance. Mathematically, the modified load capacitance can be expressed as a γ factor that multiplies the load capacitance [see Fig. 13(b)], with $\gamma = (C_L + C_{\text{inc}}/C_L)$. The γ factor increases with an increase in the resistance value of the defect.

From the RC model depicted in Fig. 13(b), the normalized delay increase ($\Delta D/D$) for a rising output transition of the NAND gate with an IRO defect is expressed as follows:

$$\frac{\Delta D}{D} = \frac{P\beta\gamma - k_p - \beta(P - k_p)}{k_p + \beta(P - k_p)} = \frac{\beta\gamma - Q - \beta(1 - Q)}{Q + \beta(1 - Q)} \tag{10}$$

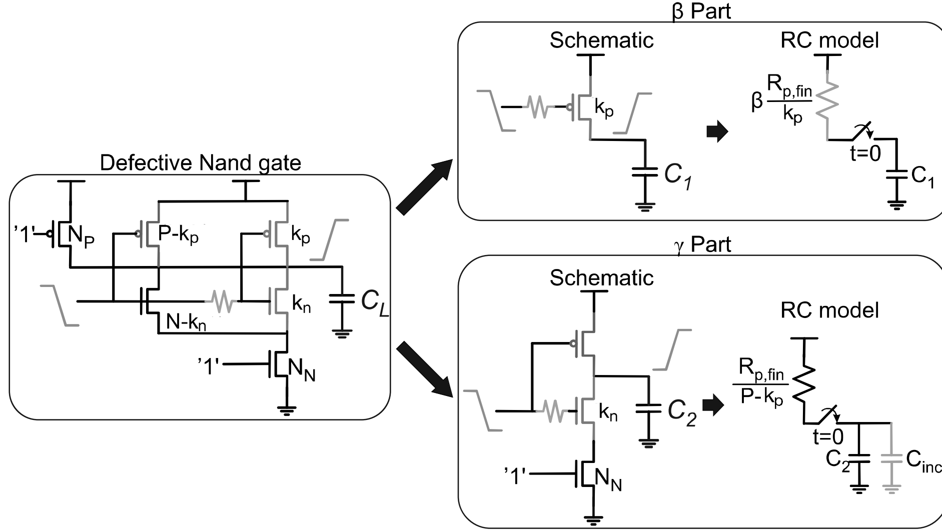

Fig. 14. RC models of the two-NAND gate to model β and γ parts for the IRO defect.

where $Q = k_p/P$ represents the ratio between the number of affected pMOS fins (k_p) and the total number of pMOS fins (P).

Estimation of the β and γ Factors: A simplified schematic of the two-NAND gate with an interconnect resistive open is depicted on the left side of Fig. 14. k_n and k_p denote the number of affected nMOS fins and pMOS fins due to the IRO defect, respectively. $N-k_n$ and $P-k_p$ represent the number of nonaffected nMOS fins and pMOS fins, respectively. To derive β and γ for (10), the two-NAND gate is partitioned into two parts.

The β part, depicted in the schematic on the upper right side of Fig. 14, accounts for the resistance of the defect, the affected k_P pMOS fins, and a portion of the load capacitance (C_1). In the RC model for the β part, the impact of the resistive open on the affected fins (k_P) is represented by an increase in the resistance $R_{p,\text{fin}}$ by a factor β. This approach mirrors the methodology employed for a resistive open at a SRO, as shown in Fig. 7.

The γ part, depicted in the schematic on the lower right side of Fig. 14, takes into account the resistive open defect, the k_n affected nMOS fins, the $P-k_p$ nonaffected pMOS fins, and a portion of the load capacitance (C_2).

It is worth noting that β can be obtained using the procedure proposed for the resistive open in a SRO, as the model for considering the impact of the resistive open on the affected pMOS fins remains the same for both IRO and SRO defects [see upper right side of Figs. 7(b) and 14].

To obtain the γ factor, we first compute the capacitance C_{inc} using the two circuits depicted in Fig. 15. In the first circuit, a resistive open with a fixed load capacitance C_2 is present [Fig. 15(a)]. In the simulation with SPICE, the delay of this defective circuit ($D_{2,\text{def}}$) is measured. Next, in the defect-free circuit [Fig. 15(b)], we vary the value of the capacitance C_2' until the delay of the defect-free circuit (D_2') matches $D_{2,\text{def}}$. Therefore, we compute $C_{\text{inc}} = C_2' - C_2$. Finally, the γ factor is computed as $\gamma = (C_L + C_{\text{inc}}/C_L)$.

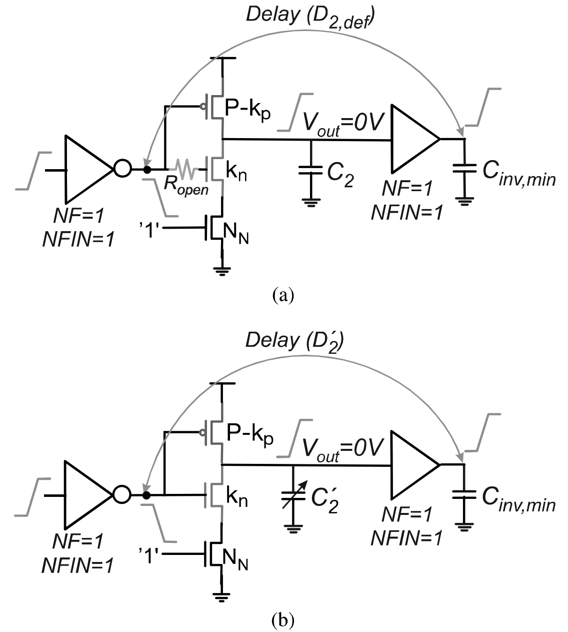

Fig. 15. SPICE characterizing circuit to compute γ. (a) With defect and C_2 constant. (b) Defect free and C_2 variable.

Indeed, since both the β and γ circuit parts belong to the same circuit, both circuit parts and their respective RC models must exhibit the same delay. This requirement ensures that the overall delay of the circuit remains consistent across all components, which is defined in the following equation:

$$\ln(2)\frac{\beta R_{p,\text{fin}} C_1}{k_p} = \ln(2)\frac{R_{p,\text{fin}}(C_2 + C_{\text{inc}})}{P - k_p} \tag{11}$$

The following expression can be obtained from (11):

$$C_2 + C_{\text{inc}} = \frac{(P - k_p)\beta}{k_p} C_1 \tag{12}$$

Noting that $C_L = C_1 + C_2$, we can replace $\gamma C_L = C_1 + C_2 + C_{\text{inc}}$ in (11) to obtain the following equations:

$$C_1 = \frac{\gamma k_p}{\beta(P - k_p) + k_p} C_L \quad (13)$$

$$C_2 = \frac{\beta(P - k_p)}{\beta(P - k_p) + k_p} C_L. \quad (14)$$

Solving for β in the left term of (11), an equation for the β factor is obtained

$$\beta = \frac{D k_p}{\ln(2) R_{p,\text{fin}} C_1}. \quad (15)$$

Using $\gamma C_L = C_1 + C_2 + C_{\text{inc}}$ in the right term of (11) and solving for γ in the right term of (11), an equation for γ is obtained

$$\gamma = \frac{D(P - k_p)}{\ln(2) R_{p,\text{fin}} C_L} + \frac{C_1}{C_L}. \quad (16)$$

An iterative process, similar to the one used in Fig. 10, is employed to determine the final values of β and γ for a given resistive open. Initially, the values of C_1 and C_2 are computed as $C_1 = (P - k_p)C_L/P$ and $C_2 = k_p C_L/P$ (see Fig. 14). Subsequently, β is determined using the circuit shown in Fig. 9 and (8) with a capacitance C_1. γ is obtained using the characterizing circuit illustrated in Fig. 15. The obtained values of β and γ are then utilized to compute new values of C_1 and C_2, which in turn are employed to calculate new values of β and γ. This iterative process continues until the values of C_1 and C_2 computed with the obtained β and γ from the simulation are smaller than a certain threshold ϵ compared to the previous values.

Similar to the resistive open in a SRO, a difference exists between the input gate capacitance of the characterizing circuits and the actual affected fins. To account for this difference, a correction factor (f_c) is employed

$$f_c = 2\frac{C_{\text{trans}}}{C_{\text{def}}} \quad (17)$$

where C_{trans} represents the input capacitance of the FinFET transistor of the characterizing circuit, while C_{def} denotes the input capacitance of the IRO defect being considered.

Fig. 16 compares the delay increase obtained from SPICE simulations with that derived using the proposed modeling strategy. The delay increase is depicted for defect locations A and B (see Fig. 13), corresponding to $Q = 6/8$ and $Q = 2/8$, respectively. It can be observed that the curve generated by (10) has a good agreement with the results obtained from SPICE simulations.

V. Analytical Models for Resistive Opens Under Process Variations

This section presents an analytical model incorporating process variations for logic gates affected by resistive open defects. Two distinct types of device parameter variations are examined. First, pure random variations are considered, where a device's parameter fluctuation is entirely independent of variations in all other devices within the cell. Second, correlated variations are considered, wherein a device's parameter fluctuation is correlated with the variation of the same parameter in all other devices within the cell. A correlation of one between devices within the same logic cell is assumed, given their proximity. Work-function variations (WFVs) in the metal gate for independent device variations (σ_{Φ_M}) and gate-length variations for correlated device variations (σ_{L_g}) are considered. For illustrative purposes of the correctness of our analytical models, this work uses a value of $\sigma_{\Phi_M} = 30$ mV for both pMOS and nMOS fin devices and a value of $\sigma_{L_g} = 0.46$ nm for both pMOS and nMOS transistors is used.

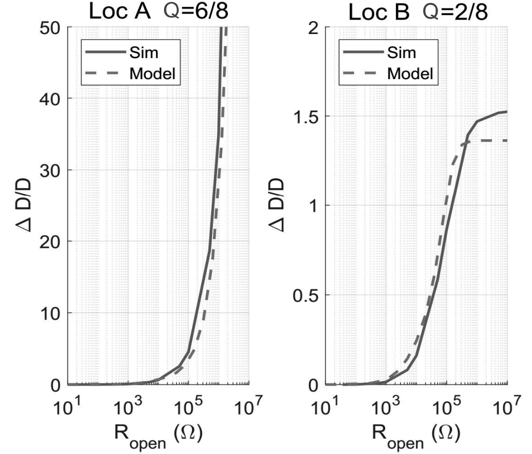

Fig. 16. Analytical model versus SPICE simulation for the normalized delay increase due to IRO defects.

The SPICE parameter used to account for WFVs is *PHIG*, which represents the gate work function and is included in advanced SPICE models [21]. *PHIG* directly impacts the threshold voltage and subthreshold swing by influencing the potential at the gate [25].

A. Analytical Delay Under Process Variations for a Defect-Free Inverter

The analysis focuses on the rising delay of an inverter logic gate, but the methodologies can be readily extended to encompass the falling delay and various other logic gate configurations. Fig. 17 presents an RC model that accounts for process variations targeting a rising output transition. Initially, the impact of process variations is determined only for the parallel resistances in the RC model depicted in Fig. 17. Subsequently, these findings are leveraged to derive the delay under process variations for the entire RC model, effectively characterizing the rising delay of the inverter. Let Y denote a random variable with a normal distribution with $E[Y] = \mu_Y$ and $\text{Var}[Y] = \sigma_Y^2$. Utilizing this random variable Y, a form $f(Y)$ function can be analyzed for its mean and variance, as outlined by Benaroya et al. [26]

$$E[f(Y)] \approx f(\mu_Y) \quad (18)$$

$$\text{Var}[f(Y)] \approx (f'(E[f(Y)]))^2 \text{Var}[Y]. \quad (19)$$

The conductance function for a single fin can be expressed as $f(Y) = 1/R_{p,\text{fin}}$. Subsequently, the conductance of P parallel fin resistances can be represented as follows:

$$f(Y) = P/R_{p,\text{fin}}. \quad (20)$$

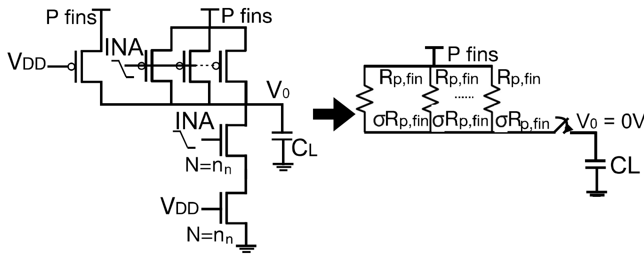

Fig. 17. *RC* modeling of process variations.

Applying (18) to (20), the mean of P equivalent resistances in parallel (μ_{R_T}) is given as

$$\mu_{R_T} = R_{p,\text{fin}}/P. \tag{21}$$

Applying (19) to (20) for independent variations and then taking the square root of the resulting term, the standard deviation of P equivalent resistances in parallel for independent variations is given as

$$\sigma_{R_T} = \sigma_{R_{p,\text{fin}}}/P^{3/2}. \tag{22}$$

Applying (19) to (20) for correlated variations and then taking the square root of the resulting term, the standard deviation of P equivalent resistances in parallel for correlated variations is given as

$$\sigma_{R_T} = \sigma_{R_{p,\text{fin}}}/P. \tag{23}$$

The expression for the rise delay for the RC model has been provided in (1). The delay standard deviation of the defect-free RC model (see Fig. 17) under independent variations, denoted as $\sigma_{D_{\text{DFi}}}$ can be obtained by multiplying the terms ln(2) and C_L from (1) with (22)

$$\sigma_{D_{\text{DFi}}} = \ln(2)\left(\frac{\sigma_{R_{p,\text{fin}}}}{P^{3/2}}\right)C_L. \tag{24}$$

Similarly, the delay standard deviation of the defect-free RC model (see Fig. 17) under correlated variations, denoted as $\sigma_{D_{\text{DFc}}}$ can be obtained by multiplying the terms ln(2) and C_L from (1) with (23)

$$\sigma_{D_{\text{DFc}}} = \ln(2)\left(\frac{\sigma_{R_{p,\text{fin}}}}{P}\right)C_L. \tag{25}$$

It must be noted that the P value represents the resistance of the entire defect-free parallel RC network. Thus, the P value can also be expressed with the following equation:

$$P = \frac{R_{p,\text{fin}}}{R_T} \tag{26}$$

where R_T represents the total resistance of P resistances in parallel.

B. Analytical Delay Under Process Variations for an Inverter With an Open Defect

The resistance of the entire RC network with a resistive open depends on the type of resistive open defect (e.g., RODS, SRO, and IRO) and the number of fins affected by the open. Because of this, expressions representing the resistance of the defective parallel RC networks (P_{def}) are developed for each type of resistive open. Subsequently, the delay standard deviation for a type of resistive open can be obtained by substituting P_{def} instead of P into (24) for independent variations and into (25) for correlated variations.

An expression for P_{def} for the RC model with a RODS defect can be obtained by calculating the total resistance (R_T) from Fig. 5(b) and utilizing (26)

$$P_{\text{def}} = \frac{PR_{p,\text{fin}} + Pk_pR_{\text{open}} - k_p^2R_{\text{open}}}{k_pR_{\text{open}} + R_{p,\text{fin}}}. \tag{27}$$

It is important to note that SRO and IRO defects share the same RC model in the pMOS network, as depicted in Figs. 7 and 13. An expression for P_{def} for the RC model with SRO or IRO defects can be derived by calculating the total resistance (R_T) from Figs. 7 and 13, and subsequently utilizing (26)

$$P_{\text{def}} = \frac{\beta(P - k_p) + k_p}{\beta}. \tag{28}$$

The normalized increment of the delay standard deviation is given by

$$\frac{\Delta\sigma_D}{\sigma_D} = \frac{\sigma_{D_{\text{def}}} - \sigma_{D_{\text{DF}}}}{\sigma_{D_{\text{DF,gate}}}} \tag{29}$$

where $\sigma_{D_{\text{DF}}}$ represents the defect-free delay standard deviation of the circuit, $\sigma_{D_{\text{def}}}$ represents the delay standard deviation of the circuit with the defect, and $\sigma_{D_{\text{DF,gate}}}$ represents the defect-free delay standard deviation of the gate under test.

Taking into account that P is used for the defect-free RC model and P_{def}, which depends on the type of resistive open defect, is used for the defective RC model in (24), and utilizing (29), the normalized increment of the delay standard deviation for independent variations is given by

RODS & SRO independent
$$\frac{\Delta\sigma_D}{\sigma_D} = \left(\frac{P}{P_{\text{def}}}\right)^{3/2} - 1 \tag{30}$$

IRO independent
$$\frac{\Delta\sigma_D}{\sigma_D} = \gamma\left(\frac{P}{P_{\text{def}}}\right)^{3/2} - 1. \tag{31}$$

It must be noted that the RC model of the IRO defect depends on the γ factor that multiplies the load capacitance [see Fig. 13(b)].

Taking into account that P is used for the defect-free RC model and P_{def}, which depends on the type of resistive open defect, is used for the defective RC model in (25), and utilizing (29), the normalized increment of the delay standard deviation for correlated variations is given by

RODS & SRO correlated
$$\frac{\Delta\sigma_D}{\sigma_D} = \frac{P}{P_{\text{def}}} - 1 \tag{32}$$

IRO correlated
$$\frac{\Delta\sigma_D}{\sigma_D} = \gamma\frac{P}{P_{\text{def}}} - 1. \tag{33}$$

Figs. 18–20 depict the $\Delta\sigma_D/\sigma_D$ results of the analytic model (dashed lines) compared to the simulation results (solid lines) for different RO defect locations under independent (WFV) and correlated (L_g) variations. Overall, the analytic model demonstrates a good approximation against the simulation results. However, its accuracy reduces for higher R_{open} values. Nevertheless, precision in the delay standard deviation becomes less critical for resistive opens with elevated

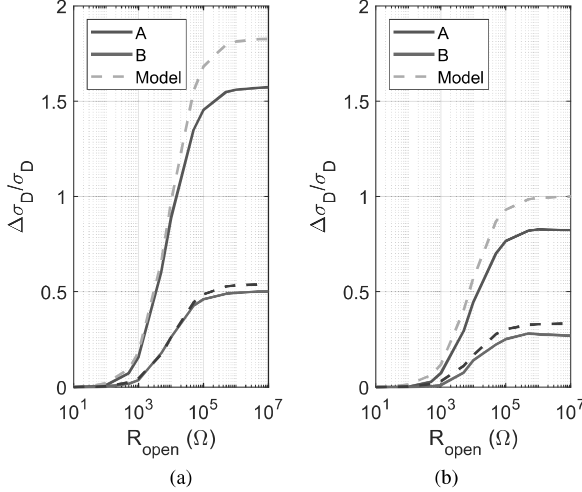

Fig. 18. Analytic model versus simulation of the normalized delay increase under process variations for a DSRO defect. (a) WFV. (b) L_g variations.

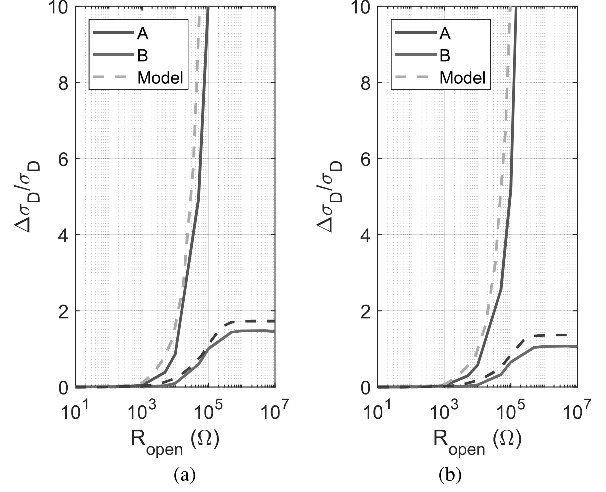

Fig. 20. Analytic model versus simulation of the normalized delay increase under process variations for a IRO defect. (a) WFV. (b) L_g variations.

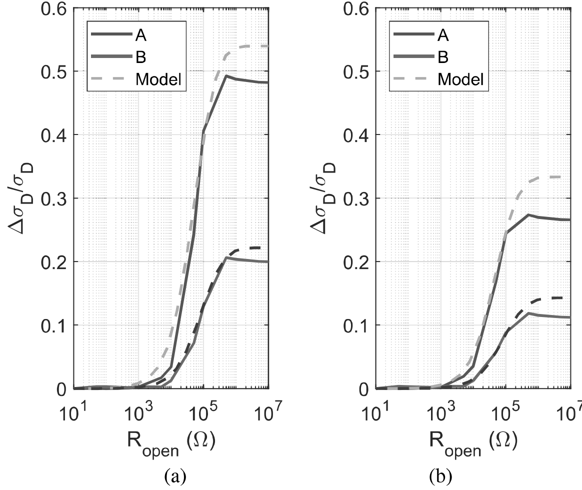

Fig. 19. Analytic model versus simulation of the normalized delay increase under process variations for a SRO defect. (a) WFV. (b) L_g Variations.

resistance values, as they typically exhibit higher mean delay values.

VI. Precharacterization Cost of the Proposed Analytical Models and Average Relative Error

A. Precharacterization Cost

A precharacterization step is necessary to apply the proposed models. The resistances of both pMOS and nMOS fins are determined using SPICE electrical simulations. These resistance values are then applied to the three types of resistive opens.

The β factor is critical for analyzing SRO defects and is derived from a set of quantized values for resistive open ($\#R_{\text{op}}$) and load capacitance ($\#C_L$). Fig. 21 illustrates a hypothetical Table containing the required data for β. For each load capacitance value, an iterative process is needed to determine the β value (see Fig. 11), with an average of five iterations (five SPICE electrical simulations) required. Consequently, the total number of SPICE simulations needed is given by ($\#R_{\text{op}} \times \#C_L \times 5$). The Table is generated for both rising and falling output transitions. It is important to note that a simple characterizing circuit (see Fig. 9) is used for SPICE simulations, so the computational time required for these simulations should not be a major concern.

Both β and γ factors must be determined for the IRO defect. Tables akin to that shown in Fig. 21 are produced for both rising and falling output transitions, displaying the β and γ values across quantized resistive open and load capacitance values.

To compute each entry in the table (i.e., the β and γ factors), one SPICE simulation of the defect-free circuit and several simulations of the defective circuit (an average of four simulations) are required. Subsequently, the final values for each entry (β and γ) are obtained through an iterative process (five simulations) similar to that used for determining the β factor for SRO defects. Thus, the total number of SPICE simulations needed for each entry is $(1 + 4) \times 5 = 25$. The computational cost for one table is therefore ($\#R_{\text{op}} \times \#C_L \times 25$). The table is generated for both rising and falling output transitions. It is important to note that simple characterizing circuits (see Figs. 9 and 15) are used for SPICE simulations, so the computational time required for these simulations should not be a major concern.

The gate delay for each gate in the library is characterized through SPICE electrical simulations for both rising and falling output transitions, evaluated across a range of quantized load capacitances. The delay standard deviation for each gate is determined using SPICE Monte Carlo simulations (500 runs), also performed across the range of quantized load capacitances.

The primary computational cost of our approach is related to determining the β and γ factors. Gate delay data for a library is typically available in advanced technologies, though standard delay deviations may be less common. The computational cost of characterizing both the gate delay and standard delay deviation is also briefly addressed below. It should be noted

R_{open}	Load Capacitance			
	C_{L1}	C_{L2}	...	C_{Ln}
val_1	$Beta_1$	$Beta_2$	...	$Beta_n$
val_2			...	
⋮				
val_n			...	

Fig. 21. β characterization data.

that the computational effort required for SPICE simulations to obtain the β factor for SRO defects, and the β and γ factors for IRO defects, should not be a major concern, as small precharacterizing circuits are used. In contrast, obtaining gate delays and delay standard deviations for an entire library across a range of load capacitances is more time-consuming. However, performing Monte Carlo simulations to evaluate large combinational circuits would be computationally prohibitive. Importantly, these simulations are performed only once and enable the assessment of resistive open defects in any general combinational circuit.

The range of load capacitances and resistive open values used for precharacterization to obtain the β and γ factors depends on the specific technology. As previously mentioned, small, low-computation circuits are simulated with SPICE, allowing for a wide, quantized range of load capacitances and resistive open values to be considered. Based on the results shown in Figs. 6, 12, and 16, an appropriate range for resistive open values is between 100 Ω and 10^6 Ω

B. Average Relative Error

The average relative error between the simulation and the proposed analytical model for the studied defect locations has been obtained. For RODS defects (see Fig. 6), the average relative errors are 10.8% and 7.7% for locations A and B, respectively. For SRO defects (see Fig. 12), the average relative errors are 12.2% and 9.2% for locations A and B, respectively. For IRO defects (see Fig. 16), the average relative errors are 8.8% and 12.3% for locations A and B, respectively.

VII. Outline of Potential Applications of the Proposed Models

This section delineates two potential applications of the developed analytical models. Initially, we deploy the proposed analytical models for fault simulation of resistive opens. Subsequently, we use them to identify critical paths affected by negative bias temperature instability (NBTI) and resistive opens.

A. Fault Simulation of Resistive Opens

The proposed analytical models extend fault simulation techniques targeting resistive opens [10], making them applicable to modern FinFET technologies. These models can be integrated into fault simulation frameworks that analytically compute the additional delays caused by defects [9], [27].

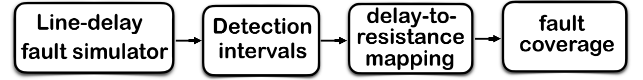

Fig. 22. Simplified flow for fault simulation of resistive opens. Adapted from [10].

A potential application of the proposed models is their use in a fault simulation engine for mapping delay to open resistance values. Fig. 22 illustrates a simplified workflow of the method, as proposed in [10]. First, a line-delay fault simulation based on signal descriptors is performed for each fault. Then, for each fault, the detection interval (in the time domain) is calculated, which encompasses the defect sizes (δ). Next, these delay fault sizes are translated into corresponding resistive open values. Finally, realistic fault coverage is achieved by considering the resistance intervals associated with the open defects. Using our proposed analytical models, delay fault sizes are mapped to an interval of resistive open values for each type of resistive open defect encountered in FinFETs. The process begins by computing the delay increase (ΔD) caused by a resistive open. Based on this delay increase, the value of the resistive open defect (R_{op}) is determined. As a result, the detection interval within the resistance domain is established [10].

For instance, considering the additional delay (δ) caused by an open defect of a given size, the expression to compute the delay increase due to a RODSs [see (3)] can be rearranged as follows:

$$\delta = \Delta D = \frac{Q}{1 + R_{p,\text{fin}}/k_p R_{\text{open}} - Q}.D. \tag{34}$$

The previous expression can be utilized to determine the detectable resistive open interval for a given set of defect sizes. A similar approach can be applied to the other models proposed in this work. For SRO and IRO defects, the β and γ values are translated into corresponding resistive open values.

B. Selection of Critical Paths Under NBTI and a Resistive Open

The proposed analytical models find utility in selecting critical paths in the presence of both NBTI [28] and resistive open in an error prediction framework. The gate delay under NBTI and a resistive open can be calculated as

$$D_{\text{gate}} = D_n + D_P + D_{\text{NBTI}} + D_{R\text{op}} \tag{35}$$

where D_{gate} is the final gate delay, D_n is the nominal gate delay, D_P is the gate delay under process variations, D_{NBTI} is the gate delay increase due to BTI, and $D_{R\text{op}}$ if the delay increase due to the resistive open.

The proposed analytical models in this work can be used to calculate the gate delay under a resistive open $D_{R\text{op}}$.

A simplified workflow for critical path selection under NBTI [28] and resistive open defects is shown in Fig. 23. First, the gate delays across the entire library are characterized, and a subset of critical logic paths is identified using static timing analysis (STA). Next, the NBTI-induced threshold voltage shift is calculated, and the proposed statistical models are

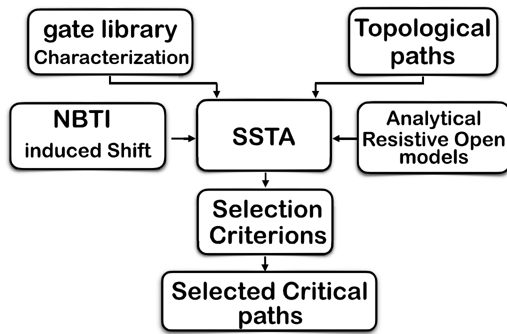

Fig. 23. Simplified flow for selection of critical paths under NBTI and resistive opens. Adapted from [28].

applied to compute the statistical delay response of the critical paths using statistical STA (SSTA). The result is a set of critical paths sensitive to both NBTI and resistive open defects, which can be used for reliable NBTI aging-delay monitoring.

VIII. Conclusion

This study introduces novel analytical models to assess the delay increase in FinFET-based circuits due to resistive open defects, offering a compact and cost-effective solution. These models encompass three types of resistive opens encountered in FinFET-based logic cells using multifin and multifinger structures, including those affecting drain/source regions, SROs, and both nMOS and pMOS transistor gates within multifin and multifinger structures. Moreover, cost-effective, compact analytical models have been developed to evaluate the delay increase, considering the influence of independent and correlated process variations. Notably, these models leverage precharacterized circuit libraries, requiring minimal precharacterization effort, particularly concerning process variations. The proposed models have been validated with SPICE electrical simulations, and a good agreement is observed between the proposed analytical models and SPICE. Importantly, these models offer a practical means to evaluate the detectability of resistive open defects, thus mitigating the cost associated with addressing varying defect sizes. Potential applications of the developed analytical models have been delineated. Ultimately, this research contributes to enhancing electronic product quality, safety, and reliability.

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