Low-cost Testing of 2.4GHz Receiver on Standard Digital ATE: Practical Implementation

Thibault Vayssade, Kamilia Tahraoui, François Lefèvre, Laurent Latorre, Florence Azaïs

Low-cost Testing of 2.4GHz Receiver on Standard Digital ATE: Practical Implementation

T. Vayssade, *Member, IEEE*, K. Tahraoui, *Member, IEEE*, F. Lefèvre, L. Latorre, *Member, IEEE,* and F. Azaïs, *Member, IEEE*.

***Abstract*—In this paper, we present the implementation of a low-cost solution for the test of 2.4GHz receivers on a standard Automatic test Equipment (ATE). The approach relies on the use of a customized binary signal generated by a digital tester channel as the test stimulus. This binary signal is specifically defined such that it presents similar spectral characteristics in the frequency band of the Device Under Test (DUT) as a conventional analog test stimulus generated by an RF tester channel. Dedicated scripts are developed that permit (i) the selection of an appropriate sampling frequency for the digital channel to avoid spectral corruption in the DUT frequency band, and (ii) the automatic conversion of the I/Q data computed by the ATE in case of a conventional RF stimulus into a binary sequence to be stored in the vector memory of the digital tester channel. Experimental results are provided that validate the efficiency of the proposed solution, under different communication protocols (ZigBee and Bluetooth Low Energy) and signal strengths.**

***Index Terms*—RF test; test signal generation; digital ATE; receiver sensitivity test, Packet Error Rate (PER), Received Signal Strength Indicator (RSSI).**

I. Introduction

The testing of integrated circuits, at the end of the manufacturing process, has always been a challenge as it involves the thorough verification of every datasheet specification for every single die to be sold, and so is at odds with the batch fabrication paradigm. It therefore represents a significant part of the total manufacturing cost. This is especially true for analog and RF components that cannot be tested using long-established structural methods, based on fault modeling, commonly used with digital circuits. These analog parts are instead verified functionally, and their performance must be physically characterized using adequate stimuli and measurements. In the sensitive context of RF transceivers, communicating over the shared resource that is the air, the testing must comply with industrial standards such as IEEE 802.15.x for BLE and ZigBee technologies.

Besides, the market for wireless appliances is very competitive, with applications ranging from networking infrastructures to consumer products including mobile devices, and a myriad of connected objects (IoT) such as sensors. In this context, IC manufacturers are in strong demand for innovative solutions to reduce the test costs. The reason RF testing is especially expensive is twofold. First, this is intrinsic to the functional testing approach as above discussed. Second, it involves expensive RF instrumentation both to generate stimuli and to measure emitters characteristics. This study focuses on the latter, aiming at RF receivers and stimuli generation.

To reduce the testing costs, a number of works targeting the development of digital solutions can be found in the literature. Some of them focus on the complete transceiver [1-5] and among them loopback [1,2] is a very attractive solution. However, this solution imposes constraints of the device architecture, and for instance it cannot be implemented in products that share a common Phase-Locked-Loop (PLL) between the transmitter (Tx) and receiver (Rx) path. Other works focus specifically on the transmit chain [6-8] where the challenge is the analysis of the test response, or on the receive chain [9-16] where the challenge is the generation of the test stimulus. Regarding test stimulus generation, some solutions aim at generating analog test stimuli using digital resources [9,10], while others rely on the use of a binary signal as test stimulus for the receiver [11-16]. In case of using a binary signal as test stimulus, two approaches can be distinguished, namely (i) the generation of binary signals customized to determine RF performance parameters based on a model of the Device Under Test (DUT) [11,12], and (ii) the generation of binary signals customized to be representative of conventional RF test stimuli [13-16].

In this work, we focus on the generation of baseband binary signals customized to be representative of RF test stimuli that are conventionally used for receiver sensitivity testing. The work is based on the theoretical developments introduced in [14] for generating baseband binary signals representative of FM/PM test stimuli. The approach was then extended in [15,16] to the case of digital modulation formats such as Binary Phase-Shift Keying (BPSK) and Minimum-Shift Keying (MSK). However, validation was carried out only in a laboratory environment, without using an actual Automatic Test Equipment (ATE) nor an actual RF product (a Universal Software Radio Peripheral (USRP) was used as an emulation of the device under test). In this paper, we focus on the practical implementation of the proposed solution in the industrial production test floor. In particular, we extend our previous works in two main aspects:

- A dedicated processing algorithm is developed that facilitates the transition from a conventional test flow that uses an RF channel for the generation of the test stimulus to an alternative test flow that can be implemented using digital channels only.
- Experimental results obtained on an actual RF product are provided, with measurements performed on the receiver of a wireless microcontroller using either an RF or digital channel of an industrial ATE (Advantest V93000 ATE) in real practical conditions. Results are compared in terms of

Packet Error Rate (PER) as a function of the Received Signal Strength Indicator (RSSI).

The paper is organized as follows. The principle and the theoretical foundations of the proposed strategy are presented in Section II. Section III describes the DUT and the specifications of the required characteristics for the test stimuli. The practical aspects for the implementation of the proposed solution on an ATE are detailed in section IV and experimental results are presented in section V. Finally, Section VI concludes the paper.

II. Proposed Digital Solution

A. Principle

In order to reduce the testing costs, our approach is to use a binary sequence generated by a standard digital tester channel instead of the conventional modulated analog signal generated by an RF channel. Drastic reduction of the testing costs can be expected, given that there is typically a factor 50 between the cost of an RF channel and the cost of a standard digital channel. Furthermore, while there is only a limited number of RF channels available on an ATE, digital channels are usually available in quantity, offering the possibility of implementing multi-site testing to further lower the testing costs.

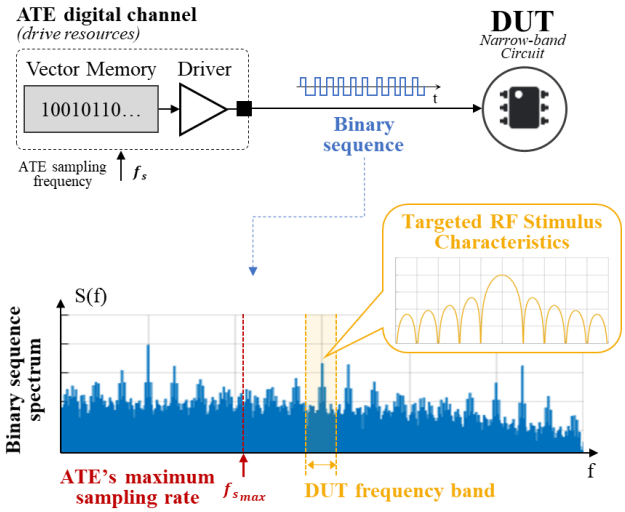


Fig.1. Principle of the proposed solution for digital generation of the test stimulus.

Obviously, a binary sequence is very different from a conventional modulated analog signal. However, an interesting point is that a digital sequence has a broadband spectrum, with frequency components that can extend well beyond the operating frequency of the ATE. Indeed, a binary sequence can be seen as the combination of multiple square-wave signals at different frequencies, where each individual square-wave signal has spectrum that exhibits harmonic components located at multiples of its fundamental frequency. This means that by exploiting these harmonic components, there is the possibility to excite a device that operates at a higher frequency than the ATE's operating frequency. This is of foremost importance because standard ATE digital channels have a limited sampling rate, typically $1.6GSps$, which means that the fundamental frequency of a square-wave signal that can be generated by these channels cannot exceed $800MHz$. This is a strong limitation, as it does not permit to address the $868MHz$, $915MHz$, and $2.4GHz$ ISM frequency bands, which are used by most RF communication devices. The exploitation of harmonic components permits to overcome this limitation.

However, it is not sufficient to excite the device in its operating frequency range. The excitation must also be carried out in accordance with the modulation scheme used by the product, i.e. with specific spectral characteristics. The major challenge is therefore to define the binary sequence in such a way that its spectral characteristics are similar to those of a conventional modulated analog signal in the frequency band of interest. Note that this compliance does not have to be ensured over the entire frequency spectrum, but only in the vicinity of the DUT operating frequency. Indeed, RF devices are narrow-band devices that generally include filters to eliminate out-of-band components. Alternatively, a filter centered on the DUT frequency band may be placed on the load board that provides the interface between the ATE and the DUT, if required. It should be underlined that this approach of exciting an RF device with a binary sequence is only valid in the context of production test, which is a controlled environment. Indeed, in a real-life application context, the broadband frequency components present in the binary sequence do not comply with the regulations for the use of RF devices.

In summary, the proposed approach is based on (i) exploiting the harmonic components contained in a binary sequence to overcome the limited sampling rate of ATE, and (ii) customizing the binary sequence so that it exhibits spectral characteristics similar to those of a conventional RF test stimulus in the DUT frequency band. This approach is illustrated in Figure 1.

B. Theoretical foundations

The theoretical foundations supporting the proposed strategy were first developed considering an elementary modulation scheme, i.e. single-tone frequency or phase modulation [13]. The analysis was then extended to the case of digital modulation formats, considering Binary Phase-Shift Keying (BPSK) and Minimum-Shift Keying (MSK) [14,15]. For the sake of comprehension, a brief summary is provided in this section.

The starting point for the definition of the binary sequence is to consider an angle-modulated analog signal defined by:

$$x(t) = A\,cos\big(\Omega(t)\big) = A\,cos(\omega_c t + \phi(t)) \quad (1)$$

where $\Omega(t)$ is the instantaneous phase of the modulated signal, A is the amplitude of the carrier signal, ω_c is the angular frequency of the carrier signal, and $\phi(t)$ is the instantaneous phase deviation. The modulation scheme determines how the instantaneous phase deviation $\phi(t)$varies.

The first step is to submit this signal to a zero-crossing operation. The resulting signal is a binary signal that can be expressed as an infinite sum of modulated analog signals:

$$y(t) = sgn[x(t)] = \frac{4}{\pi}\left(A\,cos\big(\Omega(t)\big) + \frac{A}{3}cos\big(3\Omega(t)\big) + \frac{A}{5}cos(5\Omega(t)) + \cdots\right) \quad (2)$$

where $\Omega(t)$ is the instantaneous phase of the original modulated analog signal and A is the amplitude of the binary signal. The first term corresponds to the baseband component of the binary signal while the following terms correspond to the harmonic replicas located at odd multiples of the baseband frequency.

Introducing $\Omega(t) = \omega_c t + \phi(t)$ in Eq.2, it comes:

$$y(t) = \frac{4}{\pi} \sum_i \frac{A}{i} cos(i\omega_c t + i\phi(t)) \quad for\ i = 1, 3, 5, \ldots \tag{3}$$

This equation is fundamental to the definition of the binary sequence. Indeed, it reveals that the binary signal resulting from a zero-crossing operation can be considered as an infinite sum of modulated analog signals, with a change in amplitude and instantaneous phase deviation for each individual one. In terms of spectral content, this means that the baseband spectrum has the same characteristics as the original analog signal, while each harmonic replica has different characteristics, the instantaneous phase deviation being multiplied by the harmonic replica order.

Going back to our objective to generate a test stimulus using a digital channel with specific spectral characteristics around a given carrier frequency $f_{c_{target}}$, Eq.3 permits to define three main rules:

- ***Rule 1:*** *choice of the order of the harmonic replica exploited as test stimulus*
  This choice is related to the sampling capabilities of the test equipment. Indeed, the baseband frequency of the binary signal derived from a zero-crossing operation of an analog signal should comply with the Nyquist criterion, which can be expressed by:
  $$i \geq 2f_{c_{target}}/f_{s_{max}} \tag{4}$$
  where i is the order of the harmonic replica and $f_{s_{max}}$ the maximum sampling rate of the ATE.
  Considering the loss in signal amplitude as i grows, the selected harmonic replica H_i corresponds to the smallest odd value of i that satisfies this equation.
- ***Rule 2:*** *setting of the baseband frequency* f_c
  The carrier frequency f_c of the analog signal that serves for the generation of the binary signal should be set as a submultiple of the targeted carrier frequency according to the order of the chosen harmonic replica:
  $$f_c = f_{c_{target}}/i \tag{5}$$
- ***Rule 3:*** *setting of modulation characteristics* $\phi(t)$
  In order to reach the desired spectral characteristics around $f_{c_{target}}$, the instantaneous phase deviation $\phi(t)$ of the analog signal that serves for the generation of the binary signal should be defined with:
  $$\phi(t) = \phi_{target}(t)/i \tag{6}$$
  where $\phi_{target}(t)$ is the instantaneous phase deviation corresponding to the targeted modulation format.

At this stage, we know how to calculate a binary signal containing the desired spectral characteristics from an analog modulated signal. However, due to the hardware architecture of an ATE, this signal cannot be exactly generated by a digital channel. Indeed, an ATE is a discrete-time system, which means that the electrical signal delivered on a digital channel is a binary signal whose transitions occur on a discrete-time grid determined by the ATE sampling frequency f_s. In other words, the actual binary signal generated by the ATE corresponds mathematically to a sampled-and-held version of the binary signal obtained after zero-crossing of the analog signal. This difference has two main consequences on the spectral characteristics: (i) the spectrum comprises not only the baseband spectrum and harmonic replicas but also images of these components due to the sampling process, and (ii) the amplitude of frequency components is shaped by the sin_c function due to the hold process.

The global shaping of the spectrum by the sin_c envelope is not a major issue; it just imposes to choose an ATE sampling frequency that is not too close to a submultiple of the targeted carrier frequency in order to avoid the local zeros. However, the presence of images is more problematic. Indeed, if these images fall within the DUT frequency band, they will corrupt the desired spectral characteristics. Since the location and amplitude of these images directly depends on the chosen value of the ATE sampling frequency f_s, a major challenge is to identify favorable sampling conditions, i.e. values of f_s that ensure that no image of significant magnitude fall within the frequency band of interest. To this end, a corruption estimator was defined in [14], which permits to evaluate how much the power contained in a given frequency band around the selected harmonic deviates from the power of an ideal square-wave:

$$Corr\ Est_i = \frac{\left|EBP_i - HCP_i^{expected}\right|}{HCP_i^{expected}} \tag{7}$$

where HCP stands for Harmonic Carrier Power and EBP for Enlarged Bandwidth Power. The computation of this estimator is based on an analytical expression of a sampled-and-held digital carrier; refer to [14] for more details.

In this work, we will use the corruption estimator to identify the most favorable sampling condition. Practically, the corruption score will be computed for all sampling frequencies compatible with the equipment's capabilities; the chosen ATE sampling frequency will be the one that obtains the minimum score.

III. Device Under Test (DUT)

The DUT is a low-power wireless micro-controller from NXP Semiconductors (KW47) intended for Automotive and industrial applications. As illustrated in Figure 2, it comprises a digital part that includes a CPU, memory and some peripherals as well as an RF transceiver operating in the 2.4GHz band. It supports two communication formats based on phase modulation, namely Zigbee (ZB) and Bluetooth Low Energy (BLE), with two possible data rates of $1MHz$ and $2MHz$ for BLE communication. For ZigBee communication, the phase modulation scheme is Offset Quadrature Phase Shift Keying (OQPSK) while for BLE communication, the phase modulation scheme is Gaussian Minimum Phase Shift Keying (GMSK). In both cases, these are narrow-band modulation schemes.

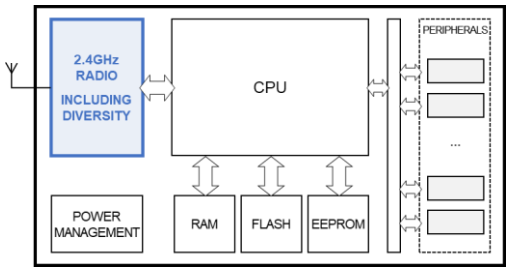


Fig.2. General architecture of the Device Under Test.

In this paper, we focus on the test of the RF module only, and more specifically on the test of the receiver (a digital solution has already been proposed for the test of the transmitter with validations in the production test environment [8]). Figure 3 shows the block diagram of the receiver architecture. It is a classical heterodyne architecture that uses frequency mixing to convert the received RF signal to an Intermediate Frequency (IF) where the signal is further processed to obtain baseband Rx data. These data are then transferred to digital processing core where additional operations are performed, such as error correction and Direct-Sequence Spread Spectrum (DSSS) decoding in case of ZigBee communication.

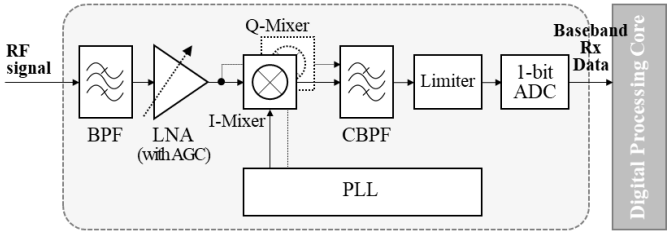


Fig.3. Block diagram of the DUT receiver architecture.

Note that a Low-Noise-Amplifier (LNA) with an Automatic Gain Control (AGC) stage is used before the down-conversion of the RF signal to IF. During normal operation, the AGC stage automatically adapts the LNA gain according to the received signal. However, it is common practice for test purpose to set the LNA gain to a fixed value, which can be achieved through the programming of control register of the AGC stage. This feature will be used in our experiments to verify the performance of the receiver under different LNA gain values.

Finally note that the device is also equipped with hardware resources that perform on-chip measurement of the Received Signal Strength Indicator ($RSSI$), with a resolution of $1dB$. This feature will be exploited in our experiments to evaluate the Packet Error Rate (PER) as a function of the $RSSI$ level.

IV. Practical Implementation on ATE

In this section, we detail the practical implementation of the three main steps that have to be accomplished for deployment of the proposed solution on an industrial ATE, which are (i) the choice of the harmonic replica that will be exploited for the generation of the binary sequence, (ii) the selection of the ATE sampling frequency that permits to avoid spectral pollution in the vicinity of the DUT frequency band, and (ii) the generation of a customized binary sequence that presents the desired spectral characteristics in the DUT frequency band according to the targeted modulation format.

A. Choice of the exploited harmonic replica

The first step consists in choosing the harmonic replica that will be exploited for the generation of the binary sequence. This choice depends, on the one hand, on the frequency of the targeted RF test stimulus and, on the other hand, on the capabilities of the test equipment. According to Rule 1 defined in section II, the minimum order of the harmonic replica that can be exploited is the smallest odd integer i that satisfies Eq.4.

For our case study, we target the generation of RF test stimuli at $f_{c_{target}} = 2.405GHz$ using a standard digital channel of the ATE V93000 (Pin Scale 1600), for which the maximum sampling frequency is $f_{s_{max}} = 1.6GHz$. With these inputs, the smallest odd integer that satisfies Eq.4 is $i = 5$, which means that the carrier frequency of the fundamental signal that serves for the generation of the stimuli will be set at $f_c = 481MHz$. This also imposes the minimum ATE sampling frequency in order to comply with the Nyquist criterion, i.e. $f_{s_{min}} = 962MHz$.

B. Selection of the ATE sampling frequency

The second step consists in selecting an ATE sampling frequency that permits to avoid spectral pollution in the DUT frequency band. This selection relies on the computation of the corruption estimator defined in Eq.7 for all possible f_s values between the Nyquist frequency and the maximum sampling frequency. The selected ATE sampling frequency is the one with the minimum score.

Note that because of the finite timing resolution of the ATE, there are only a discrete number of possible f_s values. More precisely, the sampling frequency is not a parameter that is directly specified in the ATE software, but it depends on the cycle duration (also called tester period) and the number of edges used within one cycle, both being user-defined parameters. On the ATE V93000, the minimum cycle duration is $5ns$, the maximum number of edges associated to a write event is 8, and the resolution for the setting of the tester period is $0.1ns$. To facilitate the implementation of the proposed solution, a script has been developed which automatically determines all possible f_s values for a given case study and perform the computation of the corruption estimator.

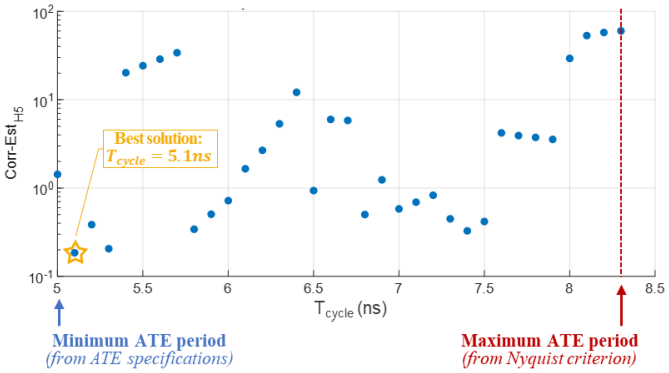


Fig.4. Corruption estimator computed for all possible tester period values.

For our case study, i.e. the generation of a test stimulus at $2.405GHz$ using the 5th harmonic replica, there are 34 possible

values for the tester period, ranging from the minimum cycle duration of $5ns$ ($f_s = 1.6GHz$) up to $8.3ns$ ($f_s = 963.9MHz$). Figure 4 shows the values of the corruption estimator computed for all these possible values, considering an arbitrary enlarged bandwidth of $20MHz$ corresponding to ten times a BLE channel width, around the targeted frequency of $2.405GHz$. The tester period value that leads to the lower score is $5.1ns$, corresponding to a sampling frequency $f_c \cong 1.568GHz$.

It should be pointed out that the evolution of the corruption score with respect to the sampling frequency does not exhibit monotonic behavior, and that it can radically differ between two possible consecutive values of the sampling frequency. This underlines the importance of the corruption estimator that permits to identify favorable sampling conditions despite this chaotic behavior.

C. Generation of the ATE binary sequence

The last step consists in defining the binary sequence to be stored in ATE vector memory, so that the electrical signal delivered by a digital channel has spectral characteristics corresponding to the chosen modulation format in the DUT frequency band. Theoretical foundations have established that this binary sequence can be obtained from zero-crossing and sampling operations applied to a virtual modulated analog signal, where the virtual analog signal is defined with a downscaling applied on both the carrier frequency and the instantaneous phase deviation, according to the order of the selected harmonic replica.

To facilitate implementation of the proposed solution, a script has been developed that automatically determines the content of the binary sequence from the baseband I/Q data that are normally supplied by the ATE to the RF channel, as illustrated in Figure 5.

In case of conventional RF test stimulus generation (see Figure 5.a), baseband I/Q data are computed in the numerical domain by the ATE processor according to the chosen modulation format, and supplied to the RF channel hardware. Here, they are converted to the analog domain by two DACs, filtered and applied to a quadrature modulator (implemented with a phase shifter, two mixers, and a signal combining stage) to get the RF modulated signal. The RF signal amplitude is then adjusted by an amplifier.

The processing algorithm developed to determine the content of the binary sequence comprises four main steps (see Figure 5.b):

- The first step consists in interpolating (resampling) the baseband I/Q data computed by the ATE processor at the sampling rate of the DACs included in the RF channel ($32MSps$ in our case) to the sampling frequency f_s selected for the operation of the digital channel.
- The second step is to extract the instantaneous phase deviation $\phi_{target}(kT_s)$ of the conventional RF test stimulus with:

$$\phi_{target}(kT_s) = atan\left(\frac{Q(kT_s)}{I(kT_s)}\right) \quad (8)$$

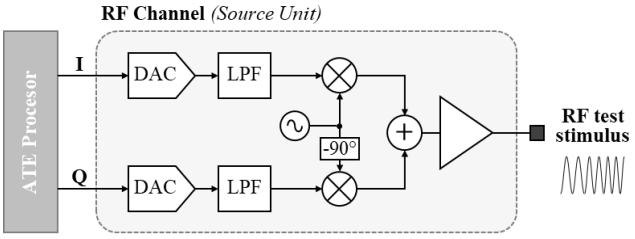
- The third step consists of calculating the virtual modulated analog signal with a downscaling applied on the carrier frequency and the instantaneous phase deviation, according to the order i of the selected harmonic replica:

$$x(kT_s) = sin\left(\frac{2\pi f_{c_{target}}}{i} kT_s + \frac{\phi_{target}(kT_s)}{i}\right) \quad (9)$$

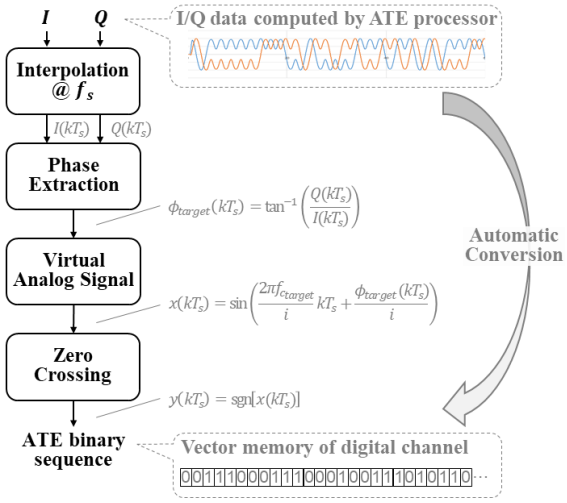
- The last step is to apply a zero-crossing operation on the virtual modulated analog signal:

$$y(kT_s) = sgn\,[x(kT_s)] \quad (10)$$

The resulting samples directly correspond to the binary sequence that has to be stored in the ATE vector memory. The amplitude of the signal delivered to the DUT will be adjusted by programming the V_{IL} and V_{IH} levels of the digital channel driver.



(a) Test stimulus generation with an RF channel



(b) Processing algorithm for automatic calculation of the binary sequence

Fig.5. Determintion of the content of the ATE binary sequence.

This script of automatic determination of the binary sequence was first validated in simulation. More precisely, an ideal digital signal was computed by applying a zero-order-hold operation on the binary sequence determined by the script; a FFT was then applied to obtain its spectrum. As an illustration, Figure 6 shows the global view of the spectrum of the simulated digital test stimulus in the ZigBee case. As expected, the global spectrum has a hairy aspect due to the presence of images created by the sampled-time generation process; the shaping by the sin_c function is also well visible. However, despite this spectral clutter, we expect the content around the selected harmonic replica to exhibit the desired characteristics, thanks to the appropriate choice of the sampling frequency f_s.

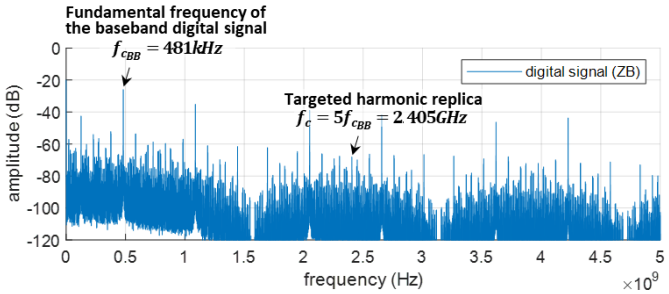
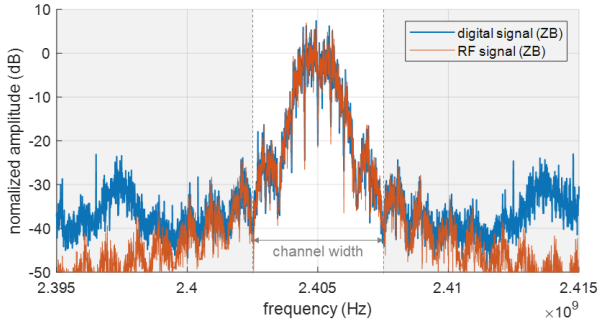
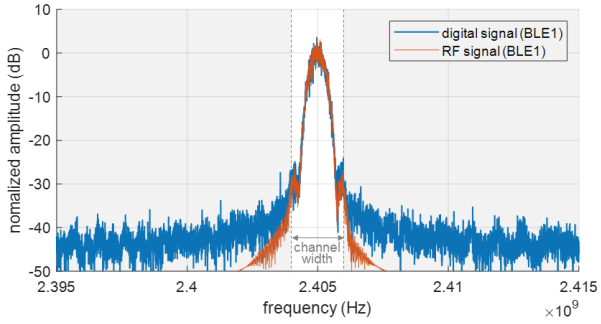


Fig.6. Illustration of the full spectrum of the simulated digital test stimulus (ZigBee case).

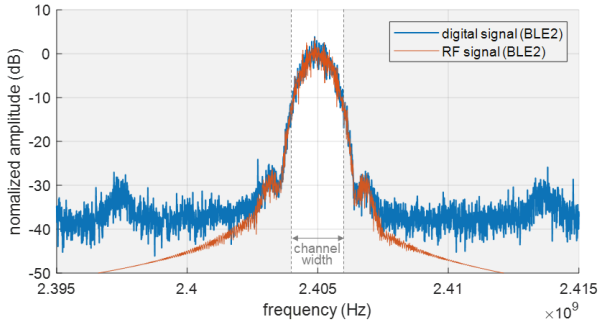
To illustrate this point, we have compared the spectrum of the simulated digital signal with that of the simulated conventional RF test signal. Results are illustrated in Figure 7 which gives a close-up view around the targeted carrier frequency of $2.405GHz$, for ZigBee and BLE modulation formats (with two different data rates of $2MHz$ and $1MHz$ for BLE). In all cases there is a good agreement between the spectrum of digital and RF signals within the channel width.



(a) ZigBee



(b) BLE 1MHz



(c) BLE 2MHz

Fig.7. Spectrum of simulated digital and RF test stimuli around $2.405GHz$.

V. Results

A. Experimental setup

To demonstrate the practical application of the proposed solution, measurements were carried out on an Advantest V93000® ATE equipped with standard digital tester channels (PinScale® 1600). The tester is also equipped with RF channels, enabling the digital solution to be compared with the conventional RF solution. The objective is to measure the evolution of the *PER* as a function of the *RSSI* level in order to evaluate the receiver sensitivity. This evaluation is carried out for different values of the LNA gain (programmed using the control register of the AGC stage).

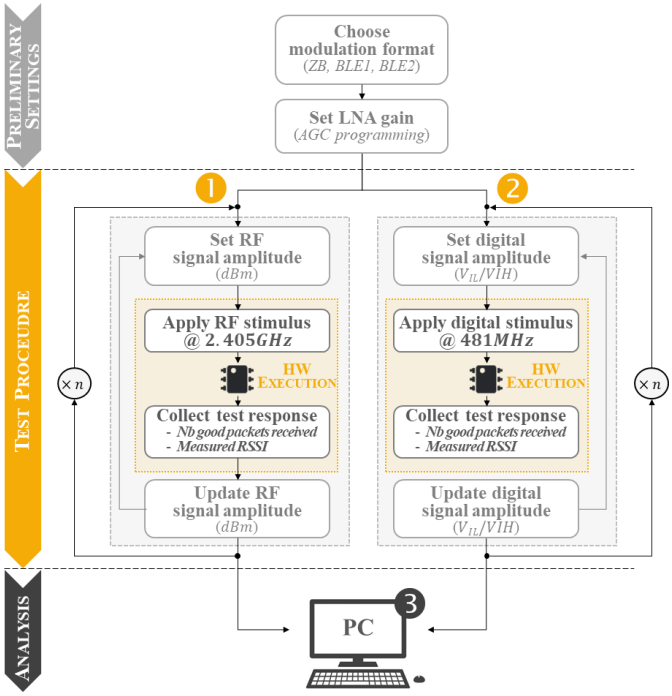


Fig.8. ATE measurement procedure.

The ATE measurement procedure is illustrated in Figure 8. It involves applying a test stimulus encoded according to the chosen communication protocol (ZB, $BLE1$ or $BLE2$) and recording the number of good packets received as well as the *RSSI* level, for different values of the test stimulus amplitude. The test stimulus is a sequence of 1,000 packets following the format defined in IEEE 802.15.1 and IEEE 802.15.4 for BLE and ZigBee communication respectively. It can be delivered either by an RF channel ($2.405GHz$ conventional modulated signal) or by a digital channel ($481MHz$ digital signal generated from the customized binary sequence). In the case of the conventional RF approach, the amplitude of the test stimulus is directly specified in dBm with a dedicated parameter in the tester software, while in the case of the digital signal, its amplitude is specified by programming the V_{IL} and V_{IH} levels of the digital channel driver. Note that neither the way amplitude is programed, nor its absolute value really matter as we use the RSSI metric in both cases, which somehow normalizes this parameter from the receiver perspective.

The test procedure, including the sweeping on the test stimulus amplitude is repeated a number of times in order to

evaluate measurement dispersion. Finally, all collected results are transferred to a PC for further analysis.

B. Preliminary experiment

A preliminary experiment was conducted with the DUT configured in ZigBee mode and the LNA gain value fixed to an intermediate level ($ACG5$). The measurement procedure was applied with 50 repetitions of the test stimulus amplitude sweep (both RF and digital test stimuli). Results are displayed in Figure 9, which reports the evolution of PER (percentage of erroneous packets received over the total number of applied packets) as a function of the measured $RSSI$ level for each individual test run, as well as the mean value over the 50 repetitions.

Several comments arise from these results. First, as expected, a perfect PER of 0% is obtained for the highest values of the signal strength ($RSSI$ above $-69dB$), but then degrades rapidly as the signal strength reduces, both when excited with the test stimulus generated by the RF test channel and the digital test channel. In both cases, a strong variability is observed. For instance, for an $RSSI$ level of $-72dB$, the PER measured when using the conventional RF test stimulus varies between 0.9% and 97.1% from one test run to another. Similarly, for the same $RSSI$ level of $-72dB$, the PER measured when using the digital test stimulus varies between 10.4% and 86.6% from one test run to another. Yet, looking at the mean over the 50 repetitions, there is at first glance a good agreement between the evolution of the PER measured when using the RF test stimulus and that measured when using the digital test stimulus.

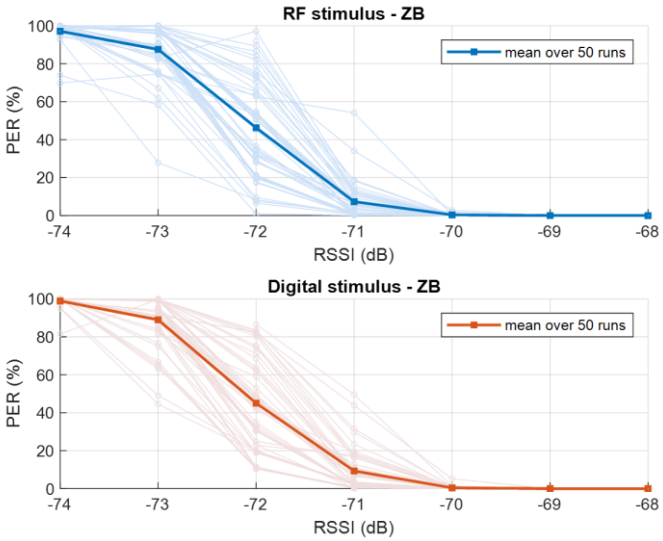


Fig. 9. PER vs. RSSI for 50 acquisitions using either RF or digital stimulus (ZB communication).

In order to have a quantitative evaluation of how the digital test solution performs compared to the conventional RF test solution, a sensitivity indicator $RSSI_{50\%}$ has been defined, which corresponds to the $RSSI$ level for a PER of 50%. Note that because the on-chip measurement of the $RSSI$ level exhibits a resolution of only $1dB$, the precise value of the indicator cannot be directly measured on the ATE. However, an estimate can be obtained by using a linear interpolation between the two measurements which give a PER value immediately below and above 50%, as illustrated in Figure 10. In the following, we will use this indicator to compare the performance of the digital solution with that of the conventional RF one.

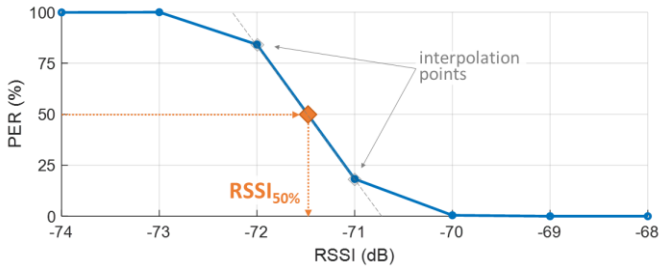


Fig. 10. Illustration of the calculation of the sensitivity indicator on one test run (i.e. one sweep on the test stimulus amplitude).

Figure 11 gives the distribution of the sensitivity indicator $RSSI_{50\%}$ computed on each of the 50 test runs using either the conventional RF test stimulus or the digital one. It can be observed that the distribution obtained using the digital test stimulus is well centered on the one obtained using the RF test stimulus and exhibits a similar Gaussian shape and width. Table I reports the detailed statistics in terms of mean value and standard deviation. These values confirm the excellent agreement between the digital test solution and the conventional RF one, with a difference of less than $0.01dB$ both in the mean value and standard deviation of the computed sensitivity indicator.

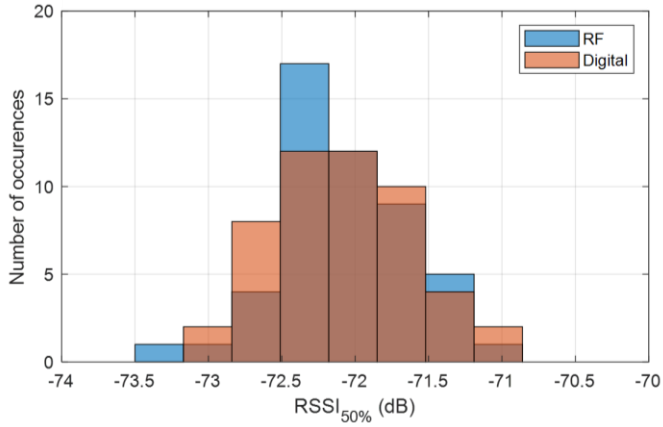


Fig. 11. Histogram of the sensitivity indicator $RSSI_{50\%}$ computed on 50 test runs using either RF or digital stimulus (ZB – AGC5).

TABLE I.
MEAN AND STANDARD DEVIATION OF $RSSI_{50\%}$ COMPUTED ON 50 TEST RUNS USING EITHER RF OR DIGITAL STIMULUS (ZB – AGC5)

Stimulus generation	$\mu(RSSI_{50\%})$	$\sigma(RSSI_{50\%})$
RF channel	$-72.083dB$	$0.460dB$
Digital channel	$-72.092dB$	$0.467dB$

C. Full experiment

The preliminary experiment has validated the efficiency of the proposed digital solution under one specific DUT operating condition, namely ZigBee communication and LNA gain value set to intermediate level ($AGC5$). The aim of this section is to validate the efficiency of the proposed solution over a wider

range of DUT operating conditions. More specifically, measurements were carried out with the device operating with the three communication protocols (ZB, $BLE1$ or $BLE2$) and three LNA gain values ($AGC4$, $AGC5$ and $AGC6$), i.e. a total of 9 conditions. For each condition, the test procedure was repeated 10 times, and the sensitivity indicator was computed for each repetition.

Results are shown graphically in Figure 12, which plots the mean $RSSI_{50\%}$ value computed over the 10 repetitions when using the digital test stimulus versus the one computed when using the conventional RF test stimulus. It can be observed that all points are well aligned on the ideal straight line, indicating that the proposed digital solution is indeed able to handle different communication formats and signal strength levels. Detailed numerical results are reported in Table 2. It can be observed that, whatever the communication format or the value of the LNA gain, the difference between the digital solution and the RF one remains below $0.04dB$.

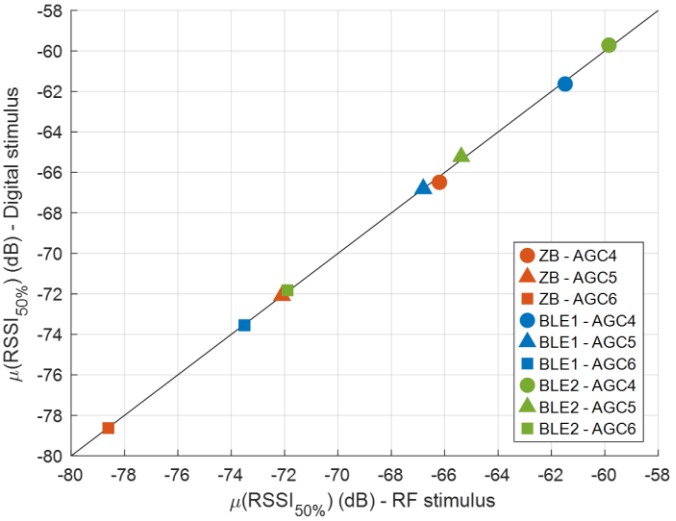


Fig. 12. $RSSI_{50\%}$ computed using digital test stimulus vs. $RSSI_{50\%}$ computed using conventional RF test stimulus for different device configurations (mean value over 10 test runs).

TABLE II.
RSSI$_{50\%}$ COMPUTED USING EITHER RF OR DIGITAL STIMULUS FOR DIFFERENT DEVICE CONFIGURATIONS (MEAN VALUE OVER 10 TEST RUNS)

		$RSSI$ @ $PER = 50\%$		Difference
		RF stimulus	Digital stimulus	
ZB	AGC4	$-66.30dB$	$-66.66dB$	$-0.36dB$
	AGC5	$-72.10dB$	$-72.09dB$	$0.01dB$
	AGC6	$-78.60dB$	$-78.63dB$	$-0.03dB$
BLE1	AGC4	$-61.49dB$	$-61.63dB$	$-0.15dB$
	AGC5	$-66.80dB$	$-66.89dB$	$-0.09dB$
	AGC6	$-73.50dB$	$-73.55dB$	$-0.05dB$
BLE2	AGC4	$-59.85dB$	$-59.71dB$	$0.13dB$
	AGC5	$-65.38dB$	$-65.23dB$	$0.15dB$
	AGC6	$-71.89dB$	$-71.82dB$	$0.07dB$

Finally, Figure 13 compares the measurement dispersion observed using either the digital test stimulus or the conventional RF test stimulus. It should be stressed that this is only a rough estimate of measurement dispersion, since the standard deviation is computed only over 10 repetitions. Still, the results reveal no significant difference between the digital and RF solutions. The evaluated standard deviation remains within the same range, with a higher dispersion for the digital solution in some cases and a higher dispersion for the RF solution in others.

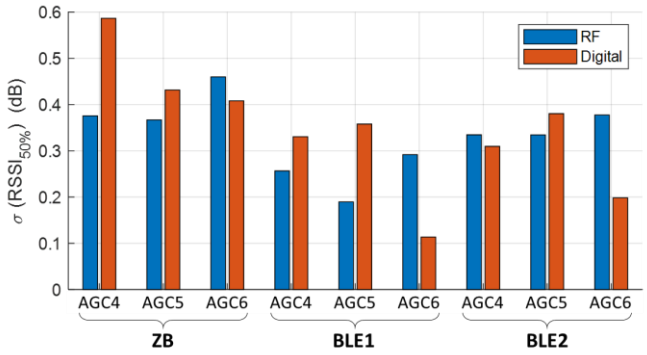


Fig. 13. Comparison of measurement dispersion using either RF or digital channel for test stimulus generation, for different device configurations (10 test runs).

VI. CONCLUSION

This paper describes an innovative approach for the generation of RF test stimuli. The idea is to replace expensive RF channels commonly found in ATEs with basic digital channels operating at lower frequencies, taking advantage of inherent harmonic replicas to "shape" the desired spectrum around the targeted RF carrier frequency. In this paper, the focus is given to practical implementation and experimental validation from an industrial perspective.

A methodology for defining the appropriate binary signal to be generated by a digital ATE channel was presented, supported with automation scripts that take into account practical limitations of ATE digital channels, such as maximum sampling rate and timing resolution.

Experimental results were also presented, obtained on an actual wireless microcontroller with BLE and ZigBee receiver capability. Validation consists in comparing the PER measured using either an RF or a digital channel of the V93000 ATE, as a function of the RSSI. Excellent agreement between both implementations was observed, making the digital approach a very good candidate for replacing the conventional RF testing solution.

Still, further investigations must be carried out. Indeed, results presented in this paper were obtained from a single DUT sample. The good match must be confirmed with a wider population of circuits, with supposedly working and failing samples to make sure that the final decision (sorting) remains the same with both test approaches. Furthermore, validation was only performed within a limited RSSI dynamic range. Additional experiments are required to fully assess the performance of the proposed solution over an extended dynamic range.

REFERENCES

[1] A. Valdes-Garcia, W. Khalil, B. Bakkaloglu, J. Silva-Martinez and E. Sanchez-Sinencio, "Built-in Self Test of RF Transceiver SoCs: from Signal Chain to RF Synthesizers," IEEE Radio Frequency Integrated Circuits (RFIC) Symp, pp. 335-338, 2007.

[2] J. J. Dabrowski and R. M. Ramzan, "Built-in Loopback Test for IC RF Transceivers," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 18, no. 6, pp. 933-946, June 2010.

[3] I. Kore, B. Schuffenhauer, F. Demmerle, F. Neugebauer, G. Pfahl and D. Rautmann, "Multi-site test of RF transceivers on low-cost digital ATE," IEEE International Test Conference (ITC), pp. 1-10 2011.

[4] C. -H. Peng et al., "A novel RF self test for a combo SoC on digital ATE with multi-site applications," IEEE International Test Conference (ITC), pp. 1-8, 2014.

[5] M. Ishida and K. Ichiyama, "An ATE System for Testing RF Digital Communication Devices With QAM Signal Interfaces," in IEEE Design & Test, vol. 33, no. 6, pp. 15-22, Dec. 2016.

[6] N. Pous, F. Azaïs, L. Latorre, and J. Rivoir, 2011. "A Level-Crossing Approach for the Analysis of RF Modulated Signals Using Only Digital Test Resources," in J. of Electronic Testing: Theory and App. (JETTA), vol. 27, no. 3, pp 289-303, 2011.

[7] S. David-Grignot, F. Azaïs, L. Latorre and F. Lefevre, "Low-cost phase noise testing of complex RF ICs using standard digital ATE," IEEE International Test Conference (ITC), pp. 1-9, 2014.

[8] T. Vayssade, F. Azaïs, L. Latorre and F. Lefèvre, "Low-Cost EVM Measurement of ZigBee Transmitters From 1-bit Undersampled Acquisition," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 40, no. 11, pp. 2400-2410, 2021.

[9] H. Malloug, M. J. Barragan, S. Mir, E. Simeu and H. Le-Gall, "Mostly-digital design of sinusoidal signal generators for mixed-signal BIST applications using harmonic cancellation," IEEE International Mixed-Signal Testing Workshop (IMSTW), pp. 1–6, 2016.

[10] S. David-Grignot, A. Lamlih, M. Moez Belhaj, V. Kerzérho, F. Azaïs, F. Soulier, P. Freitas, T. Rouyer, S. Bonhommeau, and S. Bernard, "On-chip "Generation of Sine-wave Summing Digital Signals: an Analytic Study Considering Implementation Constraints," in J. of Electronic Testing: Theory and App. (JETTA), vol. 34, no. 3, pp. 281–290, 2018.

[11] A. Banerjee, S. K. Devarakond, V. Natarajan, S. Sen and A. Chatterjee, "Optimized digital compatible pulse sequences for testing of RF front end modules," IEEE 16th International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW), pp. 1-6, 2010.

[12] M. A. Zeidan, G. Banerjee, R. Gharpurey and J. A. Abraham, "Phase-Aware Multitone Digital Signal Based Test for RF Receivers," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 9, pp. 2097-2110, Sept. 2012.

[13] T. Vayssade, M. Chehaitly, F. Azaïs, L. Latorre and F. Lefevre, "Exploration of a digital-based solution for the generation of 2.4GHz OQPSK test stimuli," IEEE European Test Symposium (ETS), pp. 1-6, 2021.

[14] K. Tahraoui, T. Vayssade, F. Lefèvre, L. Latorre, F. Azaïs, "Digital-based solution for the generation of FM/PM test stimuli", IEEE Trans. on Computer-Aided Design (TCAD), Vol. 44, No. 2, pp. 777-790, 2024.

[15] K. Tahraoui, R. Burelle, T. Vayssade, F. Lefèvre, L. Latorre, F. Azaïs, "Digital generation of RF phase-modulated test stimuli: application to BPSK modulation scheme", Proc. IEEE Defect and Fault Tolerance Symp. (DFT'24), pp. 1-6, 2024.

[16] K. Tahraoui, T. Vayssade, F. Lefèvre, L. Latorre, F. Azaïs, "Low-cost generation of RF test stimuli from baseband digital signals", Proc. IEEE Asian Test Symp. (ATS'24), pp. 1-6, 2024.

ACKNOWLEDGEMENTS

AI Disclosure Statement: no AI tools were used in the technical development of this work neither in the writing of this article.

T. Vayssade received M.S. and Ph.D. degrees in Electrical Engineering from the University of Montpellier, France, in 2017 and 2020 respectively.
From 2021 to 2023, he was an electronic engineer at ELA Innovation, France. He is now an associate professor at the University of Montpellier, France. His main research interests are RF testing and signal processing.

K. Tahraoui received the M.S. degree in Electrical Engineering from the University of Montpellier, France, in 2020.
She received the Ph.D. degree from the University of Montpellier in December 2024, for her work at LIRMM on the development of low-cost digital test solutions for RF devices.

F. Lefèvre received the Engineer's degree with radio-frequency option from the ENSERG engineering school of Grenoble, France, in 1994.
He is currently with NXP Semiconductors, Caen, France. He leads the Design for Test definition of large RF, mixed-signal and digital ICs activities, together with the industrial test development tasks.

L. Latorre received the M.S. degree in Mechanical and Electronic Engineering from the University of Montpellier, France, in 1995 and the Ph.D. degree in Electrical Engineering from the University of Montpellier, France, in 1999.
He is currently head of the Microelectronics department at LIRMM, Montpellier, France. His main research interests are low-power embedded systems, signal processing, test, and integrated front-end electronics for sensors.

F. Azaïs received the M.S. and Ph.D. degrees in Electrical Engineering from the University of Montpellier, France, in 1993 and 1996 respectively.
She is currently a CNRS researcher at LIRMM, Montpellier, France. Her main research interests are AMS/RF circuit testing, and reliability of integrated systems.