Contribution au test et à la fiabilité des systèmes sur puce

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HABILITATION A DIRIGER DES RECHERCHES

CONTRIBUTION AU TEST ET A LA FIABILITE DES SYSTEMES SUR PUCE

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Maître de Conférences

soutenue le devant le jury composé de :

M. Régis Leveugle	Professeur, TIMA/INPG	Examinateur
M. Jean-Michel Portal	Professeur, IM2NP/Université Aix-Marseille	Rapporteur
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AVANT PROPOS

Ce document présente la synthèse de mes travaux de recherche et d'enseignement effectués depuis septembre 1998, date à laquelle j'ai débuté ma thèse de doctorat. Les travaux de recherche ont été effectués au LIRMM (Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier) au sein du département de Microélectronique. Les activités d'enseignement ont été menées à la Faculté des sciences (ex UFR) / département EEA (Electronique, Electrotechnique et Automatique) de l'Université Montpellier 2 au niveau Licence et Master.

Ce document se compose de quatre parties :

- Partie 1 : Synthèse des Travaux

Cette première partie présente mon curriculum vitae, le résumé des thèmes de recherche, le bilan de ma production scientifique, mes responsabilités scientifiques, mes responsabilités administratives, ainsi que les contrats de recherche et les activités d'enseignements dans lesquels je suis impliqué.

- Partie 2 : Développement et Perspectives

Cette seconde partie, rédigée en anglais, a pour objectif de détailler mes thèmes de recherche et d'exposer mes perspectives pour les prochaines années.

- Partie 3 : Production scientifique

Cette partie présente la liste détaillée de mes publications de recherche.

- Partie 4 : Articles significatifs

Cette partie présente 5 articles majeurs convrant mes thématiques de recherche.

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PARTIE 1 : SYNTHESE DES TRAVAUX

Cette première partie présente mon curriculum vitae, le résumé des thèmes de recherche, le bilan de ma production scientifique, mes responsabilités scientifiques, mes responsabilités administratives, ainsi que les contrats de recherche et les activités d'enseignements dans lesquels je suis impliqué.

1 CURRICULUM VITAE

1.1 Etat Civil

Nom :	Virazel
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Date de naissance :	3 décembre 1974
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1.2 Cursus

1998 - 2001	Thèse de doctorat en Microélectronique soutenue le 14 novembre 2001 *LIRMM, Université Montpellier II*
1997 - 1998	Service Militaire – Scientifique du contingent *École d'Application de l'Aviation Légère de l'Armée de Terre*
1997	DEA Systèmes Automatiques et Microélectroniques – Mention Bien *LIRMM, Université Montpellier II*
1996	Maîtrise EEA – Mention Bien *Université Montpellier II.*
1995	Licence EEA – Mention ABien *Université Montpellier II.*
1994	DUT GEII *IUT de Montpellier*
1992	Baccalauréat série F2 Electronique – Mention Bien *Lycée Jean Mermoz, Montpellier.*

1.3 Parcours Professionnel

Depuis 11/2003	Maître de Conférences Titulaire – Section CNU 61 Enseignement : Faculté des Sciences / EEA, Université Montpellier II Recherche : Département Microélectronique du LIRMM *Titulaire de la PES rang A (depuis 2010)* *Titulaire de la PEDR (de 2006 à 2010)*

11/03 - 11/04	Maître de Conférences Stagiaire – Section CNU 61 Enseignement : Faculté des Sciences / EEA, Université Montpellier II Recherche : Département Microélectronique du LIRMM
09/02 - 10/03	Stage Post-Doctoral Responsables : Patrick Girard et Serge Pravossoudovitch LIRMM, Université Montpellier II
11/01 - 07/02	Stage Post-Doctoral Responsable : Hans-Joachim Wunderlich Université de Stuttgart, Allemagne

2 ACTIVITES DE RECHERCHE

2.1 Contexte

Mes activités de recherche s'inscrivent dans les thèmes portés par le département Microélectronique du Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM). Le département Microélectronique du LIRMM est spécialisé dans la recherche de solutions innovantes pour modéliser, concevoir et tester les circuits et systèmes intégrés complexes. Ses champs de compétences lui permettent de mener des activités de recherche sur les aspects suivants : le développement de nouvelles générations d'architectures de processeurs pour des applications comme la téléphonie 4G ou le multimédia ; la conception en vue du test, et le test de circuits et systèmes intégrés, qui regroupe toutes les activités de modélisation, de détection, et de diagnostic de défaillances physiques ; la conception, l'intégration et le test de microsystèmes à base de capteurs et d'actionneurs ; la sécurité numérique pour la confidentialité et l'intégrité des communications; la conception de circuits pour le domaine de la santé, avec des applications comme la neurostimulation pour les systèmes implantés dans le corps humain. Pour mener à bien ses activités, le département s'appuie sur un effectif d'une centaine de personnes, parmi lesquelles des chercheurs, enseignants-chercheurs, doctorants, post-doctorants, ingénieurs et techniciens. Ses nombreuses coopérations académiques, son implication dans de nombreux projets nationaux (ANR, FCE) et internationaux (FP7, ENIAC et CATRENE), sa participation et son aide à la création d'entreprises, et ses activités de transfert et de valorisation vers le secteur industriel, en font un acteur incontournable dans le paysage de la recherche scientifique française et européenne en Microélectronique.

J'ai intégré le département Microélectronique du LIRMM comme doctorant en septembre 1998. Au cours de ma thèse de doctorat, ma thématique de recherche s'est orientée vers le test des pannes temporelles. Dans ce cadre, j'ai plus particulièrement étudié les propriétés des séquences de test ainsi que leurs capacités à détecter les pannes temporelles.

Après avoir soutenu ma thèse de doctorat en novembre 2001, j'ai effectué un stage post-doctoral dans l'équipe du Professeur Hans-Joachim Wunderlich à l'Université de Stuttgart. J'ai ensuite réintégré le département Microélectronique du LIRMM en tant que Maître de Conférences et je suis depuis rattaché à une équipe de recherche constituée de 5 personnes : 3 enseignants chercheurs (Serge Pravossoudovitch - PR, Alberto Bosio – MCF, Arnaud Virazel – MCF) et 2 chercheurs (Patrick Girard – DR CNRS, Luigi Dilillo – CR CNRS). Le Tableau 1.1 présente l'organigramme de l'équipe TRAFIC (« Test and Reliability of Advanced and Future ICs ») en terme d'organisation des thèmes de recherche traités.

TABLEAU 1.1 ORGANIGRAMME DE L'ÉQUIPE TRAFIC

Responsables du groupe :

Patrick GIRARD *DR CNRS* Responsable du département Microélectronique (2010 à 2013) Directeur adjoint du GdR SoC-SiP	**Serge PRAVOSSOUDOVITCH** *Professeur* Directeur de l'école Polytech Montpellier

Membres non-HDR :

Alberto BOSIO *Maître Conférence* Recruté en 09/2007	**Luigi DILILLO** *CR CNRS* Recruté en 09/2007	**Aida TODRI** *CR CNRS* 09/2011 à 05/2014	**Arnaud VIRAZEL** *Maître Conférence* Recruté en 09/2003	**Thèmes de Recherche portés par le groupe**
X		X	X	*Test de Pannes Temporelles*
X	X		X	*Test Faible Consommation*
X	X		X	*Test des Mémoires SRAM*
			X	*Test des Mémoires Non-Volatiles (FLASH et MRAM)*
	X		X	*Tolérance aux Fautes*
X				*Diagnostic Logique*
		X		*Test des Circuits 3D*

2.2 Résumé des Thèmes de Recherche

Les sous-sections suivantes présentent un résumé des thèmes de recherche menés dans l'équipe. Le détail des thèmes de recherche pricipaux que j'ai menés et que je mène actuellement est donné dans la deuxième partie de ce rapport.

2.2.1 Test de Pannes Temporelles

Le test de pannes temporelles permet de vérifier le fonctionnement d'un circuit ou système à sa fréquence maximum. Certaines caractéristiques, telles que par exemple le nombre de commutations, permettent de qualifier les séquences de vecteurs par rapport aux pannes temporelles. Il est ainsi possible de prévoir à priori (sans passer par la simulation de pannes) si un vecteur peut être un "bon" vecteur (vecteur couvrant beaucoup de pannes) ou un "mauvais" vecteur (vecteur couvrant peu de pannes). A partir de ces informations, le but était de déterminer comment générer une séquence de vecteurs couvrant au mieux les pannes temporelles et ceci, de manière la plus indépendante possible de la structure du circuit considéré. En effet, l'objectif n'était pas de développer un nouvel algorithme ou une nouvelle structure de génération déterministe de vecteurs de test, mais plutôt d'explorer une approche de type aléatoire pondérée, l'idée étant de guider la génération aléatoire des vecteurs par des heuristiques prenant en compte les spécificités des conditions de détection des pannes temporelles.

Dans ce cadre, l'objectif de mes travaux de thèse était le développement de générateurs intégrés de séquences de vecteurs adjacents. De façon générale, les générateurs intégrés produisent des séquences où les vecteurs successifs diffèrent de plusieurs bits (séquences MIC pour « Multiple Input Change »). Or, il apparaît que dans le cadre du test des pannes temporelles, les séquences de vecteurs adjacents ou SIC pour « Single Input Change » sont particulièrement intéressantes. En effet, d'une part, il a été démontré qu'elles sont suffisantes pour détecter toutes les pannes temporelles détectables de façon robuste et d'autre part, qu'en réduisant les commutations multiples dans le circuit, elles assurent un meilleur taux de couverture « robuste ». La première partie de ma thèse a porté sur l'évaluation des capacités de détection de pannes des séquences SIC sur divers modèles de pannes (pannes temporelles mais également collages et court-circuit). Nous avons ainsi, d'une part mis en évidence l'intérêt de telles séquences par rapport aux séquences MIC et d'autre part, montré l'influence du caractère aléatoire des séquences de vecteurs de test sur la capacité de détection de ces séquences SIC. La suite de ces travaux a été consacrée au développement de structures matérielles de génération de vecteurs SIC ayant de « bonnes » propriétés aléatoires. Ce travail qui a été réalisé dans le cadre du projet européen « MEDEA » et en collaboration avec Monsieur René David du Laboratoire d'Automatique de Grenoble a constitué l'essentiel de mes travaux de thèse soutenue le 14 novembre 2001.

Après plusieurs années d'arrêt, nous avons relancé cette thématique avec deux thèses qui sont actuellement en cours et pour lesquelles je suis l'encadrant principal. La thèse d'A. Assokan (débutée en septembre 2012) menée dans le cadre du projet européen « ELESIS » qui aborde la problématique de génération de vecteurs de test pour les fautes de délais en prenant en compte la conception du circuit (*i.e.* prise en compte des coulages capacitifs), mais aussi les phénomènes de bruit sur l'alimentation et la masse (« Vdd-bounce » et « ground-bounce »). La thèse de D. Patel (débutée en juillet 2013) dans le cadre d'une convention CIFRE avec la société ST-Microelectronics basée à Crolles aborde plus particulièrement le test de délai des circuits prototypes.

2.2.2 Test Faible Consommation

Ces travaux portent sur la prise en compte des problèmes de consommation de puissance et/ou d'énergie pendant la phase de test des circuits intégrés digitaux. Le but est de développer des méthodes et outils permettant de réduire l'activité totale du circuit en mode test. Lors du test du circuit, l'activité du circuit étant généralement largement supérieure à l'activité générée lors du fonctionnement normal, le problème soulevé par la consommation et la dissipation de la puissance s'avère être un problème

crucial. Des études spécifiques ont effectivement montré que la puissance dissipée est deux à trois fois plus élevée lors de l'application du test que lors du fonctionnement normal. En plus des problèmes liés à l'encapsulation et au refroidissement du circuit, cette surconsommation peut entrainer de sérieux problèmes de fiabilité pouvant même parfois mener à la destruction du circuit. Dans le cadre du test intégré, un problème supplémentaire intervient. L'augmentation de la consommation d'énergie due au test intégré réduit l'autonomie des appareils portables. Par exemple, les procédures de test déclenchées à la mise sous tension des téléphones cellulaires peuvent, si l'on n'y prend garde, conduire à une consommation importante.

L'objectif est de développer des méthodes et outils permettant de réduire l'activité totale du circuit en mode test sachant qu'en technologie CMOS, la consommation est étroitement liée à l'activité dans le circuit et que l'activité dans le circuit en mode test est généralement largement supérieure à l'activité générée lors du fonctionnement normal du circuit notamment lorsque le circuit est muni de chaines de scan. Les opérations de chargement et déchargement de données de test dans les chaînes de scan engendrent une suractivité de commutation induisant une consommation excessive de puissance pouvant avoir des conséquences néfastes sur le circuit telles qu'une baisse de sa fiabilité ou sa destruction pure et simple.

Ce thème de recherche a fait l'objet de la thèse de N. Baderredine (soutenue le 15 septembre 2006), dont j'ai été l'encadrant principal, avec une focalisation particulière sur l'optimisation de la puissance instantanée. Dans le cadre de cette thèse nous nous sommes intéressés à la réduction de la consommation de puissance de pic pendant les phases de capture du processus de test par scan. Dans la mesure où ces captures sont généralement réalisées à vitesse élevée, une puissance de pic excessive au cours de l'une de ces phases peut conduire à des phénomènes parasites (« ground bounce », « IR-drop ») qui peuvent changer l'état logique de certains nœuds et conduire au marquage fautif du circuit testé. Afin de minimiser la puissance de pic pendant les cycles de test nous avons proposé deux approches : i) une basée sur le ré-ordonnancement de la chaîne de scan et ii) une consistant en une assignation particulière des valeurs non justifiées par l'ATPG. Une réduction moyenne de plus de 50% a été obtenue sur la puissance de pic dans le cycle de test. Cette thèse a été menée dans le cadre du projet européen « NanoTEST ».

Notre activité sur cette thématique « Test faible consommation » s'est poursuivie dans le cadre de la thèse de F. Wu (soutenue le 12 octobre 2011) et du projet européen TOETS. L'objectif était ici de considérer les problèmes de consommation des schémas d'horloge LOS (« Launch-Of-Shift ») et LOC (« Launch-Of-Capture ») utilisés pour le test par scan des pannes temporelles.

Cette thématique se poursuit actuellement par deux travaux de thèse. La thèse de M. Valka (débutée en janvier 2011) dans le cadre d'une convention CIFRE avec la société ST-Ericsson basée à Grenoble porte plus particulièrement sur le test des circuits dit faible consommation, *i.e.* embarquant des modules permettant de contrôler leurs consommations de puissance. La thèse d'A. Noccua (débutée en septembre 2013) dans le cadre du projet « HiCool » sur la modélisation de la consommation de puissance.

2.2.3 Test de Mémoires Volatiles et Non-Volatiles

Les mémoires représentent la grande majorité de la surface occupée par les systèmes sur puce (SoC pour « System-on-Chip ») et ce phénomène tend encore à s'amplifier. Compte tenu de l'importance de ces dispositifs mais également des caractéristiques technologiques propres à leur réalisation (limites technologiques), il est reconnu que les mémoires concentrent la plupart des défauts dans un SoC. Le test des mémoires est donc aujourd'hui un sujet de recherche particulièrement d'actualité. Dans le cadre de cette thématique, notre équipe de recherche cible trois technologies mémoires : SRAM, Flash et MRAM.

2.2.3.1 Test des Mémoires SRAM

Les solutions utilisées pour tester les mémoires sont particulières dans le sens où elles sont intimement liées à l'architecture, et aux influences spécifiques des défauts induits par le procédé de fabrication de la mémoire. Les algorithmes de test de mémoire permettent par exemple de tester, outre les défauts classiques de type collage, des modèles de défauts tels que l'interdépendance entre les cellules mémoire adjacentes. Il reste cependant un certain nombre de défauts qui sont très mal pris en compte par les algorithmes actuels, notamment les défauts introduisant un dysfonctionnement temporel. En effet, certains défauts induisent un comportement spécifique en se manifestant par exemple par une erreur uniquement après la $n^{ème}$ lecture consécutive d'une même cellule mémoire réalisée à la fréquence nominale de fonctionnement.

L'objectif de cette thématique de recherche est d'étudier ce type de comportement à caractère temporel ou dynamique induit par ces défauts particuliers, et de développer des solutions méthodologiques et algorithmiques permettant de mettre en évidence ces défauts lorsqu'ils affectent une mémoire (SRAM). Ce travail, mené en collaboration avec la société Infineon basée à Sophia Antipolis a constitué l'essentiel des travaux de thèse, pour lesquelles j'ai été l'encadrant principal, de L. Dilillo soutenue le 8 juin 2005 et d'A. Ney soutenue le 29 septembre 2008. Il s'est poursuivi dans le cadre de la thèse de R. Alvez Fonseca (soutenue le 21 juillet 2011) en se focalisant sur les aspects variabilités des processus de fabrication des SRAM. Ces thèses ont fait partie de projets européens (« ASSOCIATE », « NANOTEST » et « TOETS ») et d'une convention de recherche directe avec la société Infineon basée à Sophia Antipolis.

Cette thématique de recherche s'est poursuivie dans le cadre d'une convention de recherche avec la société INTEL Mobile Communications (ex Infineon) en ciblant tout particulièrement les mémoires SRAM faible consommation. La problématique abordée consiste à vérifier l'impact de défauts pouvant affecter les modules permettant de contrôler l'alimentation des différents blocs constituant la mémoire. Ces travaux ont fait partie de la thèse de L. Zordan soutenue en décembre 2013.

Un nouveau volet de la thématique « Test des Mémoires SRAM » a débuté en septembre 2011 avec la thèse de G. Tsiligiannis. Cette thèse aborde la problématique de l'impact des effets transitoires dus aux radiations sur les SRAM. Ces travaux ont pour objectif de montrer comment le test peut jouer un rôle majeur pour la détection de ces événements transitoires.

2.2.3.2 Test des Mémoires Flash

Si de nombreux travaux concernant le test des mémoires du type SRAM ont été publiés, peu de contributions sur le test des mémoires de type Flash sont disponibles à ce jour dans la littérature. Il faut dire que contrairement à d'autres types de mémoire, il n'y a pas de standard officiel bien établi dans ce domaine, de nombreux industriels disposant de technologies propriétaires. Dans le cadre de son programme de recherche et développement sur les mémoires Flash embarquées ou empilées dans les systèmes complexes de type SOC ou SIP (carte à puce, ASIC dédié, microcontrôleur 32 bits etc.), l'objectif d'ATMEL est d'intégrer de plus en plus de mémoire Flash sur des technologies avancées (90 nm et moins). Dans ce contexte, l'optimisation du test des mémoires Flash revêt une importance tout à fait stratégique, la qualité finale des produits livrés et le rendement en production dépendant très largement de la qualité du test.

Le point majeur de nos travaux a consisté au développement de modèles mémoire représentant le comportement réel de la Flash et permettant de mener des analyses de défauts de fabrication. Cette étude permet de disposer d'une meilleure compréhension et d'une synthèse des mécanismes de défaillance clés dans les mémoires Flash. Ceci permet d'orienter le test en vue d'obtenir le meilleur taux de couverture, et d'avoir une estimation de ce dernier. Ceci est impératif dans l'optique d'une approche qualité sérieuse avec des clients stratégiques, comme dans le domaine de l'automobile par exemple.

Ces travaux, menés en collaboration avec la société ATMEL basée à Rousset, ont constitué l'essentiel des travaux de thèse, dont j'ai été l'encadrant principal, d'O. Ginez soutenue le 24 novembre 2007 et portant sur les architectures NOR (architecture parallèle). Cette thématique s'est

poursuivie dans cadre de la thèse, dont j'ai été l'encadrant principal, de P.-D. Mauroux (soutenue le 9 décembre 2011) sur les architectures de types NAND (architecture série).

2.2.3.3 Test des Mémoires MRAM

Bien qu'encore très utilisée pour sa non-volatilité, la mémoire Flash présente de nombreux inconvénients tels que l'utilisation d'une haute tension pour la programmation de grille flottante, la rétention et le vieillissement de l'oxyde tunnel. La technologie MRAM pour « Magnetic Random Access Memory » est une des technologies mémoire émergeante présentant des performances élevées, une faible consommation et une grande densité d'intégration tout en étant entièrement compatible avec le processus CMOS.

Dans une MRAM, le stockage de la donnée est assuré par une jonction magnétique appelée MTJ (pour « Magnetic Tunnel Junction »). Une MTJ est généralement constituée de deux couches ferromagnétiques avec une couche fixe (*i.e.* ayant un champ orienté fixe) et une couche dite libre (i.e. pour laquelle le champ pet changer de direction). Les deux situations de champ sont donc la situation parallèle et antiparallèle. Dans la situation parallèle, la MTJ présente une résistance minimum (*Rmin*) et dans la situation antiparallèle la résistance est maximum (*Rmax*). Cet écart de résistance est suffisamment élevé pour être mesuré par un amplificateur de lecture. L'écriture (*i.e.* le changement de l'orientation du champ dans la couche libre) peut être réalisée de différentes manières en fonction de la technologie utilisée.

Cette étude, menée en collaboration avec la société CROCUS Technology basée à Grenoble dans le cadre du projet ANR (EMYR « Enhancement of MRAM Memory Yield and Reliability »), a constitué l'essentiel des travaux de thèse, dont j'ai été l'encadrant principal, de J. Azevedo soutenue en octobre 2013. Dans cette thèse, nous avons abordé la problématique test des mémoires MRAM en focalisant l'étude sur les défauts pouvant affecter la MTJ ainsi que la périphérie mémoire.

2.2.4 Tolérance aux Fautes

Les technologies nanométriques permettent d'envisager la réalisation de structures numériques de taille considérable regroupant plusieurs centaines de millions et bientôt milliards de transistors sur une puce. La solution aux problèmes relatifs à la conception de tels circuits constitue naturellement un des challenges importants à résoudre dans les années à venir. De la même façon, les aspects associés au test de ces circuits représentent un défi de plus en plus important.

Les technologies nanométriques actuelles et à venir, malgré les avantages mentionnés précédemment et relatifs à la miniaturisation, comportent inévitablement un certain nombre d'inconvénients que les technologues et les concepteurs s'attachent à minimiser, soit dans les processus de fabrication, soit dans les techniques de conception. Deux phénomènes déjà considérés dans les technologies submicroniques vont avoir des répercutions de plus en plus importantes dans les années à venir : i) la susceptibilité des circuits aux agressions externes voire internes telles que les particules alpha, les radiations cosmiques, les rayonnements électromagnétiques pouvant induire des fonctionnements intermittents parfois non prévisibles, ii) la variabilité du processus technologique conduisant lors de la conception à des paramètres physiques de plus en plus distribués. Pour palier les effets négatifs de tels phénomènes des actions seront prises tant au niveau du processus technologique qu'au niveau des méthodologies de conception.

Une réponse naturelle pour ne pas dire évidente à ces problèmes est de doter les circuits de redondances permettant de les rendre plus tolérants aux défaillances causées par des défauts de fabrication, des déviations technologiques ou des agressions externes. Le test de ces circuits pose alors des problèmes particuliers dus aux redondances, et donc par définition à la non testabilité de certaines pannes. L'étude du test des structures redondantes de type TMR (pour « Triple Modular Redondancy ») constitue l'essentiel des travaux de thèse, dont j'ai été l'encadrant principal, de J. Vial soutenue le 16 décembre 2009.

Cette thématique s'est poursuivie par les travaux de thèse, dont j'ai été l'encadrant principal, de D. A. Tran (soutenue en décembre 2012) en collaboration avec le Professeur Hans-Joachim Wundelrich de l'Université de Stuttgart. Ces travaux ont porté principalement sur le développement d'une structure de tolérance aux fautes capables de tolérer les erreurs permanentes et transitoires. Cette approche dite hybride utilise différents types de redondances et permet d'augmenter la robustesse des circuits intégrés digitaux.

Nous poursuivons actuellement le développement de cette structure dans le cadre d'architecture de processeur pipeline. Ces travaux font partie intégrante du sujet de thèse d'I. Wali débutée en mars 2012, en collaboration avec l'école Polytechnique de Turin (dans le cadre du « LIA LAFISI – CNRS ») et pour laquelle j'assure la direction de thèse (procédure spécifique de l'école doctorale I2S autorisant une co-direction de thèse sans HDR).

2.2.5 Diagnostic Logique

Les défaillances technologiques qui sont mises en évidence lors du test des circuits intégrés se traduisent par un dysfonctionnement du circuit dans certaines configurations. Certains défauts perturbent le fonctionnement du circuit quelle que soit la fréquence d'application des stimuli appliqués sur ses entrées, mais d'autres n'affectent le comportement du circuit qu'à partir d'une certaine fréquence de fonctionnement. Nous sommes alors en présence de pannes temporelles, appelées aussi pannes de délai. Le test de ce type de pannes devient d'autant plus important que dans les technologies submicroniques, les effets relatifs de ces pannes (retards de commutation par rapport à la fréquence de fonctionnement du circuit) sont bien plus importants que dans les technologies microniques.

L'objectif de ce projet est de développer une méthode de diagnostic permettant de prendre en compte divers modèles de pannes. La première approche développée dans le cadre de la thèse d'A. Rousset est basée sur un principe d'analyse « Effet à Cause ». Le principe d'analyse « Effet à Cause » qui met en œuvre un processus de traçage de chemins critiques a initialement été développé pour identifier des pannes de collages. Or, compte tenu des évolutions technologiques et des stratégies agressives de synchronisation, il est apparu que de plus en plus de défaillances induisaient des comportements à caractère temporel ou paramétrique mal représentés par le modèle de collage. Ce principe a donc été adapté au traitement d'autres types de pannes telles que pannes de délai ou pannes de court-circuit mais, toutes les méthodes développées jusqu'à présent sur ce principe ne ciblent qu'un seul modèle de panne, éventuellement deux lorsque les effets induits sont comparables. Or, lorsqu'une erreur est observée lors du test, rien ne permet d'identifier à priori le modèle de panne représentant le comportement induit par la défaillance, et par conséquent de définir la méthode de diagnostic à appliquer.

Cette étude nous a conduit à développer une méthode de diagnostic unifiée permettant de considérer simultanément l'ensemble des modèles de fautes généralement utilisés pour modéliser les divers comportements que peuvent engendrer les défaillances. Elle a constitué l'essentiel des travaux de thèse d'A. Rousset soutenue le 1er avril 2008. Cette thèse a été menée dans le cadre du projet européen « NanoTEST ».

Cette étude s'est poursuivie par une collaboration avec la société ST-Microelectronics basée à Crolles. L'objectif était d'adapter les concepts développés précédemment aux caractéristiques des circuits ST-Microelctronics. Ces circuits n'étant pas tous conçus dans un contexte Scan complet, une approche complémentaire basée sur un principe d'analyse « Cause à Effet » a été étudiée. Cette approche met en œuvre un dictionnaire de fautes de collage fourni par un outil de simulation de fautes classiques et une source de données représentant l'activité du circuit en présence des vecteurs fautifs. Cette source de données est fournie par une simulation symbolique du circuit sain. A partir de ces données, i.e. dictionnaire de collage et activité du circuit, le processus de diagnostic réalisé permet de localiser les sites de défaillances potentielles en précisant le modèle de panne associé. Cette étude constitue l'essentiel des travaux de thèse d'Y. Benabboud soutenue le 30 avril 2010. Elle s'est poursuivie dans cadre de la thèse de Z. Sun soutenue le 16 mai 2014 avec comme objectif le

diagnostic au niveau transistor en collaboration avec la société ST-Microelectronics basée à Grenoble. Cette activité se poursuit actuellement dans le cadre de la thèse d'A. Touati (soutenance prévue en 2016).

2.2.6 Test des Circuits 3D

L'intégration 3D est une technologie émergeante qui devra permettre de poursuivre la loi de Moore, et donc le développement des prochains nœuds technologiques CMOS. L'intégration 3D est basée sur l'utilisation de Tsvp (pour « Through-Silicon-Vias ») permettant la conception de circuits intégrés multi-niveaux offrant de hautes performances, de fortes densités d'intégrations avec un grand nombre de fonctionnalités. Cependant, un des avantages majeurs de l'intégration 3D, la densité d'intégration, représente aussi un des plus grands challenges de la conception car chaque niveau de l'empilement peut présenter une forte consommation de puissance, ainsi qu'un fort gradient de température. De plus, l'adoption de la technologie 3D est encore handicapée par la non connaissance des mécanismes de défaillances spécifiques qu'elle implique, les problèmes du test, mais aussi par le manque de solutions de conception en vue du test.

Les étapes de fabrication pour une intégration 3D sont assez différentes de celles utilisées pour les circuits intégrés utilisant une technologie 2D. Les TSVs sont les interconnexions verticales assurant le transport des signaux et de l'alimentation. Cependant, ils propagent aussi la chaleur produite par d'autres niveaux de l'empilement 3D. Par exemple, ceci peut avoir comme effet le mauvais fonctionnement d'un niveau de l'empilement 3D due à une augmentation non prévue de sa température.

C'est dans ce contexte que s'inscrivent les travaux de thèse de C. Metzler (débutée en septembre 2011) dans le cadre du projet « Master 3D ». L'objectif de cette thèse est de développer des algorithmes de test ciblant les modèles de fautes liés aux mauvais fonctionnements induits par la consommation de puissance et la température dans les architectures 3D.

2.3 Collaborations Scientifiques

2.3.1 Collaborations Universitaires

- Laboratoire d'Automatique de Grenoble (LAG) – INPG, Grenoble, France

Dans le cadre de ma thèse (1998 – 2001) j'ai collaboré avec Monsieur René David, Directeur de Recherche Emérite au LAG.

- Université de Stuttgart, Allemagne

Dans le cadre des activités « Test Faible Consommation » et « Tolérances aux Fautes », nous collaborons avec le Professeur Hans-Joachim Wunderlich de l'université de Stuttgart.

- Institue de Technologie de Kyushu, Japon

Dans le cadre de l'activité « Test Faible Consommation », nous avons collaboré avec le Professeur Xiaoqing Wen de l'Institue de Technologie de Kyushu.

- Ecole Polytechnique de Turin, Italie

Dans le cadre de l'activité « Tolérance aux Fautes» nous collaborons avec le Professeur Mateo Sonza Reorda de l'école Polytechnique de Turin.

2.3.2 Collaborations Industrielles

- Société INTEL Mobile Communications (ex. INFINEON), Sophia Antipolis, France

dans le cadre de l'activité « Test des Mémoires SRAM ».

- Société ATMEL, Rousset, France

dans le cadre de l'activité « Test des Mémoires Flash ».

- Société ST-Microelectronics, Grenoble, France

dans le cadre de l'activité « Diagnostic Logique ».

- Société ST-Ericsson, Grenoble, France

dans le cadre de l'activité « Test Faible Consommation ».

- Société ST-Microelectronics, Crolles, France

dans le cadre de l'activité « Test de Pannes Temporelles ».

- Société CROCUS Technologie, Grenoble, France

dans le cadre de l'activité « Test des Mémoires MRAM ».

3 BILAN DE MA PRODUCTION SCIENTIFIQUE

Le Tableau 1.2 fournit un bilan par année de mes différents types de publications ; thèse, ouvrages, contributions à ouvrage (chapitre), revues scientifiques, conférences avec actes (avec un classement établi personnellemment de Rang A et Rang B), conférences invitées et colloques sans actes.

TABLEAU 1.2 RÉCAPITULATIF CHRONOLOGIQUE DE MES PUBLICATIONS

Nature du Document		**98**	**99**	**00**	**01**	**02**	**03**	**04**	**05**	**06**	**07**	**08**	**09**	**10**	**11**	**12**	**13**	**14**	**Total**
Thèse de Doctorat					1														**1**
Ouvrages													1						**1**
Contributions à ouvrage						1					1								**2**
Revues scientifiques			1		1	2			2	2	1	2	3	3	3		3	5	**28**
Conférences avec actes	Rang A	2		1	2	1	2	4	4	3	9	5	3	6	6	5	9	4	**66**
	Rang B			1				2	3	5	1	3	5	5	7	6	9	6	**53**
Conférences invitées									1	1		1			3	2	1		**9**
Colloques sans actes			1	2	3	2	2	3	7	10	8	5	8	6	8	9	3	3	**80**
Total		**2**	**2**	**4**	**7**	**6**	**4**	**9**	**17**	**21**	**20**	**16**	**20**	**20**	**27**	**22**	**25**	**18**	**240**

La liste détaillée par catégorie des mes publications est donnée en Partie 3.

4 RESPONSABILITES SCIENTIFIQUES

4.1 Encadrement Doctoral

4.1.1 Bilan des Encadrements de Thèses

Le Tableau 1.3 fournit le bilan des thèses pour lesquelles j'ai été ou je suis l'encadrant principal (avec un taux d'encadrement minimun de 50%) soit 8 thèses soutenues et 3 thèses en cours.

TABLEAU 1.3 RÉCAPITULATIF DES THÈSES – ENCADRANT PRINCIPAL

Nom	Titre de la Thèse	Soutenance	Directeur de Thèse
L. Dilillo	Test des Fautes Dynamiques dans les Mémoires SRAM	Juin 2005	S. Pravossoudovitch
N. Badereddine	Réduction de la Puissance de Pic lors de la Phase de Test	Septembre 2006	P. Girard
O. Ginez	Modélisation de Fautes et Test des Mémoires Flash	Novembre 2007	P. Girard
A. Ney	Test et Diagnostic de Fautes Dynamiques dans les Mémoires SRAM	Septembre 2008	P. Girard
J. Vial	Test et Testabilité de Structures Numériques Tolérantes aux Fautes	Décembre 2009	S. Pravossoudovitch
P.-D. Mauroux	Test et Fiabilité des Mémoires Flash	Décembre 2011	P. Girard
D. A. Tran	Test et Tolérance aux Fautes	Décembre 2012	S. Pravossoudovitch
J. Azevedo	Test de Mémoires MRAM	Octobre 2013	P. Girard
A. Asokan	Test de Délai sous Contraintes Physiques	Soutenance prévue en 2015	S. Pravossoudovitch
I. Wali	Tolérance aux Fautes	Soutenance prévue en 2016	A. Virazel
D. Patel	Test et Testabilité de Prototypes	Soutenance prévue en 2016	P. Girard

J'ai aussi participé au sein de mon équipe de recherche au suivi d'autres sujets de thèse. Le Tableau 1.4 présente ce bilan soit 6 thèses soutenues et 5 thèses en cours.

TABLEAU 1.4 RÉCAPITULATIF DE L'ENCADREMENT DE THÈSES – SUIVI DE THÈSES

Nom	Titre de la Thèse	Soutenance	Directeur de Thèse
A. Rousset	Diagnostic de pannes dans les circuits logiques	Avril 2008	P. Girard
Y. Benabboud	Diagnostic de pannes électriques dans les circuits logiques	Avril 2010	P. Girard
R. Alves Fonseca	Test est Fiabilité des Mémoires SRAM	Juillet 2011	S. Pravossoudovitch
F. Wu	Test de Circuits Faibles Consommations	Octobre 2011	P. Girard
L. Zordan	Test de Mémoires Faibles Consommation	Décembre 2013	P. Girard
Z. Sun	Diagnostic au Niveau Transistor	Mai 2014	S. Pravossoudovitch
M. Valka	Test de Circuits Basse Consommation	Soutenance prévue en 2014	P. Girard
C. Metzler	Test des Circuits 3D	Soutenance prévue en 2014	P. Girard
G. Tsiligiannis	Impact des Radiations sur les Mémoires SRAM	Soutenance prévue en 2014	S. Pravossoudovitch
A. Noccua	Modélisation de Puissance	Soutenance prévue en 2016	P. Girard
A. Touati	Diagnostic Logique	Soutenance prévue en 2016	A. Bosio

4.1.2 Présentation Détaillée des Sujets de Thèse

4.1.2.1 Thèses Soutenues

Thèse de : Luigi Dillilo
Titre : Test de Fautes Dynamiques dans les Mémoires SRAM
Soutenance : 8 Juin 2005
Jury :

M. André Touboul	Rapporteur
M. Olivier Sentieys	Rapporteur
M. Paolo Prinetto	Examinateur
M. Jean-Christophe Vial	Examinateur
M. Serge Pravossoudovitch	Directeur de Thèse
M. Patrick Girard	Codirecteur de Thèse

Publications associées : [RE5], [RE6], [RE8], [RE9], [RE11], [CO8], [CO9], [CO12], [CO13], [CO14], [CO15], [CO16], [CO18], [CO19], [CO20], [CO23], [CI1], [CI2], [DR9], [DR11], [DR13], [DR14], [DR18], [DR19]
Situation actuelle du diplômé : Chargé de Recherche CNRS au LIRMM
Résumé : Dans les systèmes sur puce (SoC), les éléments de mémorisation représentent la grande majorité des dispositifs embarqués. En effet, les mémoires occupent très couramment plus de la moitié de la surface des SoC actuels et la feuille de route établie par la SIA (« Semiconductor Industry Association ») indique que ce ratio devrait dépasser 90% d'ici dix ans. L'objectif de cette thèse a été d'étudier le comportement des mémoires statiques SRAM en présence de défauts à caractère temporel ou dynamique et de développer des solutions méthodologiques et algorithmiques permettant de mettre en évidence ces défauts. Ces travaux ont été réalisés en collaboration avec la Société Infineon (Sophia Antipolis) spécialisée dans la conception de mémoires SRAM. Ce partenariat a permis d'effectuer un travail de caractérisation des défauts sur la technologie actuelle employée par la Société Infineon. A partir de ce travail d'analyse et de caractérisation des modèles de fautes adaptés aux phénomènes mis en évidence ont été développés ainsi que des solutions méthodologique et algorithmique de test. Ces travaux de thèse ont été réalisés dans le cadre du projet Européen MEDEA+ « Associate ».

Thèse de : Nabil Badereddine
Titre : Réduction de Puissance Durant le Test Par SCAN des Circuits Intégrés
Soutenance : 15 Septembre 2006
Jury :

M. Patrick Girard	Directeur de Thèse
M. Serge Pravossoudovitch	Examinateur
M. Olivier Sentieys	Rapporteur
M. Matteo Sonza Reorda	Rapporteur
M. Arnaud Virazel	Examinateur
M. Jean-Marc Vrignaud	Examinateur

Publications associées : [OU2], [RE10], [CO17], [CO21], [CO22], [CO25], [CO26], [CO29], [CO30], [DR12], [DR16], [DR20], [DR21], [DR24], [DR25], [DR27]
Situation actuelle du diplômé : Ingénieur Test, Intel Wireless Communications, Sophia Antipolis
Résumé : Cette thèse s'inscrit dans le cadre de la réduction de la consommation de puissance durant le test par scan des circuits intégrés. Le test par scan est une technique de conception en vue du test qui est largement utilisée, mais qui pose quelques problèmes. Elle nécessite en effet un nombre important de cycles d'horloge pour permettre le chargement, l'application, et le déchargement des données de test. Ces opérations engendrent une activité de commutation dans le circuit largement plus importante que celle rencontrée lors du fonctionnement normal. Cette forte activité lors du test peut avoir des conséquences graves sur le circuit telles qu'une baisse de sa fiabilité ou sa destruction pure et simple. L'objectif de cette thèse est de proposer des techniques permettant de réduire cette suractivité, en particulier durant la période comprise entre l'application d'un vecteur de test et la récupération de la réponse du circuit.

Thèse de : Olivier Ginez
Titre : Modélisation de Fautes et Test des Mémoires Flash
Soutenance : 29 Novembre 2007
Jury :

M. Dominique Dallet	Rapporteur
M. Jean-Michel Portal	Rapporteur
M. Jean-Michel Daga	Examinateur
M. Arnaud Virazel	Examinateur
M. Joan Figueras	Membre Invité
M. Patrick Girard	Directeur de Thèse
M. Serge Pravossoudovitch	Codirecteur de Thèse

Publications associées : [RE12], [CO24], [CO27], [CO33], [CO35], [CO40], [DR15], [DR34], [DR35]
Situation actuelle du diplômé : Maître de Conférences, L2MP, Marseille.
Résumé : Les mémoires non volatiles de type Flash sont aujourd'hui présentes dans un grand nombre de circuits intégrés conçus pour des applications électroniques portables et occupent une grande partie de leur surface. L'absence de défauts à l'intérieur de ces mémoires constitue donc un des éléments clés du rendement de production pour tous les fabricants de ce type d'applications. Cependant, la grande densité d'intégration et la complexité de leur procédé de fabrication rendent ces mémoires Flash de plus en plus sensibles aux défauts de fabrication. Pour mettre en évidence les défaillances qui altèrent la fonctionnalité de ces mémoires, des solutions de test efficaces et peu coûteuses doivent être mises en place Les solutions et algorithmes actuellement utilisés pour tester les mémoires RAM ne sont pas adaptés à l'environnement Flash à cause de la faible vitesse de programmation de celle-ci. De plus, les modèles de faute que l'on trouve dans la littérature et qui sont relatifs aux mémoires RAM ne sont pas forcément réalistes dans le cas des mémoires Flash. La première partie de cette thèse propose une analyse complète des défauts réalistes que l'on trouve dans ces mémoires et qui sont extraits de données silicium issue d'une technologie Flash 150nm. Cette analyse, basée sur l'injection de défauts dans une matrice réduite de mémoire Flash, a permis de mettre en exergue un grand nombre de comportements fautifs et de leur attribuer des modèles de faute fonctionnels. La suite de ce travail de thèse est consacrée à l'élaboration de nouvelles solutions de test permettant d'améliorer les stratégies existantes. Les solutions proposées sont construites en s'appuyant sur les spécificités de la mémoire Flash, comme par exemple sa faculté à programmer certains de ses blocs en une seule fois avec le même motif et en un temps de programmation réduit. Une évaluation de ces solutions est ensuite effectuée à l'aide d'un simulateur de faute que nous avons spécialement développé à cet effet. Cette évaluation montre l'efficacité des solutions de test proposées en termes de couverture de fautes et de temps de test. La validation sur une mémoire Flash de 4Mbits a montré un gain en temps de test considérable (d'un facteur 34) ainsi qu'une couverture de fautes accrues (notamment pour les fautes de couplage) par rapport à des solutions utilisées dans l'industrie.

Thèse de : Alexandre Rousset
Titre : Diagnostic de pannes dans les circuits logiques : Développement d'une méthode ciblant un ensemble élargi de modèles de fautes
Soutenance : 1er Avril 2008
Jury :

M. Serge Pravossoudovitch	Président de Jury
M. Patrick Girard	Directeur de Thèse
Mme Chantal Robach	Rapporteur
M. Emmanuel Simeu	Rapporteur
M. Laroussi Bouzaida	Examinateur
M. Alberto Bosio	Examinateur

Publications associées : [CO28], [CO31], [CO37], [CO39], [CO41], [DR17], [DR23], [DR26], [DR29], [DR30], [DR32], [DR38]
Situation actuelle du diplômé : Ingénieur R&D, TRAD, Toulouse
Résumé : Avec l'évolution de la complexité et des performances des circuits intégrés, l'occurrence de défaillances non modélisables par de simples collages devient importante et même prépondérante. Ces effets ne sont généralement pas pris en compte par les méthodes classiques de diagnostic. Cette thèse a

pour objectif le développement d'une méthode de diagnostic ciblant un ensemble élargi de modèles de fautes. La méthode de diagnostic développée est présentée dans ce manuscrit de manière progressive. Dans un premier temps, les modèles de fautes considérés sont analysés afin de dégager les conditions de sensibilisation. La deuxième partie est consacrée à la présentation globale de la méthode de diagnostic développée. Cette méthode utilise principalement une approche « Effet à Cause » basée sur le traçage de chemins critiques. La troisième partie présente l'amélioration de cette méthode pour la prise en compte de pannes à effets spécifiques. La dernière partie est consacrée à la validation de chaque étape de l'évolution de la méthode de diagnostic au travers de diverses expérimentations.

Thèse de : Alexandre Ney
Titre : Test et Diagnostic de Fautes Dynamiques dans les Mémoires SRAM
Soutenance : 29 Septembre 2008
Jury :

M. Dominique Dallet	Rapporteur
M. Christophe Muller	Rapporteur
M. Jean-Christophe Vial	Examinateur
M. Arnaud Virazel	Examinateur
M. Patrick Girard	Directeur de Thèse
M. Serge Pravossoudovitch	Codirecteur de Thèse

Publications associées : [RE13], [CO32], [CO34], [CO36], [CO38], [CO42], [CO43], [CO44], [CO47], [CO49], [DR22], [DR33], [DR37], [DR43]
Situation actuelle du diplômé : Ingénieur Test, Infineon, Sophia Antipolis
Résumé : De nos jours, les mémoires sont présentes dans de nombreux circuits intégrés conçus pour des applications électroniques embarquées et occupent une majeure partie de la surface des systèmes sur puce (SoC). Ces mémoires deviennent donc les acteurs principaux du rendement de production. Or, une forte densité d'intégration associée à une complexité élevée des procédés de fabrications rendent ces mémoires toujours plus sensibles aux défauts de fabrications. Afin de mettre en évidence les défaillances survenant dans les mémoires, plusieurs méthodes de test existent. Ces solutions de test couramment utilisées pour les mémoires SRAM sont basées sur la détection de fautes statiques telles que les fautes de collage ou de couplage. Des algorithmes spécifiques, appelés algorithmes March, sont utilisés afin de mettre en évidence ce type de fautes. Cependant, ces solutions de test ne sont pas adaptées à la détection d'un nouveau type de faute apparaissant dans les technologies submicroniques. Ces fautes, appelées fautes dynamiques, sont principalement dues à des défauts de type « ouverts-résistif » et ne se manifestent que dans des configurations très spécifiques. En effet, une séquence d'opérations est nécessaire à la mise en évidence de ces fautes. Le premier objectif de cette thèse a été de proposer des solutions de test permettant la détection de fautes dynamiques dues à des défauts « ouverts-résistifs » dans le driver d'écriture et l'amplificateur de lecture. Une extension sur l'étude des comportements dynamiques face à des variations de procédés de fabrication dans le point mémoire a été proposée. Enfin, la seconde partie de cette thèse fournit de nouvelles solutions de diagnostic, capables de prendre en compte les fautes dynamiques d'une part, et proposant une détection précise des sites fautifs. Ces travaux ont été réalisés en collaboration avec la société Infineon basée à Sophia Antipolis spécialisée dans la conception de mémoires SRAM.

Thèse de : Julien Vial
Titre : Test et Testabilité de Structures Numériques Tolérantes aux Fautes
Soutenance : 16 Décembre 2009
Jury :

M. Serge Pravossoudovitch	Directeur de Thèse
M. Patrick Girard	Co-Directeur de Thèse
M. Jean Arlat	Rapporteur
M. Jean-François Naviner	Rapporteur
M. Régis Leveugle	Examinateur
M. Arnaud Virazel	Examinateur

Publications associées : [RE14], [RE17], [CO45], [CO46], [CO48], [CO53], [CO54], [DR31], [DR36], [DR39], [DR40], [DR41], [DR42], [DR47]

Situation actuelle du diplômé : PRAG, IUT Lyon.

Résumé : Les technologies submicroniques permettent aujourd'hui la réalisation de circuits intégrés regroupant des milliards de transistors sur une même puce. En prenant aussi en compte la miniaturisation croissante des procèdes de fabrication et la complexité des nouveaux circuits intégrés (SoC, Sipo), il est de plus en plus difficile de réaliser un circuit intègré sans aucun défaut de fabrication. Par conséquent, le rendement de fabrication des circuits diminue et une diminution de plus en plus importante est à craindre pour les prochaines années. Cette tendance est confirmée par l"ITRS (International Technology Roadmap for Semiconductors). L'objectif de cette thèse est d'étudier la possibilité de réaliser des structures numériques de tolérance aux fautes afin d'augmenter le rendement de fabrication. En effet, bien que ces structures aient été réalisées pour assurer une certaine sureté de fonctionnement lorsque le système est affecté par des fautes apparaissant pendant l'utilisation du circuit, plusieurs d'entre elles ont la capacité de tolérer des défauts de fabrication. Dans ce manuscrit, un état de l'art sur la tolérance aux fautes est réalisé. Puis, une architecture numérique tolérante aux fautes est choisie pour déterminer sa capacité à augmenter le rendement de fabrication. Il s'agit de l'architecture TMR (Triple Modular Redundancy). Une procédure de test permettant d'évaluer sa tolérance aux fautes est décrite. Une amélioration de l'architecture TMR est ensuite proposée. Cette amélioration consiste à partitionner les modules en plusieurs parties indépendantes. Grâce à cela, les architectures TMR sont suffisamment tolérantes aux défauts de fabrication pour pouvoir améliorer le rendement de fabrication des circuits intégrés. Le dernier chapitre de ce manuscrit concerne l'utilisation d'architectures TMR dans un contexte SoC. Plus le SoC contient de mémoires, plus la réalisation d'architectures TMR permet d'augmenter le rendement.

Thèse de : Youssef Benabboud

Titre : Diagnostic de pannes électriques dans les circuits logiques

Soutenance : 30 avril 2010

Jury :

M. Abbas Dandache	Rapporteur
M. Emmanuel Simeu	Rapporteur
M. Olivia Riewer	Examinateur
M. Alberto Bosio	Examinateur
M. Patrick Girard	Directeur de Thèse
M. Serge Pravossoudovitch	Co-directeur de Thèse

Publications associées : [CO50], [CO51], [CO52], [CO56], [CO66], [DR46]

Situation actuelle du diplômé : Ingénieur R&D, LFoundry, France

Résumé : Les technologies avancées (finesse de gravure inférieure à 90nm) permettent la production de circuits de plus en plus complexes avec des performances très élevées. Ces nouvelles technologies imposent donc de nouveaux défis pour la conception de circuits, mais également pour les méthodologies de test de fabrication et de diagnostic. De ce point de vue, les défaillances observées dans ces technologies ne peuvent pas être modélisées par des fautes classiques de collage. Les fautes de délai, de court-circuit, de circuit ouvert, etc. doivent également être prises en compte. Dans ce contexte, l'objectif de cette thèse a été de développer une méthode de diagnostic logique capable à la fois de traiter un ensemble complet de modèles de fautes et de fournir une localisation fiable et précise des défaillances dans un système sur puce. Ce manuscrit est organisé comme suit. Dans la première partie, les modèles de faute existants sont analysés afin de montrer les conditions de sensibilisation de chacun d"eux. La deuxième partie présente une méthode de diagnostic logique basée sur une approche « Effet-à-Cause». La dernière partie propose une nouvelle technique de diagnostic basée sur une approche « Cause-à-Effet » et permettant de traiter les circuits séquentiels. Les deux approches de diagnostic proposées exploitent les conditions de sensibilisations afin de cibler un ensemble élargi de modèles de fautes durant le processus de diagnostic. La première technique a été complètement validée, la deuxième partiellement validée sur un ensemble important de circuits benchmark et sur des systèmes sur puce fournis par la société STMicroelectronics.

Thèse de : Renan Alves Fonseca
Titre : Test est Fiabilité des Mémoires SRAM
Soutenance : 21 juillet 2011
Jury :

M. Serge Pravossoudovitch	Directeur de Thèse
M. Patrick Girard	Codirecteur de Thèse
M. Luigi Dilillo	Examinateur
M. Jean-Christophe Vial	Examinateur
M. Paolo Prinetto	Rapporteur
M. Sandip Kundu	Rapporteur

Publications associées : [RE19], [CO57], [CO58], [CO60], [CO61], [CO62], [CO75], [DR45], [DR50], [DR52], [DR62]
Situation actuelle du diplômé : Enseignement supérieur, Brésil
Résumé : Aujourd'hui, les mémoires SRAM sont faites avec les technologies les plus rapides et sont parmi les éléments les plus importants dans les systèmes complexes. Les cellules SRAM sont souvent conçues en utilisant les dimensions minimales du nœud technologique. En conséquence, les SRAM sont plus sensibles à de nouveaux phénomènes physiques qui se produisent dans ces technologies, et sont donc extrêmement vulnérables aux défauts physiques. Afin de détecter si chaque composant est défectueux ou non, des procédures de test de haut coût sont employées. Différentes questions liées à cette procédure de test sont compilées dans ce document. Un des principaux apports de cette thèse est d'établir une méthode pour définir les conditions environnementales lors de la procédure de test afin de capter des défauts non-déterministes. Puisque des simulations statistiques sont souvent utilisées pour étudier des défauts non-déterministes, une méthode de simulation statistique efficace a été spécialement conçue pour la cellule SRAM. Dans cette thèse, nous traitons aussi la caractérisation de fautes, la caractérisation de la variabilité et la tolérance aux fautes.

Thèse de : Fangmei Wu
Titre : Test de Circuits Faibles Consommations
Soutenance : 12 octobre 2011
Jury :

Mme Nathalie Julien	Rapporteur
M. Emmanuel Simeu	Rapporteur
M. Nabil Badereddine	Examinateur
M. Luigi Dilillo	Examinateur
M. Patrick Girard	Directeur de Thèse
M. Serge Pravossoudovitch	Codirecteur de Thèse
M. Alberto Bosio	Membre invité

Publications associées : [RE16], [CO63], [CO65], [CO69], [CO78], [CI5], [DR48], [DR51], [DR53], [DR56], [DR64]
Situation actuelle du diplômé : Femme au foyer
Résumé : Cette thèse concerne l'étude et la réduction de la consommation de puissance durant le test par SCAN des circuits digitaux. Afin de détecter les fautes de transition, les deux principaux schémas d'horloge utilisés sont : Launch-Off-Shift (LOS) et launch-Off-Capture (LOC). L'ensemble des travaux réalisés montre que le test LOS est plus efficace que le test LOC en termes de couverture de faute de transition et de durée de test. Toutefois, le test LOS demande une consommation de puissance plus élevée lors du cycle de « launch-to-capture » (LTC), notamment en termes de pic de consommation. Dans cette thèse, nous proposons une nouvelle approche de génération de vecteurs de test LOS sous contrainte de puissance. La technique proposée est capable de réduire et d'évaluer les pics de consommation durant le test afin de se rapprocher le plus possible de la consommation fonctionnelle. Les avantages résultants permettent de résoudre les problèmes liés aux pertes de rendement et ceux liés au « test escape » (circuits fautifs déclarés sains).

Thèse de : Pierre-Didier Mauroux
Titre : Test et Fiabilité des Mémoires Flash
Soutenance : 9 décembre 2011
Jury :

M. Jean-Michel Portal	Rapporteur
M. Patrick Garda	Rapporteur
M. Philippe Coll	Examinateur
M. Arnaud Virazel	Examinateur
M. Serge Pravossoudovitch	Codirecteur de Thèse
M. Patrick Girard	Directeur de Thèse

Publications associées : [RE18], [CO55], [CO59], [CO68], [CO70], [CI4], [DR44], [DR49], [DR54], [DR55]
Situation actuelle du diplômé : Ingénieur R&D, ATMEL Rousset, France
Résumé : Depuis quelques années, les mémoires non-volatiles de type Flash sont présentes dans un grand nombre de systèmes sur puce. La grande densité d'intégration et la complexité de leur procédé de fabrication rendent les mémoires Flash de plus en plus sujette aux défauts. La présence de défauts affecte le rendement, la rétention, l'endurance et donc la fiabilité des mémoires Flash. Cette thèse a porté sur l'analyse des mécanismes de défaillances, la modélisation des comportements fautifs et le développement de solution en vue d'améliorer le test des mémoires Flash. Dans ce contexte, nous avons proposé un modèle SPICE de la mémoire Flash TSTAC^{TM} d'ATMEL. En comparaison avec l'état de l'art, le modèle SPICE proposé permet de simuler les opérations fonctionnelles de la mémoire de manière dynamique. Ce modèle a était utilisé pour effectuer des simulations d'injections de défauts réalistes pouvant affecter la matrice de la mémoire Flash TSTAC^{TM}. D'autres types de simulations électriques effectuées à l'aide du modèle ont permis de développer deux méthodes de caractérisation : la première permettant de détecter les variations d'épaisseur d'oxyde des cellules mémoires ; la deuxième méthode permet de caractériser la programmation par pulsation (pulse programming) et ainsi prédire la valeur du champ électrique durant l'écriture d'une cellule.

Thèse de : Duc Anh Tran
Titre : Architecture Hybride Tolérante aux Fautes pour l'Amélioration de la Robustesse des Circuits et Systèmes Intégrés Numériques
Soutenance : 21 décembre 2012
Jury :

Mme. Lirida Naviner	Rapporteur
M. Matteo Sonza Reorda	Rapporteur
M. Régis Leveugne	Examinateur
M. Arnaud Virazel	Examinateur
M. Serge Pravossoudovitch	Directeur de Thèse
M. Patrick Girard	Codirecteur de Thèse

Publications associées : [RE26],[CO64], [CO77], [CO80], [DR57], [DR58], [DR59]
Situation actuelle du diplômé : Ingénieur R&D, Sondrel, UK
Résumé : L'évolution de la technologie CMOS consiste à la miniaturisation continue de la taille des transistors. Cela permet la réalisation de circuits et systèmes intégrés de plus en plus complexes et plus performants, tout en réduisant leur consommation énergétique, ainsi que leurs coûts de fabrication. Cependant, chaque nouveau nœud technologique CMOS doit faire face aux problèmes de fiabilité, dues aux densités de fautes et d'erreurs croissantes. Par conséquence, les techniques de tolérance aux fautes, qui utilisent des ressources redondantes pour garantir un fonctionnement correct malgré la présence des fautes, sont devenues indispensables dans la conception numérique. Cette thèse étudie une nouvelle architecture hybride tolérante aux fautes pour améliorer la robustesse des circuits et systèmes numériques. Elle s'adresse à tous les types d'erreur dans la partie combinatoire des circuits, c'est-à-dire des erreurs permanentes (« hard errors »), des erreurs transitoires (« SETs ») et des comportements temporels fautifs (« timing errors »). L'architecture proposée combine la redondance de l'information (pour la détection d'erreur), la redondance de temps (pour la correction des erreurs transitoires) et la redondance matérielle (pour la correction des erreurs permanentes). Elle permet de réduire considérablement la consommation d'énergie, tout en ayant une surface de silicium similaire

comparée aux solutions existantes. En outre, elle peut également être utilisée dans d'autres applications, telles que pour traiter des problèmes de vieillissement, pour tolérer des fautes dans les architectures pipelines, et pour être combiné avec des systèmes avancés de protection des erreurs transitoires dans la partie séquentielle des circuits logiques (« SEUs »).

Thèse de : Joao Azevedo
Titre : Test et Testabilité des Mémoires MRAM
Soutenance : 11 octobre 2013
Jury :

M. Jean-Michel Portal	Rapporteur
M. Olivier Sentieys	Rapporteur
M. Ken Mackay	Examinateur
M. Arnaud Virazel	Examinateur
M. Serge Pravossoudovitch	Directeur de Thèse
M. Patrick Girard	Codirecteur de Thèse

Publications associées : [RE24], [CO79], [CO81], [CO90], [CO107], [DR60], [DR66], [DR67], [DR70],
Situation actuelle du diplômé : Post-Doc, LIRMM
Résumé : De nos jours, les mémoires occupent une grande superficie en silicium dans les System- on-Chips. Très largement utilisés, les mémoires Flash non volatiles présentent encore plusieurs inconvénients. Les MRAMs permettent de répondre à toutes les problema- tiques liées aux Flash. Cependant, elles sont sujettes à des défauts comme tout autre type de mémoire. Très peu de travaux portent sur le test de MRAM et la recherche effectuée dans ce domaine vise principalement la première génération de mémoires magnétiques. Dans ce travail, la physique derrière la modélisation MTJ est abordée. Cette com- préhension est le point de départ pour développer un modèle fiable. Le MTJ est l'élément de base pour les technologies MRAM. L'injection de défauts résistif ouvert, résistif courts-circuits et capacitives ont été réalisées dans le but d'analyser les mécanismes de défaillance spécifiques de la TAS-MRAM. Un test du type march spécifique est pro- posé à l'aide des résultat d'analyses d'injection de défauts et de l'association de chaque mécanisme de défaillance à un modèle de défaut fonctionnel spécifique. L'évolution du TAS-MRAM est la MRAM à base MLU qui est également développée par Crocus Technology. Finalement, un modèle MLU-MTJ sera élaboré et discuté.

Thèse de : Leonardo Zordan
Titre : Test de Mémoires SRAM à Faible Consommation
Soutenance : 6 décembre 2013
Jury :

Mme. Loréna Anghel	Rapporteur
M. Matteo Sonza Reorda	Rapporteur
Mme. Nathalie Julien	Examinateur
M. Alberto Bosio	Examinateur
M. Luigi Dilillo	Membre invité
M. Arnaud Virazel	Membre invité
M. Serge Pravossoudovitch	Codirecteur de Thèse
M. Patrick Girard	Directeur de Thèse

Publications associées : [CO71], [CO82], [CO87], [CO93], [CO96], [CO103], [CI6], [DR61]
Situation actuelle du diplômé : Ing. R&D, INTEL, Sophia Antipolis
Résumé : De nos jours, les mémoires embarquées sont les composants les plus denses dans les "System-On-Chips" (SOCs), représentant actuellement plus que 90% de leur superficie totale. Parmi les différents types de mémoires, les SRAMs sont très largement utilisées dans la conception des SOCs, particulièrement en raison de leur haute performance et haute densité d'intégration. En revanche, les SRAMs conçues en utilisant des technologies submicroniques sont devenus les principaux contributeurs de la consommation d'énergie globale des SOCs. Par conséquent, un effort élevé est actuellement consacré à la conception des SRAMs à faible consommation. En plus, en raison de leur structure dense, les SRAMs sont devenus de plus en plus susceptibles aux défauts physiques

comparativement aux autres blocs du circuit, notamment dans les technologies les plus récentes. Par conséquent, les SRAMs se posent actuellement comme le principal détracteur du rendement des SOCs, ce qui cause la nécessité de développer des solutions de test efficaces ciblant ces dispositifs. Dans cette thèse, des simulations électriques ont été réalisées pour prédire les comportements fautifs causés par des défauts réalistes affectant les blocs de circuits spécifiques aux technologies SRAM faible consommation. Selon les comportements fautifs identifiés, différents tests fonctionnels, ainsi que des solutions de tests matériels, ont été proposés pour détecter les défauts étudiés. Par ailleurs, ce travail démontre que les circuits d'écriture et lecture, couramment incorporés dans les SRAMs faible consommation, peuvent être réutilisés pour augmenter le stress dans les SRAMs lors du test, ce qui permet d'améliorer la détection des défauts affectant la mémoire.

Thèse de : Zhenzhou Sun
Titre : Amélioration de la Localisation de Défauts dans les Circuits Digitaux par Diagnostic au Niveau Transistor
Soutenance : 16 mai 2014
Jury :

M. Matteo Sonza Reorda	Rapporteur
M. Salvador Mir	Rapporteur
M. Etienne Auvray	Examinateur
M. Alberto Bosio	Examinateur
M. Serge Pravossoudovitch	Codirecteur de Thèse
M. Patrick Girard	Directeur de Thèse

Publications associées : [CO89], [CO92], [DR69], [DR74], [DR77]
Situation actuelle du diplômé : Ing. R&D, Cadence, Paris
Résumé : La croissance rapide dans le domaine des semi-conducteurs fait que les circuit digitaux deviennent de plus en plus complexes. La capacité à identifier la cause réelle d'une défaillance dans un circuit digital est donc critique. Le diagnostic logique est une procédure qui permet de localiser une erreur observée dans un circuit fautif, l'analyse de défaillance peut être ensuite appliquée pour déterminer la cause réelle de cette erreur. Un diagnostic efficace et précis est donc fondamental pour améliorer les résultats de l'analyse de défaillance et augmenter éventuellement le rendement de production. "Effet à Cause" et "Cause à Effet" sont deux approches classiques pour le diagnostic logique. Ce diagnostic fournit une liste de suspects au niveau porte logique. Cependant, cette approche n'est pas précise dans le cas où le défaut est localisé à l'intérieur de la cellule logique. Dans cette thèse, nous proposons une nouvelle méthode de diagnostic intra-cell basé sur l'approche "Effet à Cause" pour améliorer la précision de la localisation de défaut au niveau transistor. L'approche proposée utilise l'algorithme CPT (Traçage de chemins critiques) appliqué au niveau transistor. Pour chaque cellule suspecte, nous appliquons un CPT avec les vecteurs de test fautifs. Le résultat obtenu est une liste de suspects préliminaires. Chaque suspect peut être un noeud (G, S, D) de transistor. Par la suite, nous appliquons un CPT avec les vecteurs de test non-fautifs pour minimiser la liste de suspects. La méthode proposée donne la localisation précise du défaut pour une erreur observée. Par ailleurs, la méthode est indépendante du modèle de faute invoqué.

4.1.2.2 Thèses en Cours

Thèse de : Miroslav Valka
Titre : Test de Circuits Basse Consommation
Soutenance : prévue en septembre 2014
Directeur de Thèse : Patrick Girard
Publications associées : [CO73], [CO76], [CO91], [CO111], [DR72]

Thèse de : Carolina Metzler
Titre : Test des Circuits 3D
Soutenance : prévue en septembre 2014
Directeur de Thèse : Patrick Girard
Publications associées : [CO83], [CO88], [CO97], [CO110], [CO114], [DR71]

Thèse de : Georgios Tsiligiannis
Titre : Impact des Radiations sur les Mémoires SRAM
Soutenance : prévue en septembre 2014
Directeur de Thèse : Serge Pravossoudovitch
Publications associées : [RE22], [RE25], [RE27], [RE28], [CO84], [CO85], [CO86], [CO99], [CO100], [CO101], [CO104], [CO105], [CO106], [CO109], [CO118], [CO119], [RE73], [RE76]

Thèse de : Anu Asokan
Titre : Test de Délai sous Contraintes Physiques
Soutenance : prévue en septembre 2015
Directeur de Thèse : Serge Pravossoudovitch
Publications associées : [CO113], [CO117], [DR80]

Thèse de : Imran Wali
Titre : Tolérance aux Fautes
Soutenance : prévue en septembre 2016
Directeur de Thèse : Arnaud Virazel
Publications associées : [CO112], [DR78]

Thèse de : Aymen Touati
Titre : Diagnostic Logique
Soutenance : prévue en septembre 2016
Directeur de Thèse : Alberto Bosio
Publications associées : [CO116], [DR79]

Thèse de : Darayus Patel
Titre : Test et Testabilité de Prototypes
Soutenance : prévue en septembre 2016
Directeur de Thèse : Patrick Girard

Thèse de : Alejandro Noccua
Titre : Modélisation de Puissance
Soutenance : prévue en septembre 2016
Directeur de Thèse : Patrick Girard

4.2 Encadrement de Stages de Master – Université Montpellier II

4.2.1 Master 1ère année

Stage de : N. Froget
Sujet du Stage : Outil d'Evaluation de l'Activité de Commutation des les Circuits
Période : avril 2004 à juillet 2004

Stage de : N. Rondier
Sujet du Stage : Implantation matérielle d'un générateur d'adresse
Période : avril 2005 à juillet 2005

Stage de : A. El Fdil
Sujet du Stage : Réalisation d'un Outil d'Injection de Fautes
Période : avril 2006 à juillet 2006

Stage de : P.-D. Mauroux
Sujet du Stage : Outils de Test – Logiciel et ATE
Période : avril 2007 à juillet 2007

Stage de : N. Ettaki
Sujet du Stage : Implantation sur FPGA d'un Processeur
Période : avril 2008 à juillet 2008

Stage de : J. Thaour
Sujet du Stage : Implantation sur FPGA d'un Processeur
Période : avril 2010 à juillet 2010

Stage de : A. Ouzia
Sujet du Stage : Développement d'une Structure Matérielle de Tolérance aux Fautes
Période : avril 2011 à juillet 2011

Stage de : Y. Si Ahmed
Sujet du Stage : Développement d'une Structure Matérielle de Tolérance aux Fautes
Période : avril 2011 à juillet 2011

Stage de : G. Harcha
Sujet du Stage : Développement d'un Banc de Test pour Mémoire Magnétique TAS-MRAM
Période : avril 2014 à juillet 2014

4.2.2 Master 2ème année

Stage de : B. Bel'Hantier
Sujet du Stage : Réduction de la Consommation lors du Test par Ré-ordonnancement de Chaîne de Scan
Période : février 2003 à juillet 2003

Stage de : A. Rousset
Sujet du Stage : Diagnostic de Pannes Temporelles dans les Circuits munis d'une Chaîne de Scan
Période : février 2004 à juillet 2004

Stage de : J. Vial
Sujet du Stage : Test de Structures Tolérantes aux Pannes
Période : février 2006 à juillet 2006

Stage de : L. Damri
Sujet du Stage : Implantation d'un TMR sur un Système sur Puce
Période : mars 2009 à juillet 2009

Stage de : M. Sabsabi
Sujet du Stage : Test et Tolérance des Mémoire Flash NAND
Période : mars 2010 à juillet 2010

Stage de : A. Ouzia
Sujet du Stage : Implémentation de Portes Logiques Dynamiques
Période :mars 2012 à juillet 2012

Stage de : Y. Si Ahmed
Sujet du Stage : Implantation d'un uP en VHDL
Période : mars 2013 à juillet 2013

Stage de : A. Makhlouf
Sujet du Stage : Implémentation d'une Approche Hybride de Tolérance aux Fautes sur un Processeur Pipeline
Période : mars 2014 à juillet 2014

4.3 Encadrement de Projets d'Elèves Ingénieurs – EII / Polytech

Projet de : M. Hage-Hassan
Sujet du Projet : Test de Pannes Temporelles dans les Décodeurs de Mémoires SRAM
Période : septembre 2003 à janvier 2004
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : S. Bouniol
Sujet du Projet : Test des Fautes Dynamiques du Point Mémoire SRAM
Période : septembre 2003 à janvier 2004
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : J. Mensorali
Sujet du Projet : Conception en vue du Test de Pannes Temporelles dans les Mémoires SRAM
Période : septembre 2003 à janvier 2004
Collaboration industrielle : STMicroelectronics, Crolles

Projet de : A. Belkhadili
Sujet du Projet: Test des Circuits de Pré Charge des Mémoires SRAM
Période : septembre 2004 à janvier 2005
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : R. Roudani
Sujet du Projet: Evaluation des Séquences de Test pour les Mémoires SRAM
Période : septembre 2005 à janvier 2006
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : F. Yougbare
Sujet du Projet: Impact des Variations du Processus de Fabrication sur les Mémoires SRAM
Période : septembre 2005 à janvier 2006
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : F. Didier
Sujet du Projet: Impact des Variations du Processus de Fabrication sur les Mémoires SRAM
Période : septembre 2006 à janvier 2007
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : M. Moussally
Sujet du Projet: Simulateur de Fautes pour les Mémoires Flash
Période : septembre 2006 à janvier 2007
Collaboration industrielle : ATMEL, Rousset

Projet de : I. Issa
Sujet du Projet: Implantation d'une Méthode de Diagnostic
Période : septembre 2006 à janvier 2007
Collaboration industrielle : STMicroelectronics, Crolles

Projet de : C. Tabouret
Sujet du Projet: Réalisation d'un banc de test de mémoires
Période : septembre 2007 à janvier 2008
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : F. Devic
Sujet du Projet: Test intégré de mémoires SRAM
Période : septembre 2008 à janvier 2009
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : A. Polte
Sujet du Projet: Evaluation de la Stabilité d'une Cellule SRAM dans un Environnement Faible Consommation
Période : septembre 2009 à janvier 2010
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : C. Rodrigues
Sujet du Projet: Mise en place d'un modèle de simulation de mémoire SRAM
Période : septembre 2010 à janvier 2011
Collaboration industrielle : Infineon Technologies, Sophia Antipolis

Projet de : E. M. El Amrani
Sujet du Projet: Amélioration d'un Outil de Diagnostic
Période : septembre 2011 à janvier 2012
Collaboration industrielle : STMicroelectronics, Grenoble

4.4 Autres Responsabilités Scientifiques

4.4.1 Participation à des Jurys de Thèses

Thèse de Nabil Badereddine – Examinateur
soutenue le 15 septembre 2006 au LIRMM, Université de Montpellier 2

Thèse de Olivier Ginez – Examinateur
soutenue le 29 novembre 2007 au LIRMM, Université de Montpellier 2

Thèse de Alexandre Ney – Examinateur
soutenue le 29 septembre 2008 au LIRMM, Université de Montpellier 2

Thèse de Julien Vial – Examinateur
soutenue le 16 décembre 2009 au LIRMM, Université de Montpellier 2

Thèse de Pierre-Didier Mauroux – Examinateur
soutenue le 9 décembre 2011 au LIRMM, Université de Montpellier 2

Thèse de Duc Anh Tran – Examinateur
soutenue le 21 décembre 2012 au LIRMM, Université de Montpellier 2

Thèse de Joao Azevedo – Examinateur
soutenue le 11 octobre 2013 au LIRMM, Université de Montpellier 2

Thèse de Léonardo Zordan – Membre Invité
soutenue le 6 décembre 2013 au LIRMM, Université de Montpellier 2

4.4.2 Participation à des Comités de Programmes de Conférence

2005	IEEE International Conference on Embedded and Ubiquitous Computing
Depuis 2008	IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era
Depuis 2008	IEEE International Symposium and Exhibits in Quality Electronic Design
Depuis 2009	ACM/IEEE Design Automation and Test in Europe
Depuis 2009	IEEE Asia Symposium on Quality Electronic Design
Depuis 2009	IEEE International Conference on Advances in System Testing and Validation Lifecycle
Depuis 2010	IEEE European Test Symposium
Depuis 2011	IEEE International Conference on Computer Design

4.4.3 Présidence de Sessions de Conférence

2007	IEEE International Test Conference – Session « Design for Testability »
2008	IEEE European Test Symposium – Session « Delay Fault Testing »
2009	ACM/IEEE Design Automation and Test in Europe – Session « Debug and Diagnosis »
2010	IEEE European Test Symposium – Session poster
2011	ACM/IEEE Design Automation and Test in Europe – Session « Advances in Test Generation and Fault Simulation »
2011	IEEE European Test Symposium – Session « Power switches »

4.4.4 Participation à des Comités de Lecture

Revues

TCAD – Transactions on Computer-Aided Design	depuis 2002
JETTA – Journal of Electronic Testing: Theory and Application	depuis 2003
TODAES - Transactions on Design Automation of Electronic Systems	depuis 2003
JOLPE – Journal of Low Power Electronics	depuis 2005
IET CDT – Journal Computers & Digital Techniques	depuis 2007
TVLSI – Transactions on Very Large Scale Integration Systems	depuis 2008
TECS – Transactions on Embedded Computing Systems	depuis 2010

Conférences

DAC – Design Automation Conference	2005 / 2006 / 2007
DATE – Design Automation and Test in Europe	2003 / 2006
DDECS - Design and Diagnostics of Electronic Circuits and Systems	2003
DELTA - Symposium on Electronic Design, Test & Applications	2007
DTIS – Design and Technology of Integrated Systems in Nanoscale Era	2006

ETS – European Test Symposium	2003 / 2006
ICCAD – International Conference on Computer-Aided Design	2008
ICCD – International Conference on Computer Design	2004 / 2005 / 2008 / 2011 / 2012
IOLTS – International On-Line Testing Symposium	2006
ITC – International Test Conference	depuis 2005
VTS – VLSI Test Symposium	2003 / 2004 / 2005 / 2008 / 2009

4.4.5 Participation à l'Organisation de Congrès

2001 IFIP International Conference on VLSI (VLSI-SOC)
Montpellier, France, 3-5 décembre 2001
Réalisation des actes

2002 IEEE European Test Worshop (ETW)
Corfou, Grèce, 2002
Réalisation du CD ROM

2004 South European Test Seminar
Morzine, 15-19 mars 2004
Responsable de l'organisation locale

2004 IEEE European Test Symposium (ETS)
Ajaccio, France, 23-26 mai 2004
Réalisation des actes et du CD ROM

2004 Workshop on Silicon Debug and Diagnosis (SDD)
Ajaccio, France, 27 mai 2004
Responsable de l'organisation locale

2005 IEEE European Test Symposium (ETS)
Tallinn, Estonie, 22-25 mai 2005
Préparation du CR ROM pour le 10ème anniversaire de l'ETS

2013 IEEE European Test Symposium (ETS)
Avignon, France, 27-31 mai 2013
Responsable de l'organisation locale et du budget (Ecole de printemps - 2 jours, Symposium - 3 jours et trois « worhshop » parallèles - 1 jour), (270 participants), (110k€ de budget).

2013 Workshop « Leading-Edge Embedded Non Volatile Memories »
Gardanne, France, 30 septembre au 1 octobre 2013
Membre du comité exécutif – 160 participants

5 CONTRATS DE RECHERCHE

5.1 Bilan Chronologique

Le Tableau 1.5 présente les différents contrats de recherche auxquels j'ai participé et je participe actuellement.

TABLEAU 1.5 RÉCAPITULATIF DES CONTRATS DE RECHERCHE

Contrat	97	98	99	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16
EUREKA : MEDEA																				
MEDEA + : ASSOCIATE																				
MEDEA + : NANOTEST																				
STM Crolles A																				
INFINEON																				
CATRENE : TOETS																				
ATMEL																				
INTEL																				
ANR ARPEGE : EMYR																				
STE Grenoble																				
STM Grenoble																				
ENIAC : ELESIS																				
CATRENE : MASTER 3D																				
LIA LAFISI																				
FUI HICOOL																				
STM Crolles B																				

5.2 Présentation des Contrats

EUREKA : MEDEA
Nature du contrat : Projet CEE EUREKA - MEDEA - n° AT406
Titre du contrat : « Advanced Tools for Deep Sub-micron Designs »
Partenaires : ALCATEL, ANACAD, BULL, PHILIPS, TEMIC MHS, THOMSON TCS, TEMENTO, UPMC, LIRMM
Période du contrat : 1997-2000

MEDEA + : ASSOCIATE
Nature du contrat : Projet CEE EUREKA - MEDEA - n° A503
Titre du contrat : « Advanced Solutions for SOC Integration And Test in Europe »
Partenaires : ALCATEL, PHILIPS, INFINEON, TEMENTO, LIP6, INESC, LIRMM
Période du contrat : 2001-2004

MEDEA+ NanoTEST
Nature du contrat : Projet CEE EUREKA - MEDEA - n° 2A702
Titre du contrat : « NanoTEST »
Partenaires : STMicroelectronics, Infineon, Philips, NXP, Q-Strar Test, Temento, CEA-LETI, TIMA, LIRMM
Période du contrat : 2005-2008

STM Crolles A
Nature du contrat : Convention de collaboration industrielle + Bourse Cifre
Titre du contrat : « Diagnostic de circuits microélectroniques »
Partenaires : STMicroelectronics Crolles, LIRMM
Période du contrat : 2007-2009

INFINEON
Nature du contrat : Convention de collaboration industrielle
Titre du contrat : « Test de Mémoires SRAM »
Partenaires : Infineon, LIRMM
Montant pour le LIRMM : 130 k€
Période du contrat : 2008-2011

CATRENE TOETS
Nature du contrat : Projet CEE EUREKA - CATRENE- n° CT302
Titre du contrat : « TOETS : Towards One European Test Solution »
Partenaires : NXP, ON Semiconductor, Q-star, E2V Semiconductor, Infineon, STMicroelectronics, Temento Systems, iRoc, MXM Group, Essilor, Handshake Solutions, CEA Leti, CEA List, UT/CTIT, Supelec, TIMA, KU Leuven, LIRMM
Montant pour le LIRMM : 740 k€
Période du contrat : 2009-2012

ATMEL
Nature du contrat : Convention de recherche
Titre du contrat : « Test et fiabilité des mémoires Flash »
Partenaires : ATMEL Rousset, LIRMM
Période du contrat : 2004-2006 et 2009-2011

INTEL
Nature du contrat : Convention de collaboration industrielle
Titre du contrat : « Test de Mémoires SRAM faibles consommations »
Partenaires : Intel, LIRMM
Montant pour le LIRMM : 130 k€
Période du contrat : 2011-2013

EMYR
Nature du contrat : ANR, programme ARPEGE
Titre du contrat : « Enhancement of MRAM Memory Yield and Reliability »
Partenaires : CEA List, CROCUS Technology, LIRMM
Montant pour le LIRMM : 180 k€
Période du contrat : 2011-2013

STE Grenoble
Nature du contrat : Convention de collaboration industrielle + Bourse Cifre
Titre du contrat : « Test de Circuits Basse Consommation »
Partenaires : STE, LIRMM
Montant pour le LIRMM : 45 k€
Période du contrat : 2011-20014

STM Grenoble
Nature du contrat : Convention de collaboration industrielle + Bourse Cifre
Titre du contrat : « Diagnostic au Niveau Transistor »
Partenaires : STM, LIRMM
Montant pour le LIRMM : 30 k€
Période du contrat : 2011-20014

ENIAC ELESIS
Nature du contrat : Projet CEE ENIAC
Titre du contrat : « ELESIS : European Library-based flow of Embedded Silicon test Instruments »
Partenaires : NXP, STMicroelectronics, ATMEL, Salland Eng., JTAG Technologies, D4T Systems, Temento Systems, PRESTO Eng., iRoc, NANIUM, Infineon, Q-star, CEA, TIMA, LIRMM, INESC Porto, Univ. Twente
Montant pour le LIRMM : 670 k€
Période du contrat : 2012-2015

CATRENE MASTER 3D
Nature du contrat : Projet CEE EUREKA - CATRENE- n° CT312
Titre du contrat : « ELESIS : European Library-based flow of Embedded Silicon test Instruments »
Partenaires : ALES, ams AG, AXO, CAMTEK, CEA-LETI, CNRS LIRMM, DR Yield, EVG, FhG IWMH, Fogale, Fraunhofer, IMS Bordeaux, Infineon, ISIS, NXP, PVA AS, QUALTERA SAS
Montant pour le LIRMM : 310 k€
Période du contrat : 2013-2015

LIA LAFISI
Nature du contrat : Laboratoire International Associé / CNRS
Titre du contrat : « Test et Test Intégré de Circuits et Systèmes »
Partenaires : Politecnico di Torino, LIRMM
Montant pour le LIRMM : 60 k€
Période du contrat : 2013-2016

FUI HICOOL
Nature du contrat : Laboratoire International Associé / CNRS
Titre du contrat : « Solutions front-end de conception faible puissance de circuits intègres complexes »
Partenaires : DeFacTo, Docea, STMicroelectronics, TIMA, LIRMM
Montant pour le LIRMM : 280 k€
Période du contrat : 2013-2015

STM Crolles B
Nature du contrat : Convention de collaboration industrielle + Bourse Cifre
Titre du contrat : « Test et Testabilité de Circuits Prototypes »
Partenaires : STMicroelectronics Crolles, LIRMM
Montant pour le LIRMM : 35 k€
Période du contrat : 2013-2016

La répartition thématique des contrats de recherche est donnée sur le Tableau 1.6.

TABLEAU 1.6 RÉPARTITION THÉMATIQUE DES CONTRATS DE RECHERCHE

Thèmes de Recherche	**Contrat de Recherche Associé**
Test de Pannes Temporelles	MEDEA, ELESIS, STM Crolles B, LAFISI
Test Faible Consommation	TOETS, STE Grenoble, HICOOL
Test des Mémoires SRAM	ASSOCIATE, NANOTEST, INFINEON, INTEL
Test des Mémoires Non-Volatiles	ATMEL, EMYR
Tolérance aux Fautes	LAFISI
Diagnostic Logique	STM Crolles A, STM Grenoble
Test des Circuits 3D	MASTER 3D

6 ACTIVITES D'ENSEIGNEMENTS

6.1 Bilan des heures d'enseignements

Le Tableau 1.7 fournit un bilan de la répartition des heures d'enseignements que j'ai effectuées depuis 1998 essentiellement aux niveaux Licence et Master dans le département EEA de la Faculté de sciences de l'Université Montpellier 2.

TABLEAU 1.7 RÉCAPITULATIF CHRONOLOGIQUE DES HEURES D'ENSEIGNEMENTS

	Monitorat	**Post-doc**	**Maître de Conférences**											
	98 - 01	01 - 03	03 - 04	04 - 05	05 - 06	06 - 07	07 - 08	08 - 09	09 - 10	10 - 11	11 - 12	12 - 13	13 - 14	**Total**
Cours		3	4	41	31	50	60	63	57	67,5	70,5	85,5	85,5	**618**
TD	30	67	137	106	125	122	85	76	115	101	111	82,5	82,5	**1240**
TP	252	122	107	77	32	28	41	32	54	64	28	17	28	**882**
hETD	198	151	214	218	192	215	202	202	255	266	245	228	238	**2824**

6.2 Détails des enseignements

Les enseignements que je dispense s'inscrivent dans les thématiques portées par la section CNU 61. Ils abordent la thématique de l'informatique industrielle : logique combinatoire et séquentielle, langage VHDL, architecture des calculateurs, modélisation GRAFCET, les réseaux de Petri et le test des circuits intégrés digitaux.

Pour l'ensemble de ces enseignements, je suis responsable de l'unité d'enseignement correspondante. J'ai donc produit les documents pédagogiques : les supports de cours, les exercices de TD et les sujets de TP. Pour le suivi pédagogique du programme des unités d'enseignements que je gère, j'assure les heures de cours, une partie des heures de TD et au minimum un groupe de TP chaque année.

6.2.1 Logique combinatoire et séquentielle

Ce module, dispensé au niveau L, aborde les points suivants :

- Rappels des fonctions logiques élémentaires.
- Notions de calcul, bases, compléments, opérateurs arithmétiques.
- Mémoires élémentaires.
- Les bascules (RS, latch, flip-flop et JK).
- Les registres et registres spécifiques.
- Les compteurs et décompteurs.

6.2.2 Langage de description matériel

Ce module, dispensé au niveau L et M, aborde les points suivants du langage VHDL

- Bases du langage : Librairies, entité et architecture.

- Descriptions comportementales et structurelles.
- Simulation et validation : « test-bench ».
- Les technologies de circuits reprogrammables.

6.2.3 Architecture des calculateurs

Ce module, dispensé au niveau L, aborde les points suivants :

- Principes de fonctionnement des machines de Von Neumann.
- Modes d'adressages.
- Décodeurs d'instructions câblés et micro-programmés.
- Systèmes d'interruptions.
- Les entrées / sorties.

6.2.4 Modélisation GRAFCET

Ce module, dispensé au niveau L, aborde les points suivants du GRAFCET :

- Définition de la norme : étapes, actions, transitions, réceptivités.
- Les structures classiques : sémaphore, communication.
- Les entrées-sorties.
- Les temporisations.
- L'implantation : règles et algorithmes d'évolution, équations logiques équivalentes.
- Les automates programmables industriels.

6.2.5 Réseaux de Petri

Ce module, dispensé au niveau M, aborde les points suivants des réseaux de Petri :

- Définitions du modèle réseau de Petri autonome et généralisé.
- Les structures.
- Les outils d'analyse.
- Propriétés de bon fonctionnement.

6.2.6 Test de systèmes intégrés digitaux

Ce module, dispensé au niveau M, aborde les points suivants :

- Les défauts de fabrication.
- Les modèles de fautes.
- La génération de vecteurs de test.
- La simulation de fautes.

- L’analyse de testabilité.
- La conception en vue du test.

6.3 Administration de l’enseignement

2004/2011	Correspondant TICE du département d'Enseignement EEA.
Depuis 2004	Responsabilité de modules d’enseignements en L et M.
	Tuteur pédagogique : 1 moniteur en 2004-2005 2 moniteurs en 2005-2006 3 moniteurs en 2006-2007 4 moniteurs en 2007-2008 6 moniteurs en 2008-2009 5 missions complémentaires d’enseignement et 1 ½ ATER en 2009-2010 5 missions complémentaires d’enseignement et 1 ½ ATER en 2010-2011 3 missions complémentaires d’enseignement et 1 ½ ATER en 2011-2012 3 missions complémentaires d’enseignement et 2 ½ ATER en 2012-2013 2 missions complémentaires d’enseignement en 2013-2014
Depuis 2005	Membre du bureau du département d'Enseignement EEA.
Depuis 2007	Responsable de la spécialité « Systèmes Microélectroniques » du Master EEA de l’université de Montpellier 2. Résultats 2007-2008 : 18 inscrits, 12 diplômés Résultats 2008-2009 : 14 inscrits, 13 diplômés Résultats 2009-2010 : 13 inscrits, 11 diplômés Résultats 2010-2011 : 12 inscrits, 10 diplômés Résultats 2011-2012 : 15 inscrits, 13 diplômés Résultats 2012-2013 : 11 inscrits, 7 diplômés Résultats 2013-2014 : 12 inscrits
Depuis 2010	Responsable de la première année du Master EEA de l’université de Montpellier 2. Résultats 2010-2011 : 96 inscrits, 68 diplômés Résultats 2011-2012 : 82 inscrits, 43 diplômés Résultats 2012-2013 : 89 inscrits, 65 diplômés Résultats 2013-2014 : 94 inscrits
Depuis 2012	Responsable adjoint de la mention Master EEA de l’Université Montpellier 2, 190 étudiants par an en moyenne.

7 RESPONSABILITES ADMINISTRATIVES

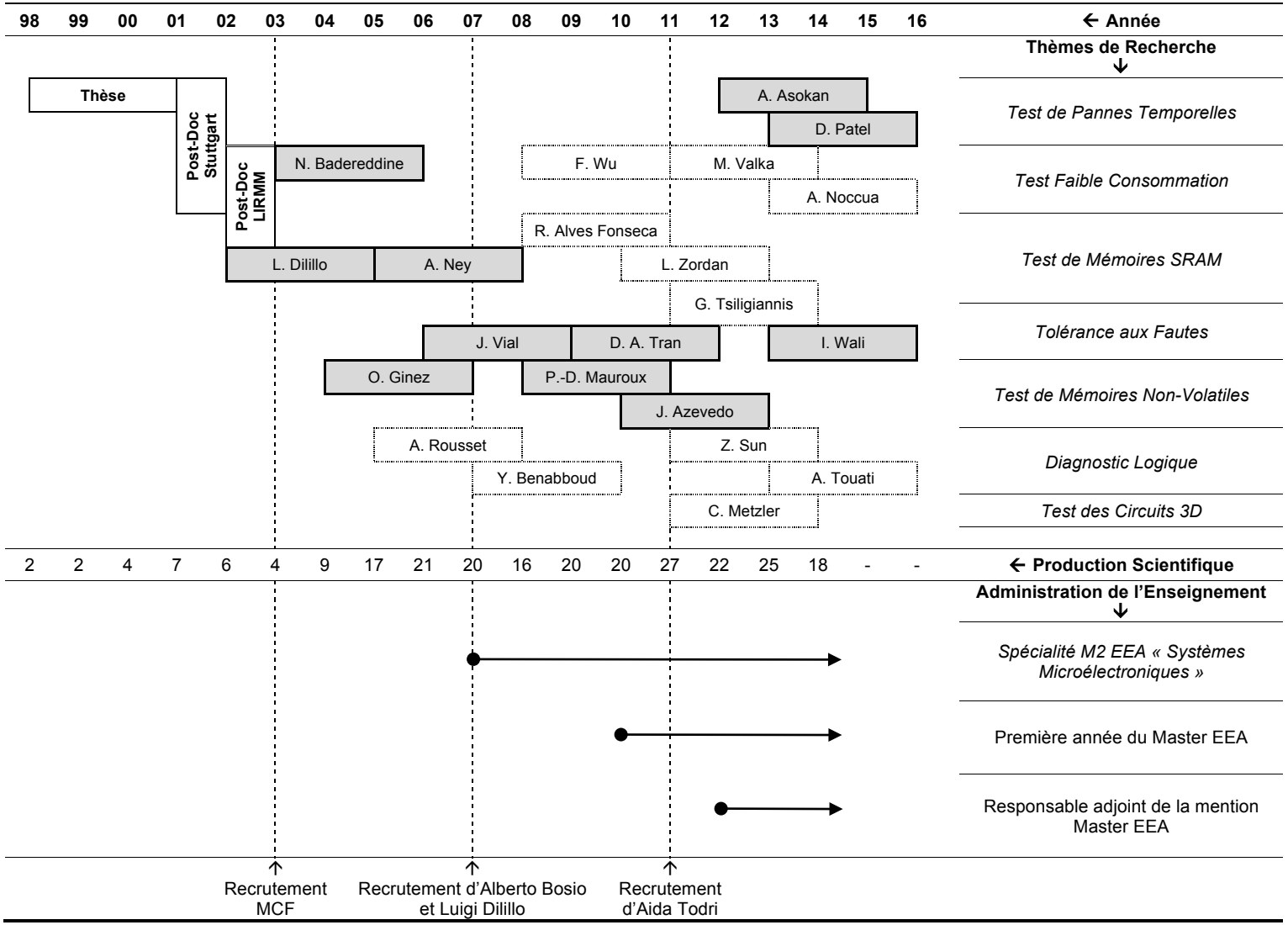
2007 – 2008	Administrateur permanent au conseil d'administration de l'université de Montpellier 2.
	Membre de la commission de spécialistes 61 de l'université Montpellier 2
Depuis 2009	Vice-président du pool d'experts, section 61, de l'université de Montpellier 2.
2007 – 2008	Membre du COPS (« Conseil d'Orientation Pédagogique et Scientifique ») du PFR (« Pôle Formation Recherche ») MIPS (« Mathématique, Informatique, Structures et Systèmes ») de l'université de Montpellier 2.
2011	Comités de sélection d'enseignants-chercheurs IUT Montpellier / Laboratoire LIRMM (section 61).
2013	Comités de sélection d'enseignants-chercheurs Polytech'Marseille / Laboratoire IM2NP (section 63).
Depuis 2014	Membre élu du CTE (« Comité Thématique d'Etablissement ») MIPS (« Mathématique, Informatique, Structures et Systèmes ») de l'université de Montpellier 2.

8 BILAN

Afin de dresser le bilan de mes activités de recherche et d'enseignement, le Tableau 1.8 regroupe les informations suivantes :

- Mon cursus : thèse de doctorat et contrats post-doctoraux
- Les encadrements de thèse, avec en grisé les thèses pour lesquelles j'ai été l'encadrant principal
- L'évolution de ma production scientifique (total de publication toutes catégories par année)
- Les prises de responsabilité dans l'administration de l'enseignement

TABLEAU 1.8 BILAN CHRONOLOGIQUE DES MES ACTIVITÉS DE RECHERCHE ET ADMINISTRATION DE L'ENSEIGNEMENT



PARTIE 2 : DÉVELOPPEMENT ET PERSPECTIVES

Cette seconde partie, rédigée en anglais, a pour objectif de détailler mes thèmes de recherche principaux et d'exposer mes perspectives pour les prochaines années.

1 INTRODUCTION

In this part of the document, main results of research topics I carried out are developed. They are all related to research activities I did and I supervised:

- Delay testing (my PhD thesis)
- Low power testing (one PhD supervised)
- Memory testing (five PhD supervised)
- Fault tolerance (two PhD supervised)

I conclude with the main contributions of my research activities and some ongoing works and future perspectives.

2 DELAY FAULT TESTING

At-speed testing is becoming an essential part of the verification process of today's VLSI circuits since it allows optimizing the test time and provides the means to test for delay faults. A delay fault occurs in a circuit when one or more paths in the circuit fail to propagate a signal within the time interval specified by the clock period. Detection of delay faults requires two-pattern tests. An initialization vector is applied and the circuit is allowed to stabilize. Then, the test vector is applied and the circuit outputs are sampled at clock speed. The response is then compared to that of the fault-free circuit to determine the presence or the absence of a delay fault.

Delay fault testing requires two pattern tests. *SIC* (Single Input Change) test sequences have been investigated in the literature. *SIC* test pairs are sufficient to detect all robustly detectable path delay faults, with a test length shorter than that required with *MIC* (Multiple Input Change) test pairs. This fact has motivated the development of *BIST* (Built-In Self-Test) techniques in which *SIC* test pairs are generated for testing delay faults.

My PhD thesis has been carried out in the field of delay fault testing. My work has focused on the definition of efficient test sequences for path delay fault testing. During my PhD thesis I addressed the following points:

- Highlight the fact that random sequences provide better fault coverage compared to pseudo-random sequences generated with an *LFSR* (Linear Feedback Sift Register).
- Interest of *SIC* sequences for delay fault testing in comparison with *MIC* sequences
- Effectiveness of *SIC* sequences with regards to stuck-at and bridging faults.
- Development of a hardware *SIC* generator with “good” random properties.

As example, Figure 2.1 presents the scheme of the hardware *SIC* generator I developed. It is composed of k-bit *LFSR*. Only m-bit (m<<k) of the LFSR are used as input of a mapping circuit. Such LFRS configuration improves the randomness of the generated test sequence. The 1-out-if-n output code is then used to invert the content of a T flip-flop. This functioning allows the generation of a *SIC* sequence.

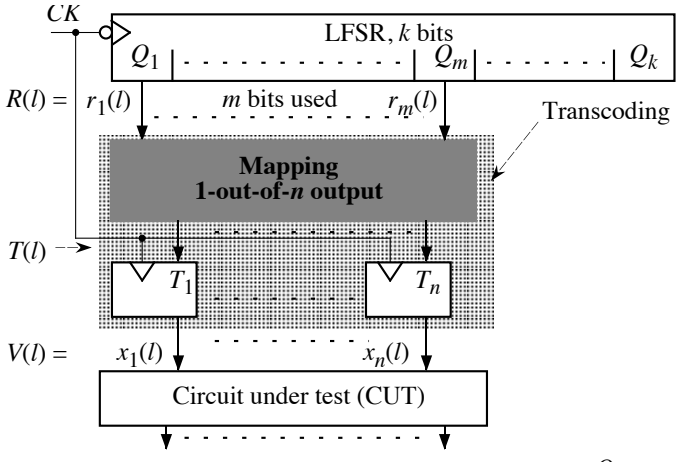


FIGURE 2.1 HARDWARE SIC GENERATOR

More details and results can be found in the fourth part of this report where I have attached the main journal paper I produced in this field (reference [RE4])

3 LOW POWER TESTING

While many techniques have evolved to address power minimization during the functional mode of operation, it is now mandatory to manage power during test mode. Circuit activity is substantially higher during test than during functional mode, and the resulting excessive power consumption can cause structural damage or severe decrease in reliability of the circuit under test. In the context of scan testing, the problem of excessive power during test is much more severe as the application of each test pattern requires a large number of shift operations that contributes to unnecessarily increasing the switching activity.

In this subsection, I present the main contributions carried out on low power testing. This work is related to the PhD thesis of Nabil Badereddine made in collaboration with Hans-Joachim Wunderlich from the University of Stuttgart. I first start by presenting peak power issues during scan testing in order to highlight the problem of an elevated peak power during the test cycle of the scan procedure. Then, I introduce the two approaches developed to target peak power reduction during the test cycle by reducing the activity at circuit inputs; the first one consists in reordering the scan cell and the other one is based on a specific X-filling heuristic.

Problem formulation

During conventional scan testing, each test vector is first scanned into the scan chain. After a number of load clock cycles, a last shift in the scan chain launches the test vector. The Scan Enable (*SE*) signal is disabled, thus allowing the test response to be captured/latched in the scan chain at the next clock pulse (see Figure 2.2). After that, *SE* is switched on, and the test response is scanned out as the next test vector is scanned in.

There can be a peak power violation (peak power exceeding a specified limit) during either the load/unload cycles or during the test cycle. In both cases, a peak power violation can occur because the number of flip-flops that change value in each clock cycle can be really higher than that during functional operation.

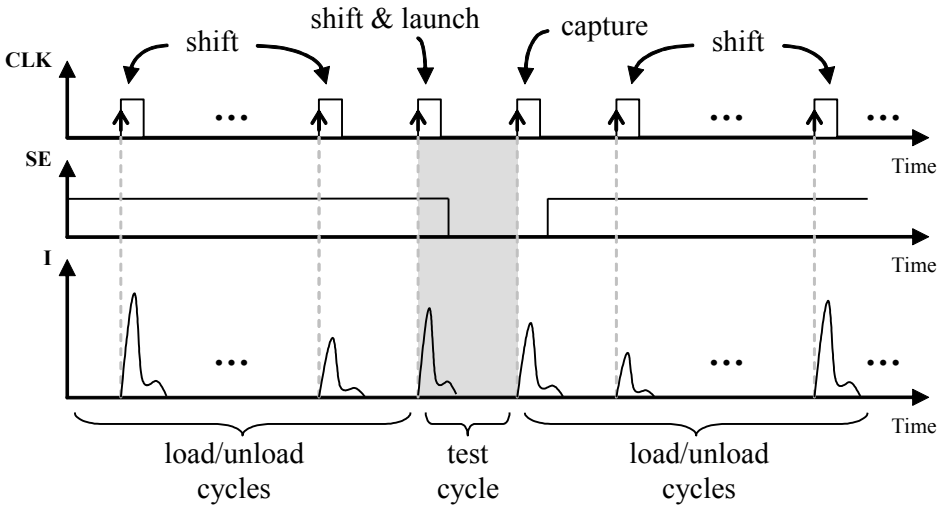


FIGURE 2.2 SCAN TESTING AND CURRENT WAVEFORM

It has been shown in the literature that even if peak power is higher during the load/unload cycles, peak power during the test cycle is in the same order of magnitude. This may lead to problematic noise phenomena during the test cycle. Let us consider the IR-drop phenomenon. It is due to a high peak current demand that reduces voltages at some gates in the circuit under test and hence causes these gates to exhibit higher delays. The gate delays do not affect the load/unload process as no value has to be captured/stored during this phase. Conversely, the gate delays can really affect the test cycle

because values of output nodes in the combinational logic have to be captured in the scan flip-flops. As this operation is generally performed at-speed, this phenomenon is therefore likely to occur during this phase and negatively impact test results and thus yield.

Scan cell reordering

Considering the fact that minimizing peak power during the test cycle is needed, we proposed a solution based on scan cell reordering. From the set of scan cells and a pre-computed sequence of deterministic test vectors, a heuristic process provides a scan chain order that minimizes the occurrence of transitions and hence the peak power during the test cycle.

We developed and implemented a heuristic solution based on Simulated Annealing (*SA*). The different steps performed by the *SA* heuristic are represented in the flow chart of Figure 2.3.

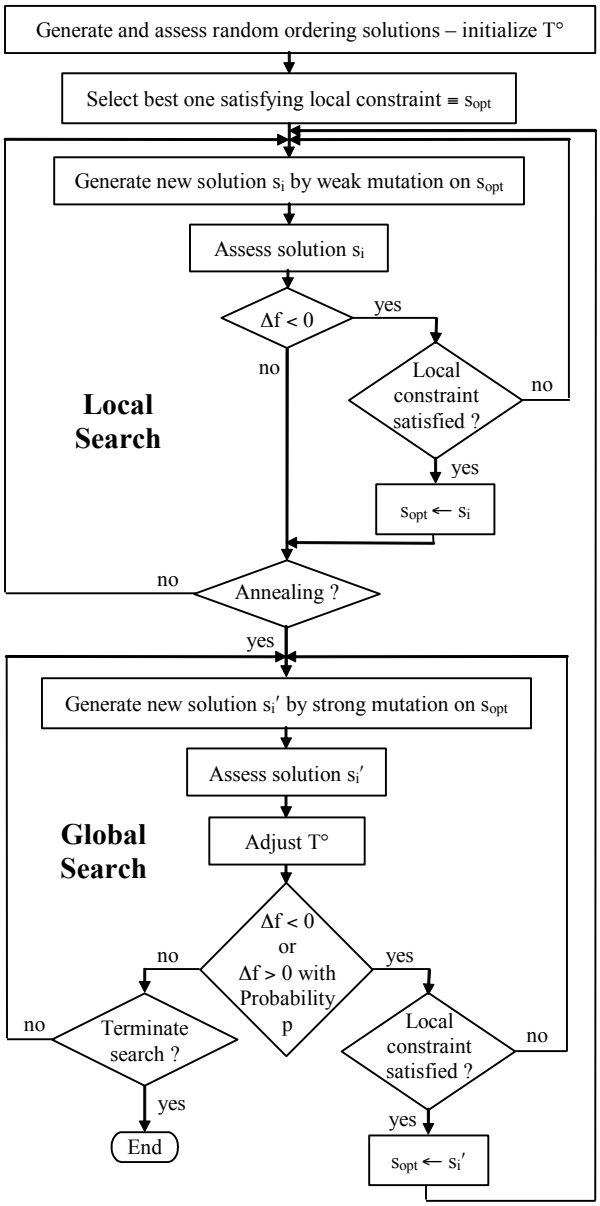


FIGURE 2.3 SCAN REORDERING FLOW CHART

Inputs to this algorithm are a set of scan-cells and the deterministic test vectors generated assuming a given order of these scan cells in the scan chain. The output is an ordered scan chain with minimum

peak power during the test cycles. The algorithm starts by randomly generating a set of solutions and select the best one S_{opt} that satisfies the local constraint. The best solution is the one with the lowest cost expressed as the number of bit differences over the entire test sequence. Then, the algorithm follows the two following main steps. First, a local search is made to find better solutions from the current optimum solution. Next, in order to escape from local minima, a global search is made in which solutions better than S_{opt} ($\Delta f < 0$) are accepted when the local constraint is satisfied, and solutions worse than S_{opt} ($\Delta f > 0$) can be accepted with a certain probability $p = \exp(-\Delta f / T)$. The temperature T is decreased during the search process so that the probability of accepting worse solutions gradually decreases.

For ISCAS'89 and ITC'99 benchmark circuits, the proposed approach reduces peak power during the test cycle up to 51% compared to an ordering provided by an industrial synthesis tool. Fault coverage and test time are left unchanged by the proposed solution

X-filling

In conventional ATPG, don't care bits (Xs) are filled in randomly, and then the resulting fully specified pattern is simulated to confirm detection of all targeted faults and to measure the amount of faults which where not explicitly targeted during pattern generation but were detected anyway. It is interesting to note that the fraction of don't care bits in a given pattern is nearly always a very large fraction of the total available bits. The significant fraction of don't care bits presents an opportunity that can be exploited for power minimization during scan testing.

In order to reduce peak power during the test cycle, the contribution of this work is to use a test generation process during which non-random filling is used to assign values to don't care bits (Xs) of each test pattern of the deterministic test sequence.

First, the Xs are assigned with the help of the following classical non-random filling heuristics:

- Adjacent filling also called *MT*-filling (Minimum Transition filling): all don't care bits in a pattern are set to the value of the last encountered care bit (working from left to right). When applying *MT*-filling, the most recent care bit value is used to replace each consecutive `X' values.
- 0-filling: all don't care bits in a pattern are set to '0'.
- 1-filling: all don't care bits in a pattern are set to '1'.

Second, the Xs are assigned with the help of the proposed Structural-Based power-aware X-filling (*SB*-filling) technique, which consists in assigning Xs according to structural information. Depending on the type of gates directly connected to the scan flip-flops, the Xs will be filled so as to block possible transitions in the combinational part of the circuit. Let us consider the circuit presented in Figure 2.4. In this example, gate *G1* has its two inputs directly fed by the scan chain while gate *G2* has only one input connected to a flip-flop.

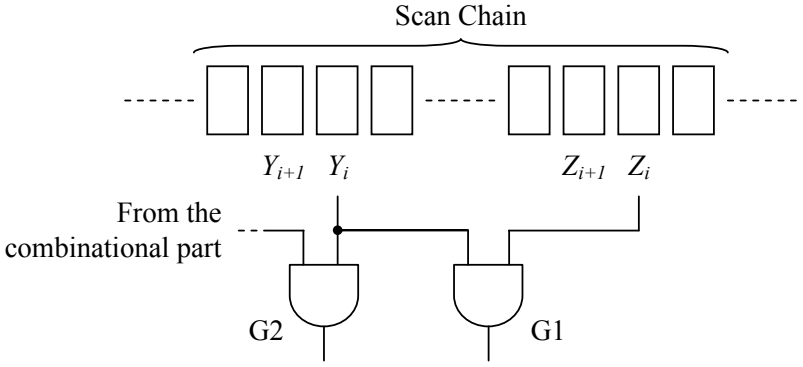


FIGURE 2.4 EXAMPLE OF GATES CONNECTED TO A SCAN CHAIN

In order to ensure the stability (no transition) of gate *G1*, we have to satisfy the following equation:

$$\overline{Y_i} \cdot \overline{Y_{i+1}} + \overline{Z_i} \cdot \overline{Z_{i+1}} + \overline{Y_i} \cdot \overline{Z_{i+1}} + \overline{Z_i} \cdot \overline{Y_{i+1}} + Y_i \cdot Y_{i+1} \cdot Z_i \cdot Z_{i+1} = 1$$

Each term of Eq. 1 corresponds to a succession of values at the inputs of the gate that guarantee its output's stability. The two first terms $\overline{Y_i} \cdot \overline{Y_{i+1}}$ and $\overline{Z_i} \cdot \overline{Z_{i+1}}$ correspond to a succession of two '0s' on the same input. The two following ones ($\overline{Y_i} \cdot \overline{Z_{i+1}}$ and $\overline{Z_i} \cdot \overline{Y_{i+1}}$) can also ensure the stability at the gate's output but may induce a glitch on the output. Finally, the last term $Y_i \cdot Y_{i+1} \cdot Z_i \cdot Z_{i+1}$ means that all the inputs stay at '1' in order to obtain a stable '1' at the gate's output.

Based on this equation and know values in the ATPG patterns, the problem was solved with the use of a greedy algorithm. Experiments performed on ISCAS'89 and ITC'99 benchmark circuits show that the *SB*-filling technique provides the best tradeoff between peak power reduction and increase of test length compared to classical X-filling solutions.

4 MEMORY TESTING

Semiconductor memories can be classified according to the type of data storage and data access mechanisms in three main families: the Read-Write Memories (*RWMs*), Read-Only Memories (*ROMs*) and Non-Volatile Read-Write Memories (*NVRWMs*). Figure 2.5 gives a schematic view of the various types of memories in each family.

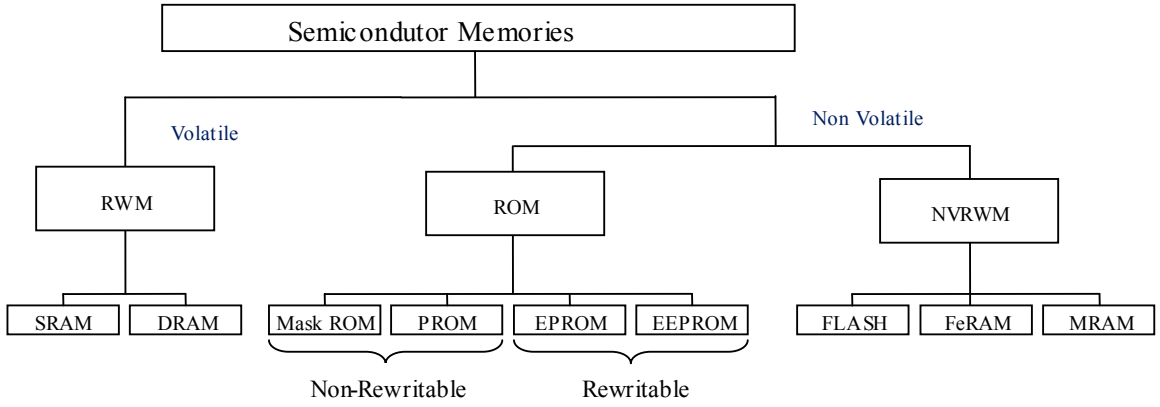


FIGURE 2.5 MEMORY TAXONOMY

For several current applications (audio, video, data processing), system performances are strictly related to the capacity (size) and speed of its memory elements. This is one of the main reasons of the memory predominance in embedded systems and System-on-a-Chip (*SoC*). Moreover, memories are designed to exploit the technology limits in order to reach the highest storage density and the highest access speed. The main consequence is that memory devices are statistically more likely to be affected by manufacturing defects. The importance of manufacturing test is also due to its impact on the final product cost. Since memories are becoming the main responsible of the *SoC* yield and represent a large percentage of the product cost, searching for efficient test and diagnosis solutions is mandatory for these devices.

In this context, I have addressed the test problematic of three memory technologies, *SRAM*, Flash and *MRAM*. Next sub-sections give an overview of main contributions in providing test and diagnosis solutions for these memory technologies.

4.1 SRAM Testing

Functional faults traditionally employed in SRAM testing, such as stuck-at, transition and coupling faults are nowadays insufficient to give correct models of the effects produced by some defects that may occur in VDSM technologies. Advances in process manufacturing densities and memory architectures have carried the development of new fault models, which are tightly linked to the internal memory structure. These faults are not directly detectable with standard March algorithms and thus they need specific test sequences and, in some cases, at-speed tests, which are necessary especially for delay fault detection.

In this subsection, I present the main contributions carried out on SRAM testing. This work is related to the PhD thesis of Luigi Dilillo and Alexandre Ney both in collaboration with Infineon Technology. I first start by presenting the methodology developed to analyze defects in SRAM blocks. As case study, I develop the test methodology of the sense amplifier. Then, I introduce the two approaches proposed for SRAM diagnosis.

Defect-based testing

Many links have been established between delay faults and resistive-open defects. Resistive-opens cause a timing-dependent behavior. A two-pattern sequence is usually necessary to sensitize the fault, but, in contrast with stuck-open faults, detection of resistive-opens should be performed at-speed. The significance of resistive-opens has considerably increased in recent technologies, due to the presence of many interconnection layers and an ever-growing number of connections between each layer. Hence resistive-open defects were the main target of this study. Resistive defects have been injected in different block constituting an embedded-SRAM (core-cell, pre-charge circuitry, sense amplifier and write driver) with the main purpose of verifying the presence of timing-dependent faults.

For each block of an SRAM we have adopted the following methodology:

- Structural description and corresponding fault-free electrical behavior,
- Detailed electrical analysis of resistive defects inducing a faulty behavior,
- Functional fault modeling of resistive defects leading to dynamic faults,
- Dedicated March-based test strategies with the corresponding complexity evaluation.

As case study, I developed in the following the analysis of resistive-open defects in sense amplifiers of SRAMs.

An I/O circuitry, composed by write drivers and sense amplifiers, is used to control or observe the true bit line (BL) and the complement bit line (BLB) during the write and read operations of a given core-cell. A global view of the I/O circuitry is presented in Figure 2.6.a in which I have only represented sense amplifiers for the sake of clarity.

A BL couple is selected by the signal SEL_{BLx}. During a read operation, the bit line voltage levels of selected columns are propagated towards each SA_i and SAB_i nodes ($0 \leq i \leq k$). Then, the sense amplifier corresponding to the targeted core-cell is activated by its signal $SAON_i$ (all the others remaining off). The outputs z_i and zb_i of this sense amplifier control the data output circuitry. This block generates the output data (*Data_out*). The transistor view of the considered sense amplifier is presented in Figure 2.6.b. Before every read operation, BL and BLB are pre-charged at Vdd. The sense amplifier nodes (*SA* and *SAB*) are also pre-charged at Vdd by their own pre-charge circuits. A read operation begins with the selection of the targeted core-cell. This access time allows one of the two bit lines to be discharged of about 100mV.

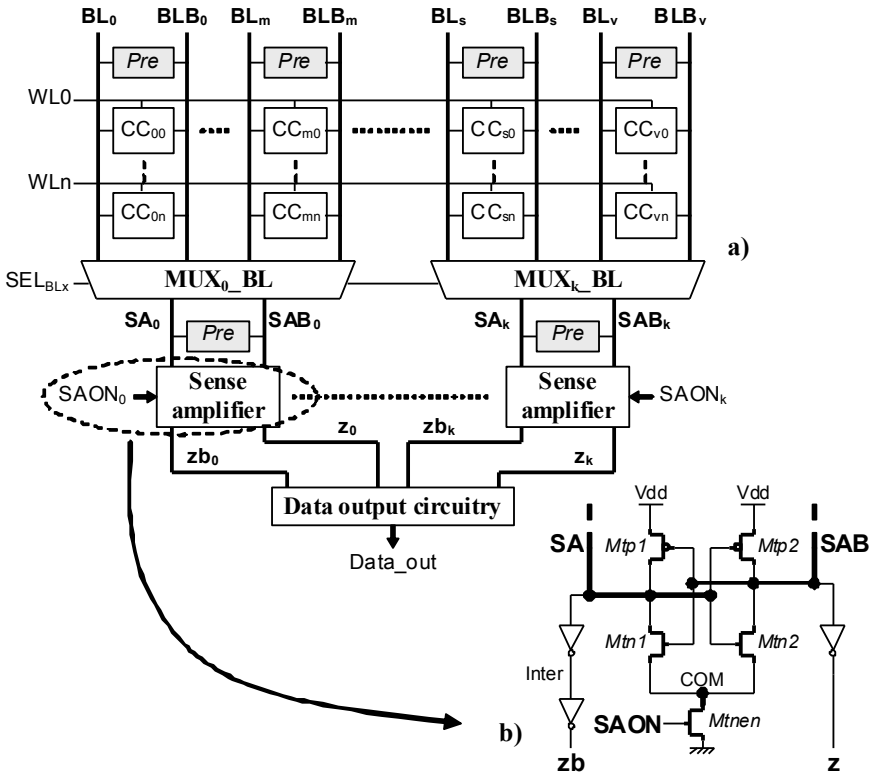


FIGURE 2.6 I/O CIRCUITRY A) GENERAL SCHEME AND B) SENSE AMPLIFIER SCHEME

The second step consists in activating the sense amplifier in order to translate this weak differential voltage between BL and BLB ($\Delta BL = BL - BLB = SA - SAB$) in a full swing differential signal, which is then interpreted as a digital signal by the data output circuitry. In summary, for a read performed on a core-cell belonging to the group i ($0 \leq i \leq k$) of core-cells controlled by the same sense amplifier, we have:

- for a r0: $SA_i = 0$, $SAB_i = 1$ and $z_i = 0$, $zb_i = 0$
- for a r1: $SA_i = 1$, $SAB_i = 0$ and $z_i = 1$, $zb_i = 1$

As shown in Figure 2.7, nine resistive-open defects have been placed in different locations of the sense amplifier.

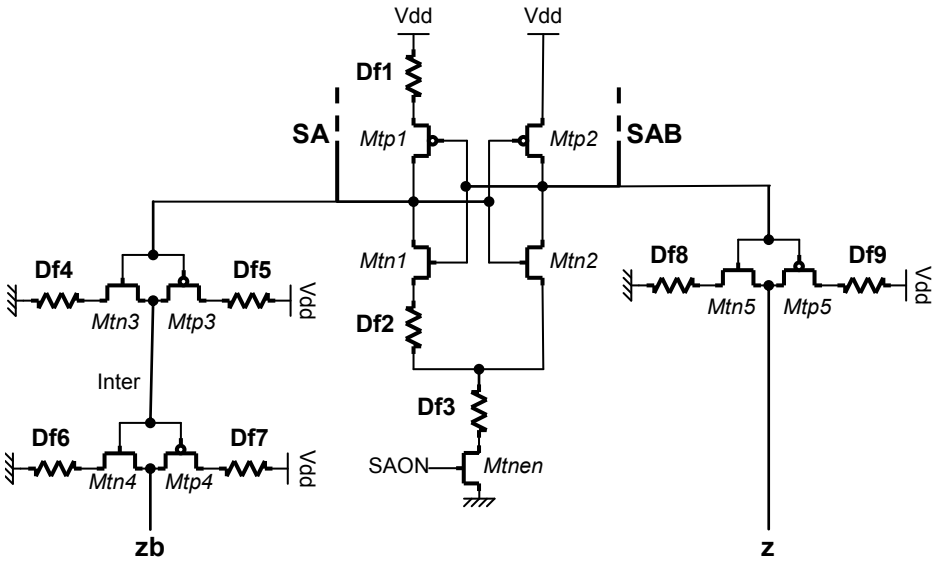


FIGURE 2.7 DEFECT INJECTION IN THE SENSE AMPLIFIER

The whole operating environment range has been examined with the aim of determining test conditions, which maximize the fault detection. Hence, simulations have been performed by varying the following parameters:

- Process corner: slow, typical, fast, fn/sp, sn/fp
- Supply voltage: 1.08V, 1.2V, 1.32V
- Temperature: - 30°C, 27°C, 110°C

Table 2.1 presents a summary of fault models identified for each injected resistive defect, along with conditions for maximum fault detection.

TABLE 2.1 RESULTS SUMMARY

Defect	Fault Model	Min Res (kΩ)	Process corner	Voltage (V)	Temp (°C)
Df1	-	-	-	-	-
Df2	IRF	0.35	Fast	1.32	-30
Df3	d2cIRF1	1.8	Fast	1.32	-30
Df4	d2cIRF2	140	Slow	1.08	-30
Df5	d2cIRF2	20	Fast	1.32	-30
Df6	d2cIRF2	15	Fast	1.32	-30
Df7	d2cIRF2	150	Fast	1.32	110
Df8	d2cIRF2	140	Slow	1.08	-30
Df9	d2cIRF2	20	Fast	1.32	-30

Definitions of fault models are the following:

- Incorrect Read Fault: a core-cell is said to have an IRF if a read operation performed on it returns an incorrect logic value.
- dynamic two-cells Incorrect Read Fault of type 1: a sense amplifier is said to have a d2cIRF1 if it is unable to read any value. The read data value is the one previously stored in the data output circuitry.
- dynamic two-cells Incorrect Read Fault of type 2: a sense amplifier is said to have a d2cIRF2 if it is only able to perform a r0 or r1 operation.

As shown in Table 2.1, *Df1* does not involve any faulty behavior. *Df2* involves an IRF, which are detected by standard March tests. Finally, a d2cIRF1 is observed in presence of *Df3* and a d2cIRF2 has been obtained for *Df4*, *Df5*, *Df6*, *Df7*, *Df8* and *Df9*.

Hereafter, electrical simulations of the sense amplifier are detailed. Waveforms in Figure 2.8 present the faulty behavior of the memory in presence of *Df3*. This simulation reports the behavior of two different core-cells (CC_A and CC_B) belonging to the same group of columns (*i.e.* sharing the same sense amplifier) with CC_A containing a logic '0', CC_B a logic '1' and the data output circuitry (*DataOut*) initialized at a logic '0'.

A r0 operation is first applied on CC_A. The fault is not observed as the read data (a logic '0' in this case) is the same than that initially stored in the data output circuitry. Then, a second read operation is performed with a r1 on CC_B. The data output circuitry remains in a memory state, implying that it still provides a logic '0' instead of a logic '1'. The fault is therefore sensitized and observed during the second read operation.

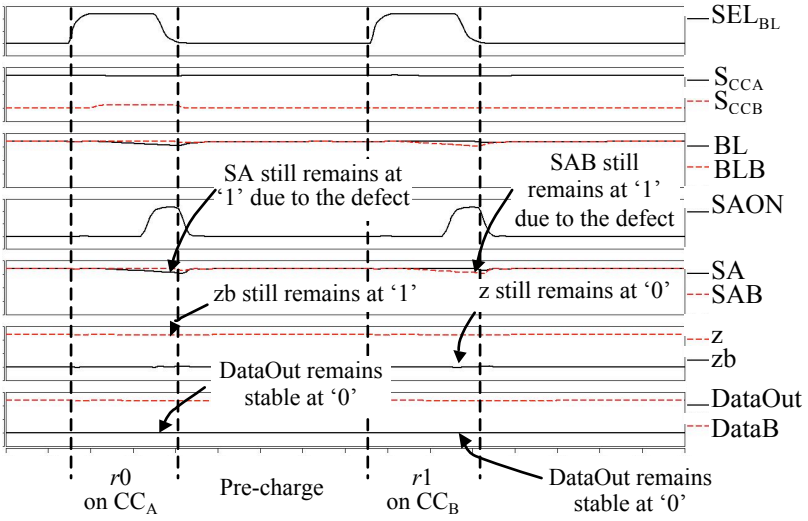


FIGURE 2.8 WAVEFORMS OF FAULTY BEHAVIOR

The detection of d2cIRFs requires a specific sequence of read operations. In this study, we have proven that March C- with an alternating data background (the particularity to perform each read/write operation with an alternated data value) is able to detect all d2cIRF that may affect SRAM sense amplifier.

Effect-cause Diagnosis

Fault detection, diagnosis and localization are extensively used to repair manufacturing defects in memories and improve the product quality, reliability and yield. Traditional techniques for memory repair consider identification of fault type and fault location as two separate phases. For repair purposes, the identification of the exact location of the detected fault is more important than the information on the type of fault. In particular, the mapping of the faulty cells allows the use of the spare columns and rows. Conversely, diagnosis approaches targeting yield ramp-up require the identification of the cause of the failure as well as its location.

As soon as the application of March algorithms has revealed logic errors in a given memory, diagnosis can be performed. Generally, diagnosis approaches for memories are based on a signature analysis and the Diagnosability Ratio (*DR*) is a parameter used to measure the quality of a diagnostic algorithm. Diagnostic methods generally resort to a fault dictionary (cause-effect or signature-based diagnosis) and try to achieve the highest *DR* for a given test algorithm. However, signature-based diagnosis methods present two main drawbacks. First, as they use a fault dictionary, the possible fault models affecting the memory must be known before running the diagnosis procedure. Consequently, if a memory is affected by a fault not considered in the fault dictionary, the diagnosis phase fails to provide any result or may provide a wrong response. Secondly, most of the existing signature-based solutions target only the diagnosis of static faults.

In this work, we proposed a new diagnosis approach that represents an alternative to signature-based approaches. This new diagnosis technique is based on the effect-cause paradigm already developed for logic design diagnosis. It consists in creating a database containing the history of operations (read and write) performed on those core-cells, where read operations have returned faulty logic values, during the test phase. This information is crucial to track the root cause of the observed faulty behavior and is used to generate the set of possible Fault Primitives representing the suspected fault models.

The principle of the history-based diagnosis is based on the collection of two types of relevant information: i) the faulty responses provided by the tester and ii) the record of the sequence of preceding operations performed on the core-cells where read operations have returned faulty logic

values during the test. With this information, a set of Fault Primitives (*FPs*) is generated. As can be seen in Figure 2.9, the proposed diagnosis solution requires three inputs:

- Memory Architecture: this input provides information related to the tested memory in terms of dimension (number of row and columns), I/O organization and other information about the structure.
- March Test Specifications: this input provides information on the applied test algorithm in terms of sequence of operations performed on the memory and addressing order (row after row, named 'fast R', column after column, named 'fast C',…).
- Tester Report: this input provides information about the results of the test. For each observed error, this report indicates which is (are) the read operation(s) that reveal the fault and the corresponding core-cell address.

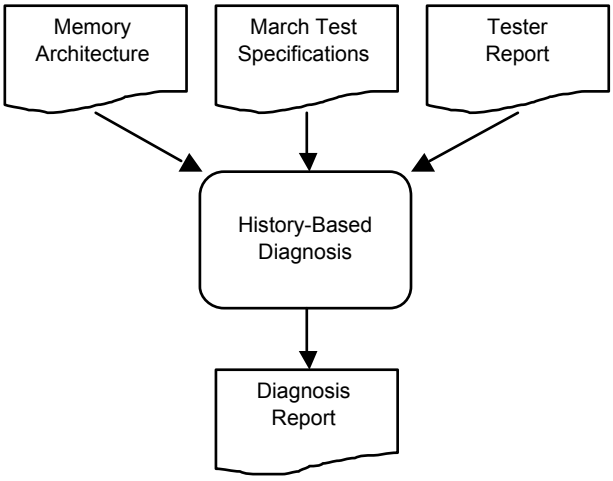


FIGURE 2.9 HISTORY-BASED DIAGNOSIS PRINCIPLE

In our experiments, we have considered several fault models for which we have applied the signature-based and history based diagnoses. Table 2.2 presents the results given by both solutions. The first and second columns give the fault model injected (*FMod*) and its location (*Location*) in the memory. Column 3 specifies the applied test algorithm and the addressing order used during the test application (*Test*). The last two columns give the diagnosis report with the two approaches, *i.e.* signature-based (*SB*) and history-based (*HB*) diagnosis.

TABLE 2.2 SIGNATURE VS. HISTORY-BASED DIAGNOSIS

FMod	Location	Test	SB	HB
SAF1	$CC_{99,3}$	March C-, *fast C*	**SAF1** IRF RDF	**SAF1,** IRF RDF
TF0	$CC_{123,12}$	March C-, *fast C*	**TF0**	**TF0**
dRDF	$CC_{99,3}$	March C-, *fast R*	SAF0 TF1 RDF IRF	SAF0, TF1 RDF, IRF **dRDF**
URWF	WD $C_{0\ to\ 3}$	March C-, *fast C*	SAF1 IRF RDF	SAF1, IRF, RDF **URWF**

Such history-based diagnosis approach offers many advantages. It does not require the a priori knowledge of the set of fault models targeted by the test algorithm because it does not rely on an established fault dictionary. It does not suffer from an additional limitation of signature-based approaches with respect to the treatment and storage of large data volume. Moreover, this method is able to perform the diagnostic of both static and dynamic faults and provides a better *DR* compared to signature-based diagnosis approaches. Another feature of the proposed history-based approach is its

capability to provide accurate and reliable information on the fault location. This is imposed by the fact that some fault models can be related to multiple possible electric causes, leading to a difficult location of the faulty memory component (address decoders, core-cells, sense amplifiers, write drivers…).

Design for diagnosis

The overall objective of this work is to provide a mean to identify which block of a memory (core-cell array, write drivers, address decoders, pre-charge circuits, etc …) is defective. Even if around 80% of the silicon area of a memory is taken by the core-cell array, which is hence more prone to defects than any other block, providing such type of information can save considerable amount of time during the ramp up phase in case of a malfunction coming from outside the core-cell array. A first step in this work is to diagnose faulty write drivers by proposing very low cost *DfD* (Design-for-Diagnosis) solutions.

A typical write driver operation consists in pulling-down one of the two bit lines of a given cell depending on the write operation type (w0, w1) while maintaining the other bit line at Vdd. The resulting voltage levels on bit lines during a write operation are a good indicator of the write driver correctness and reliability. The proposed *DfD* solution allows verifying voltage levels on both bit lines during write operations. This operation can be done during the diagnosis phase and can easily determine the defective write driver (if any) in the memory. This solution allows saving a considerable amount of time during the ramp up phase in case of a malfunction coming from a defect in one of the write drivers. Moreover, proposed diagnosis solution is also able to determine weak write drivers. A weak write driver is a driver that may act a write operation correctly even if it does not drive the correct voltage levels on both bit lines. Although such a weak driver will not be identified during the test phase, it may impact the reliability of the whole memory as a malfunction can manifest after a certain amount of time during the lifetime of the memory.

The hardware implementation of the developed *DfD* is presented in Figure 2.10. It is composed of two parts; the analog structure and the data processing providing the diagnosis result. The analog structure is designed in order to obtain less than Vdd/2 on *BL* and more than Vdd/2 on *BLB* for a fault-free w0 operation. The data processing part allows translating these analog levels into a digital signal. Two inverters are used to amplify the signals and a XOR gate is used to provide the diagnosis results. Node *S* must be at logic ‘1’ during the write operation in case of a write driver satisfying the analog conditions.

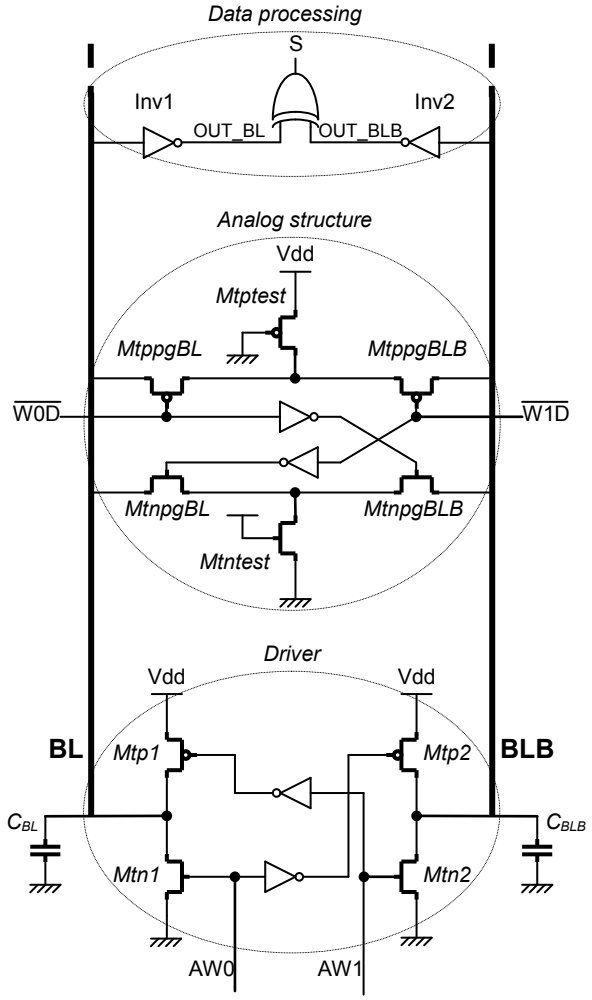


FIGURE 2.10 HARDWARE IMPLEMENTATION OF THE DIAGNOSIS MODULE

We have shown that the proposed *DfD* solution must be designed depending on voltage levels on bit lines that have to be measured and requires an activation sequence of only three write operations. The proposed hardware solution has a low impact on the area overhead (about 0.5% for a 512x512 *SRAM*). Beside diagnosis, an additional interest of such a solution is its usefulness during a post-silicon characterization process, where it can be used to extract the main features of the write drivers (logic and analog levels on bit lines). This type of information is particularly useful for high safety applications, such as automotive or medical applications.

For more details, I have attached in the fourth part of this report one of the main journal paper I produced in this field (reference [RE5]).

4.2 Non-Volatile Memory Testing

4.2.1 Flash Testing

Flash memory is a non-volatile memory that allows programming and erasing memory data electronically. The mainstream operation is based on the floating-gate concept in which charges can be stored and removed. Its low-power consumption and high integration density make it popular for portable devices. Two types of array can be used to realize a Flash memory: NOR and NAND-based arrays.

In this sub-section, I develop the main contributions carried out on NAND-Flash architectures. This work is related to the PhD thesis of Pierre-Didier Mauroux and done in collaboration with ATMEL. I first start by describing the principle of the Spice model developed. Then, I demonstrate the practicality of the model for guiding the design and test phases of NAND-Flash. Related to test, I present results of a comprehensive analysis for actual resistive defects (open and short) that may affect the NAND-Flash array. Then, I utilize the Spice model to propose a test solution to detect oxide thickness variations. These analyses highlight the practicality of the proposed model to provide a realistic set of fault models that have to be tested, thus enhancing existing solutions for Flash testing. The other main advantage of the proposed Spice model is its ability to help the design phase of the NAND-Flash. This is demonstrated by using the model to predict the behavior of the Flash memory with technology scaling. Then, the model is used to characterize the pulse programming method. This programming method consists of applying a sequence of incremental pulses starting from a low to high programming voltage allowing to reduce and control the stress of the transistor silicon oxide.

SPICE modeling

The NAND-Flash core-cell is based on the Floating Gate (*FG*) concept where the Fowler-Nordheim (*FN*) tunneling effect is used for charge injection or removal. A cross section of a single NAND string is shown in Figure 2.11.a. It is composed of two Select-Transistor (SG_1 and SG_2) and a *FG*-transistor.

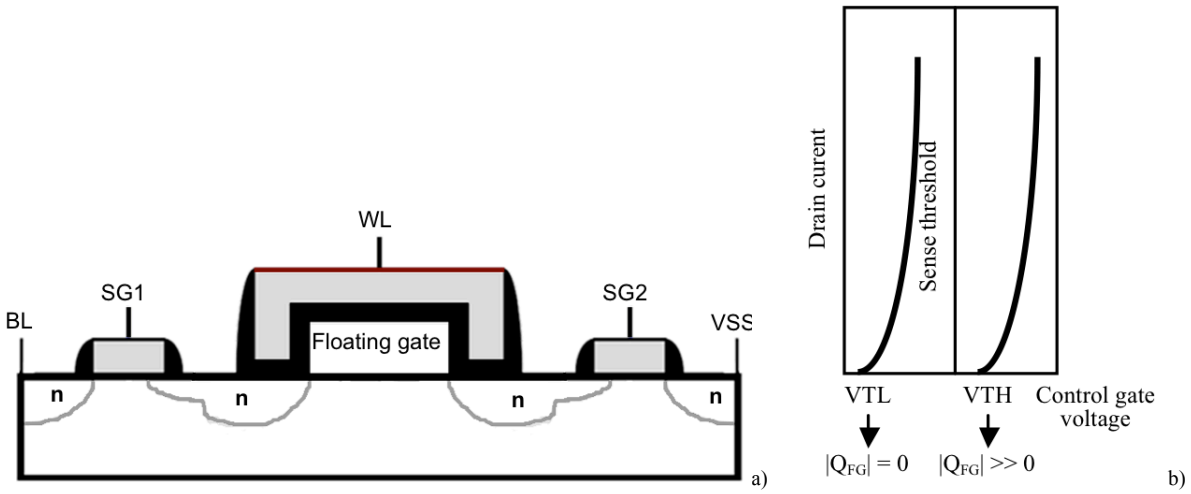


FIGURE 2.11 NAND-FLASH FUNCTIONING A) CROSS SECTION OF SINGLE NAND STRING AND B) VT MODULATION WITH CHARGE QUANTITY

Three different operations can be performed on a NAND-Flash: Erase, Write and Read. The Erase operation consists in removing charges from the *FG*. The erase operation is performed simultaneously on all core-cells within the same string and the same page and not on a single core-cell for structural reason. At the end of the erase operation, the Vt of the *FG*-transistor has a low value denoted *VTL*. From a functional point of view, *VTL* corresponds to logic '1'. The write operation consists in injecting electrons into the *FG*. Under this operation, charges injected into the *FG* change the Vt from

a low to a high Vt (*VTH*) that corresponds to logic '0' (see Figure 2.11.b). For the read operation, the core-cell is selected and a sense amplifier, working in current measurement mode, performs the data sensing. During the read operation, if the *FG*-transistor has a *VTL*, a current passes through the bit-line and the sense amplifier returns logic '1' on its output. Otherwise, if the FG-transistor has a *VTH*, there is no current through the bit-line and the sense amplifier returns logic '0' (see Figure 2.11.b).

The Spice model of the NAND-Flash memory developed to represent the Erase, Write and Read operations is made of two layers: a functional and a programming layer. Figure 2.12.a presents the functional layer where blocks K_i represent the coupling factors due to different capacitances as follows:

$$K_G = \frac{C_{ONO}}{C_{TOT}} \text{ and } K_C = \frac{C_{OX}}{C_{TOT}}$$

where C_{ONO} and C_{OX} are the *ONO* (Oxide-Nitrite-Oxide) and tunnel oxide capacitances, respectively. Moreover, C_{TOT} represents the total capacitance of the *FG*-transistor. This capacitance is used to store the charge provided by the block *FN* representing the Fowler-Nordheim tunneling effect. This block is modeled as current source in a Spice block that follows this equation:

$$I_{FN} = A \times \alpha \times E_{ox}^2 \times \exp\left(\frac{-\beta}{E_{ox}}\right)$$

with:

A: Tunnel area
α : Fowler-Nordheim constant
Eox: Oxide electric field
β: Fowler-Nordheim constants

Then, these three effects (block *Sum*) are sum to control the gate of an NMOS transistor representing the *FG*-transistor. The voltage, *Vfg* represents the equivalent floating gate voltage (*i.e.* the threshold voltage) of a core-cell under the Fowler-Nordheim and capacitive coupling effects.

The functional layer as shown in Figure 2.12.a is controlled by the programming layer, which is able to determine the channel voltage level (*Vchan*). Note that *Vchan* controls the electric field during erase and write operations. For this purpose, the solution proposed implies of using the capacitive modeling of the *FG*-transistor and add two select gates to modulate the Vchan level. Figure 2.12.b illustrates the equivalent electric schematic of the programming layer.

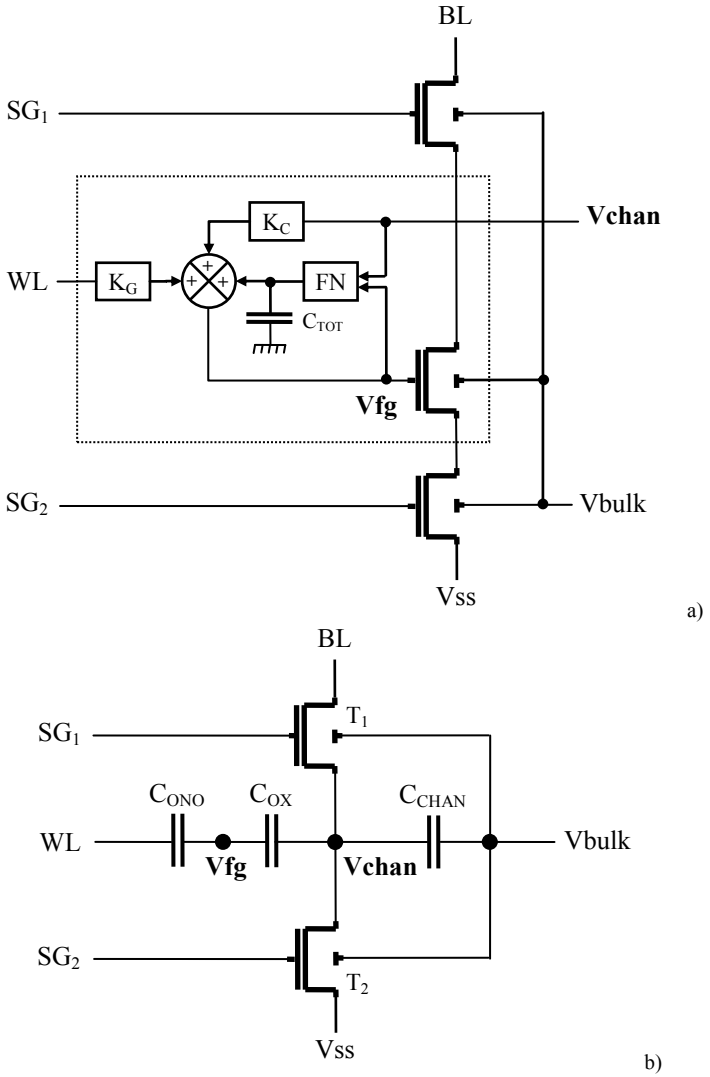


FIGURE 2.12 PRINCIPLE OF THE SPICE MODEL WITH A) FUNCTIONAL LAYER AND B) PROGRAMMING LAYER

NAND-Flash Testing

Here after, I present the usage of the developed Spice model for defect analysis especially for the case of resistive-open defects and impact of the oxide thickness variations.

Employing the Spice model, we performed a complete analysis of resistive defects (open and short) that may affect the NAND-Flash array. Figure 2.13 represents the ten resistive defect locations on a hypothetical 4x4 NAND-Flash memory array where each *FG*-transistor has been represented with the proposed Spice model.

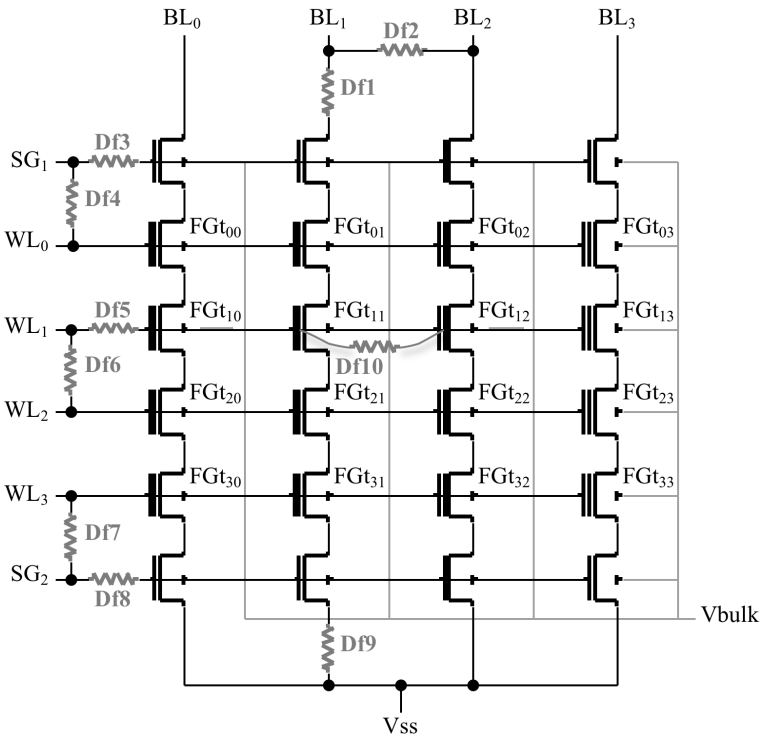


FIGURE 2.13 RESISTIVE DEFECT LOCATION IN A 4X4 FLASH MEMORY ARRAY

For each defect location, a set of electrical simulation was performed with different Erase/Write/Read sequences and defect sizes. As case study, Figure 2.14 presents the Vt level and bit-line current observed in presence of the defect *Df2*. Based on these waveforms we can analyze the defect impact on the NAND functioning during programming and read operations.

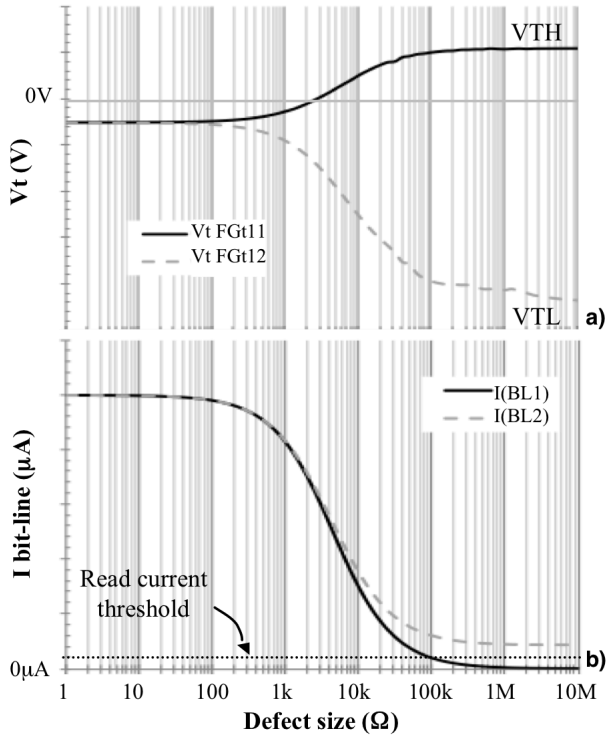


FIGURE 2.14 SIMULATION RESULTS OF THE DEFECT INJECTION A) VT VALUES AND B) BIT-LINE CURRENTS

Based on these simulations, observe fault behaviors were modeled with respect to the memory test literature. Table 2.3 summarizes the different fault models associated to each resistive defect and targeted *FG*-transistors with respect to the simulated NAND-Flash memory array. In this table, we also report the defect size thresholds at which these faulty behaviors occur.

TABLE 2.3 FAULT MODELING SUMMARY

Defect	Size (Ω)	Fault model
Df1	> 150 k	**SAF0** of all FG-transistors of the defective bit-line
Df2	< 200 k	**SAF1** of the written FG-transistors sharing one of the two shorted bit-lines
Df3	∞	**SAF0** of all FG-transistors
Df4	< 450 k	**SAF0** of all FG-transistors
Df5	-	No effect
Df6	10 k < … < 100 k	**SAF1** of the written FG-transistors sharing one of the two shorted word-lines
	< 10 k	**SAF0** of all the other FG-transistors sharing the two defective word-lines
Df7	< 300 k	**SAF0** of all FG-transistors
Df8	∞	**SAF0** of all FG-transistors
Df9	> 70 k	**SAF0** of all FG-transistors of the defective bit-line

The gate oxide is also an important parameter of the Flash memory since it insures the correct erase and write operations. It has also an important impact on the charge retention of *FG* (defined as the time that the *FG* can keep enough charges – typically 10 years) and also on the Flash endurance (defined as the number of programming cycle that the oxide can endure before its degradation - typically 100k cycles for an Flash).

The natural aging of the oxide impacts the Flash endurance. The observed phenomenon, referred as "cycling", shows the progressive degradation of the *VTL* level. Such problem is typically related to the hole generation and trapping caused by a high number of electric stresses of programming phases. Such aging phenomenon must be taken into account for computing Flash endurance and requires specific prediction models.

The retention of charges into the *FG* is an important reliability factor of the Flash technology. Even if the aging of the oxide may affect the retention of charges into the *FG*, the oxide thickness variation still remains the main source of retention problem after the manufacturing process. Two extreme cases must be considered: wide and small oxide thickness variations.

Wide oxide variations are easily observed during Flash operation. In the case when oxide thickness is too high, there is no charge injection/removal into/from the *FG*. The cell remains close to its default state with a standard threshold voltage. On the other hand, a short between FG and the channel provides a very good bit programming but there is no data retention because *FG* is not isolated. These two cases are extreme and are easily detected as erase and/or write operation fails.

The problem can be much more severe when there is only a small variation of the oxide thickness ($+\Delta ox$ or $-\Delta ox$), which is highly probable to occur due to process dispersions in VDSM technologies. When the variation is positive ($+\Delta ox$), the electric field is small and less charges are injected or depleted into the *FG*. The VT Window (*VTW*) is affected but there is no impact on the data retention and memory endurance. The *FG*-transistor affected by this variation works correctly as long as the variation allows a large enough *VTW*. If the *VTW* becomes too small, then the erase and/or write operations fail, thus making their detection quite easy. In the case of a negative variation ($-\Delta ox$), there is a good *VTW* as charge injection (or removal) into the *FG* performs better, but with a bad charge retention. This implies that the duration of the stored information is not maximal. Moreover, a little $-\Delta ox$ variation can increase oxide stress, thus affecting the endurance of the FG-transistor. In this case, as the FG-transistor works correctly, the only way to control such variation is by measuring the *VTW* of all the FG-transistors in the array. This can be done in characterization phase (test of margins) of the Flash by using analog resources. But in production test, this method is not feasible due to

economical reasons. Thus, a test solution targeting only functional operations (*i.e.* erase, write and read) needs to be developed in order to detect such possible defective oxide thickness.

The test solution proposed to avoid any characterization phases consists in varying the inhibition voltage on non-selected bit lines. The inhibition voltage applied on the non-selected bit lines disables the electric field and consequently, the write operation. To illustrate such behavior, electrical simulations were performed with the help of the proposed Spice model. Table 2.4 reports results of the read operation performed on the non-written *FG*-transistor (*FGt01*) after the write operation is performed on *FGt00*. Both *FG*-transistor are chairing the same WL. Results are shown for different values of the oxide thickness of *FGt01* and applied inhibition voltages. Results are reported with *PASS* and *FAIL* terms where:

- *PASS*: the read operation on *FGt01* returns logic '1' - expected value.
- *FAIL*: the read operation on *FGt01* returns logic '0' - non expected value.

TABLE 2.4 RESULTS OF THE READ OPERATION ON THE NON-WRITTEN FG-TRANSISTOR

		Applied voltage on the non-selected bit line					
		Nominal	-0.3v	-0.7v	-1v	-1.3v	-1.7v
Oxide Thickness (Å)	-21	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
	-18	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
	-15	PASS	FAIL	FAIL	FAIL	FAIL	FAIL
	-12	PASS	PASS	FAIL	FAIL	FAIL	FAIL
	-9	PASS	PASS	PASS	FAIL	FAIL	FAIL
	-6	PASS	PASS	PASS	FAIL	FAIL	FAIL
	-3	PASS	PASS	PASS	PASS	FAIL	FAIL
	Nominal	**PASS**	PASS	PASS	PASS	PASS	FAIL

One observation from these results is that the read operation on *FGt01* is correctly performed (*PASS* in bold in Table 2.4) for nominal oxide thickness and applied voltage values as expected. In addition, it can be observed that the read operation becomes *FAIL* for an important negative oxide thickness variation (-18 Å). By reducing the inhibition voltage we enable the detection of small negative oxide thickness variation. In such case, the write operation performed on *FGt00* is also performed on *FGt01*.

Others analyses have been performed for capacitive defects and defects in the Flash peripheral circuits. All these works have allowed us to define the set of fault model that must be targeted by the test algorithm.

NAND-Flash Design and Characterization

Another important advantage of the Spice model is its ability to predict the behavior of the Flash memory with technology scaling. Let us consider a single core-cell string, the model is able to consider the coupling capacitances between *FG*-transistors and *SG*-transistors, denoted as lateral coupling. This coupling is due to capacitances between the gate of *SG*-transistors and the *FG* of *FG*-transistor at the poly-silicon layer.

Electrical simulations were performed with the proposed model and data are reported in Figure 2.15. These waveforms show Vt levels achieved after Erase and Write operations on the *FG*-transistor for different values of the lateral coupling space between poly-silicon of *FG*-transistor and *SG*-transistors.

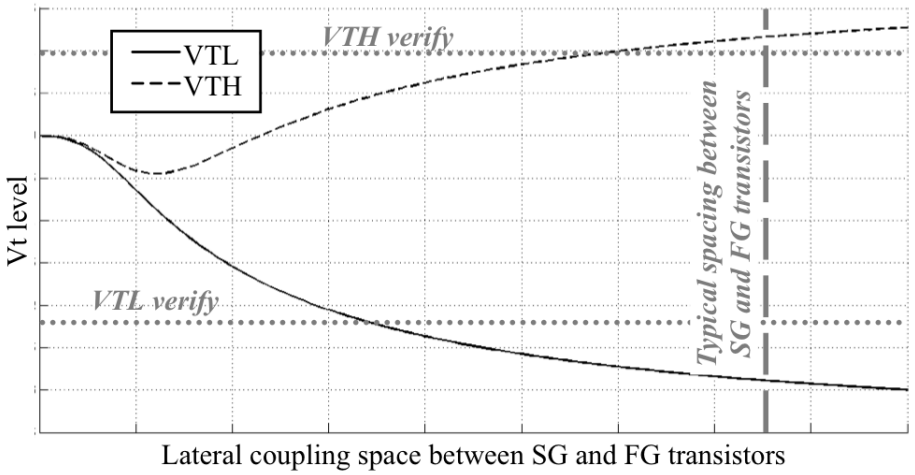


FIGURE 2.15 LATERAL COUPLING ON A ONE CORE-CELL STRING CASE STUDY

As shown in Figure 2.15, the typical spacing between *FG*-transistor and *SG*-transistors ensure Vt levels higher than the limit (*VTH verify* and *VTL verify*). In addition, data reported in Figure 2.15 demonstrate that spacing between FG-transistor and SG-transistors can be reduced, allowing to decrease the silicon area of the NAND-Flash array, while keeping good Vt levels.

We have also used the proposed model to characterize the pulse programming approach. The pulse programming methodology consists in applying a sequence of incremental step pulses (*Vstep*) starting from a low (*Vlow*) to a high (*Vhigh*) programming voltage. This programming method allows reducing and controlling the stress of the silicon oxide, *i.e.* the *Eox* applied to inject and remove charges into the floating gate. Consequently, this programming method increases the reliability of the NAND-Flash.

For a better understanding of the pulse programming approach, Figure 2.16.a presents the Vt level reached after one-pulse and multiple-pulse programming phases. These electrical simulations correspond to a write operation on an erased *FG*-transistor. In Figure 2.16.a, we observe that *VTH verify* level is reached after one programming pulse using the highest programming voltage. We also observe that the stress of the oxide is important at the beginning of the pulse and the maximum *Eox* is about 1.47×10^9 eV/m. Electrical simulations shown in Figure 2.16.b illustrate the benefit of the pulse programming approach. It can be observed that the *VTH verify* level is reached after nine programming pulses (from *Vlow* to *Vhigh*). Since first programming pulses use a lower programming voltage compared to simulations presented in Figure 2.16.a, the *Eox* (*i.e.* the stress of the oxide) is lower. A maximum of 1.23×10^9 eV/m is measured.

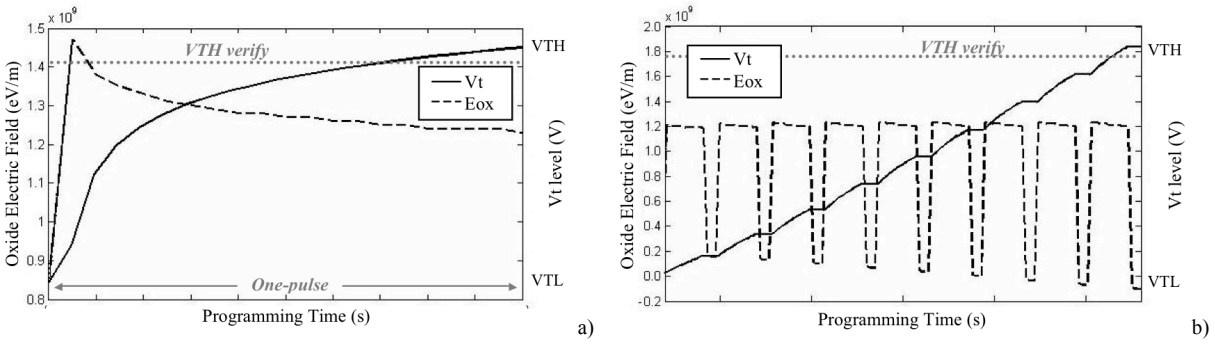


FIGURE 2.16 VT LEVEL ACHIEVED AFTER A) A ONE PULSE AND B) A MULTIPLE PULSE WRITE OPERATION CASE STUDY

Based on these results, the proposed Spice model was used to characterize the pulse programming methodology. A total of 352k simulations have been performed. Each simulation corresponds to a

combination of *Vlow*, *Vhigh* and *Vstep*. Data are reported in Figure 2.17 for a maximum of nine programming pulses.

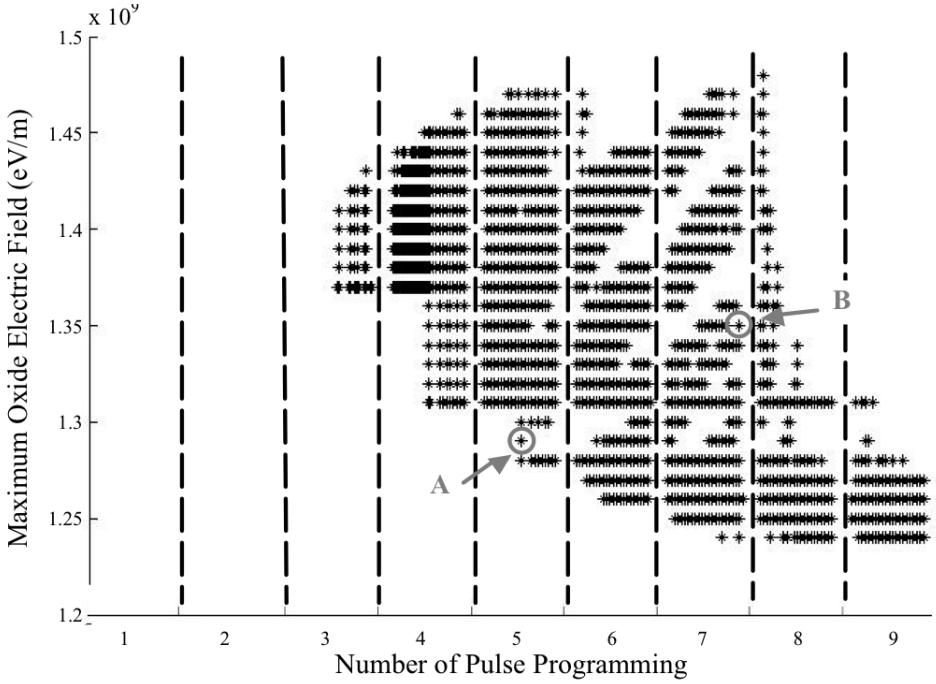


FIGURE 2.17 CHARACTERIZATION OF THE PULSE PROGRAMMING METHOD

Point *A* in Figure 2.17 refers to a combination of *Vlow*, *Vhigh* and *Vstep* allowing to reach *VTH verify* with five programming pulses and a maximum *Eox* of about 1.29×10^9 eV/m. In addition, since point *A* is in the middle of the fifth pulse, it means that the *VTH verify* level has been reached in the middle of this programming pulse and, consequently, five programming pulses are sufficient to guaranty a good write operation. Point *B* refers to a combination of *Vlow*, *Vhigh* and *Vstep* allowing to reach *VTH verify* at the seventh programming pulse with a maximum *Eox* of about 1.35×10^9 eV/m. This time, *VTH verify* level has been reached at the end of this programming pulse. An additional programming pulse is necessary to guaranty *VTH verify* level considering the gap between the model and actual device.

The main conclusion from these simulations is that the increase of the number of programming pulses decreases the *Eox*. Consequently, using the proposed model, we are able to determine the values of *Vlow*, *Vhigh* and *Vstep* such that the lowest silicon oxide stress is obtained for a desired number of programming pulses.

For more details, I have attached in the fourth part of this report one of the main journal paper I produced in this field (reference [RE12]).

4.2.2 TAS-MRAM Testing

Magnetic Random Access Memory (*MRAM*) is an emerging technology with the potential to become the universal on-chip memory. *MRAMs* have high data processing speed, low power consumption and high integration density compared with Flash memories. In addition to non-volatility, these memories, when compared with *SRAMs*, have fair processing speed and reasonable power consumption. Additionally, *MRAMs* are CMOS process fabrication compatible.

In this sub-section, I develop the main contributions carried out on *TAS-MRAM* testing. This work is related to the PhD thesis of Joao Azevedo I supervised and done in collaboration with CROCUS Technology. I first start by providing fundamentals and background on *MRAM* technologies. Then, I present the architecture developed for defect analysis and some important results in terms of fault modeling and test algorithm.

MRAM Technologies

MRAMs are Spintronic devices that store data in Magnetic Tunnel Junctions (*MTJs*). A basic *MTJ* device is usually composed of two ferromagnetic (*FM*) layers separated by an insulating layer, as shown in Figure 2.18. One of the *FM* layers is pinned and acts as a reference layer. The other one is free and can be switched between, at least, two stable states. These states are parallel or anti-parallel with respect to the reference layer. When it is in the parallel state, the *MTJ* offers the minimum resistance (*Rmin*) while the maximum resistance (*Rmax*) is obtained when anti-parallel. The difference between *Rmin* and *Rmax* quantified by the Tunnel Magneto Resistance (*TMR*), is high enough to be sensed during the read operation.

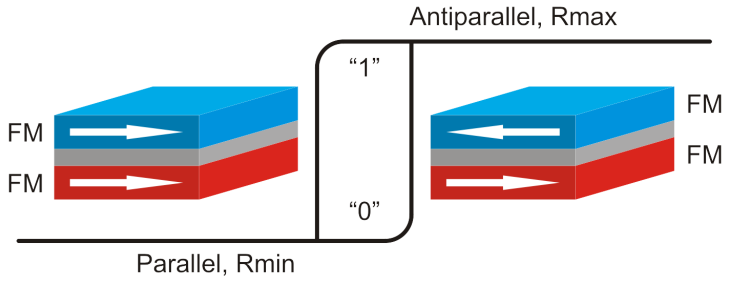


FIGURE 2.18 MTJ IN PARALLEL AND ANTIPARALLEL STATES

Read operation consists in determining the *MTJ's* magnetization state and can be performed by voltage or current sensing across the *MTJ* stack. A CMOS sense amplifier can be used to obtain the stored bit information.

Write operation can be performed using magnetic fields or spin-polarized current and depends on MRAM technologies:

- Field Induced Magnetic Switching (*FIMS*) *MRAMs*. In this approach, two perpendicular magnetic fields are applied simultaneously. Main drawbacks are related to calibration of the field and the thermal activation of half-selected *MTJs*, which increases addressing errors.
- Toggle *MRAMs* was proposed to overcome the selectivity issue of *FIMS* technology. Synthetic layers replaced FM layers and two perpendicular current lines generating magnetic fields are oriented at 45° from the two magnetization stable states.
- Thermally Assisted Switching (*TAS*) *MRAMs* is an alternative switching method for *MRAMs*. The *MTJ* is modified by inserting an anti-ferromagnetic layer (*AFM*) that pins the storage layer while below its blocking temperature (*BT*). *BT* is the threshold temperature above which it is possible to change the magnetization state of the free layer. When *MTJ's* temperature rises above *BT*, the storage layer is freed and can be reversed under the

application of a small magnetic field provided by a single field-line. The magnetic field is maintained beyond the heating voltage pulse to ensure the correct pinning of the storage layer.

- Current Induced Magnetic Switching (*CIMS*) *MRAMs* is the most recent *MRAM* technology. The writing is accomplished by injecting a spin-polarized high current density through *MTJ* without the assistance of any external magnetic field. This approach relies on Spin Transfer Torque (*STT*) effect. *STT* phenomenon is the exchange of spin angular momentum between an incoming spin-polarized current and the local magnetization. This effect applied to *MRAMs* could restore the scalability beyond several Gbit/chip making such a technology the most promising for non-volatile mass data storage.

TAS-MRAM Architecture

The *TAS-MRAM* architecture developed is shown in Figure 2.19. It takes into account the actual organization of the targeted *TAS-MRAM* technology, *i.e.* page organization, column and row decoders, field-line driver and read/write driver. In order to perform electrical simulation of any read/write sequences, the proposed architecture embeds the *TAS-MTJ* model developed by Spintec. This model is based on the physical equations of the *MTJ* and is calibrated with respect to the targeted technology. Moreover, this model is compiled in C language and is compatible with the Spectre simulator of the standard Cadence design suite.

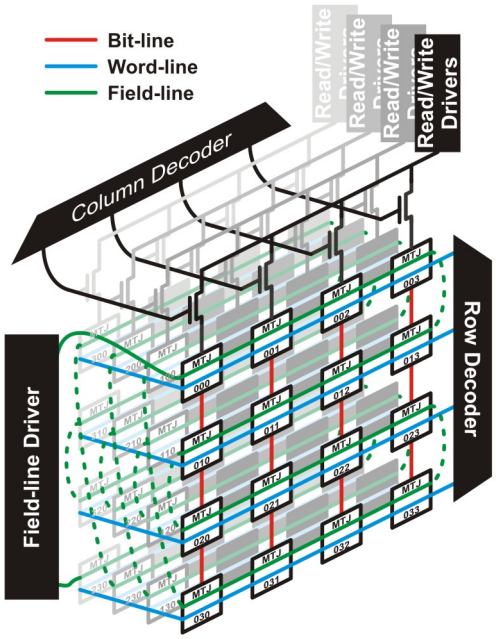


FIGURE 2.19 TAS-MRAM ARCHITECTURE

This architecture has been used to simulate fault-free read/write operations. Table 2.5 summarizes simulated fault-free characteristics of $MTJ_{1,1,1}$ of the *TAS-MRAM* architecture shown in Figure 19. The first column gives the four possible operations r0, r1, w0 and w1. The next five columns provide all the *MTJ's* parameters:

- V – Voltage level at the *MTJ* interface.
- I – Current passing through the *MTJ* during read or write operations.
- R – Resistance of the *MTJ*.
- T – Temperature of the *MTJ* during operations.

- M – Magnetization state that is related to the angle between the two ferromagnetic layers. The parallel magnetization state is represented ideally by "1 ==> logic 0" and the anti-parallel magnetization state by "-1 ==> logic 1". The magnetization state is correlated to the resistivity of the *MTJ*.

Finally, the last column gives the sensing voltage (S) during read operation only. The two resistive states of the MTJ are 1.48kΩ for *Rmin* and 2.80kΩ for *Rmax* during read operation. In normal operation the sensing voltage (S) is around 165mV for *Rmin* and 254mV for *Rmax*. During write operations, the current that passes through the MTJ is high enough to heat its temperature above the blocking temperature, *i.e.* 193°C for W0 and 193/183°C for W1.

TABLE 2.5 $MTJ_{1,1,1}$ CHARACTERISTICS UNDER READ/WRITE OPERATIONS

Operation	$MTJ_{1,1,1}$ parameters					S (mV)
	V (mV)	I (uA)	R (kΩ)	T (°C)	M	
R0	111.49	74.89	1.48	31.16	1	165.67
R1	202.35	72.11	2.80	34.26	-1	254.49
W0	745.32	606.59	-	193.18	1	n.a.
W1	745.32 863.09	606.59 542.63	- -	193.18 183.75	-1	n.a.

TAS-MRAM Testing

To illustrate the usage of the proposed *TAS-MRAM* architecture, I develop in the following the analysis we performed on resistive-bridge defects. The location of injected defects takes into account adjacent lines of the same metal layer or between metal layers of the layout (see Figure 2.20). Defects are classified into two groups: i) Defects related to traditional CMOS fabrication process (*Df1* to *Df4*) and ii) defect related to *MTJ* fabrication process (*Df5*).

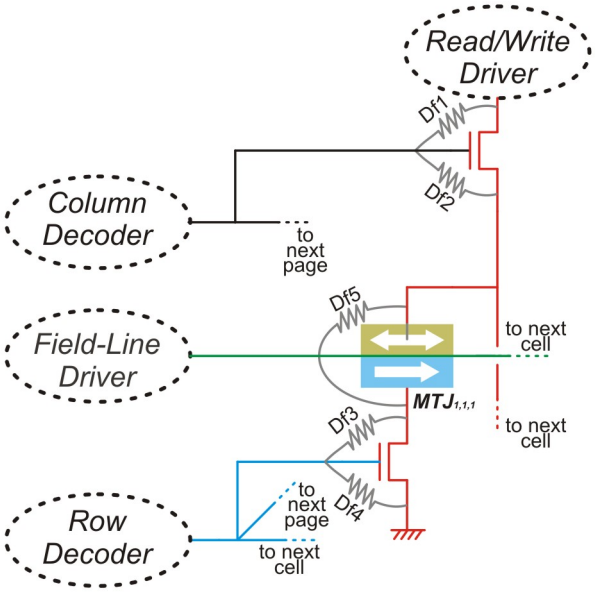


FIGURE 2.20 RESISTIVE-BRIDGE DEFECT INJECTION WITH RESPECT TO $MTJ_{1,1,1}$

Each defect was injected and a set of electrical simulation was performed with different Read/Write sequences and defect sizes. As case study, Figure 2.21 plots the sensing voltage (*S*) when *Df5* is injected for r1 and r0 operations, respectively. Note that the dashed area represents the minimum value of *S* (*Min S*) for a proper r1 operation and the maximum value of *S* (*Max S*) for r0. We have determined the read voltage threshold in a way to guarantee both logic '0' and logic '1' during read operations. Based on r0 and r1 simulations performed on all *MTJs* of the *TAS-MRAM* architecture presented in Figure 2.19, *Min S* and *Max S* values are:

- *Min S* for a r1 = 230mV represents the upper bound of the dashed area.
- *Max S* for a r0 = 187mV represents the lower bound of the dashed area.

If the *S* value is in between the dashed area, the output logic data from the sense amplifier is not reliable.

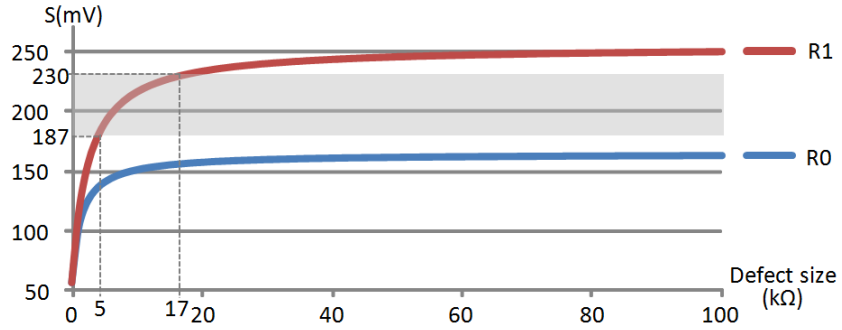


FIGURE 2.21 R0 AND R1 OPERATIONS PERFORMED ON $MTJ_{1,1,1}$ UNDER DF5

As shown in Figure 2.21, *Df5* does not affect r0 operations as the sensing voltage is always under the dashed area. The r1 operations are not reliable for 5kΩ < *Df5* < 17kΩ as the sensing voltage is in between the required levels. When *Df5* lies below 5kΩ, the sense amplifier always return logic '0' even if the *MTJ* contains logic '1'. In this case, the current passing through the defect reduces the sensing voltage and makes r1 operations to be faulty.

A full defect injection campaign was performed for resistive, bridging and capacitive defects. The proposed architecture was used to deeply analyze the observed faulty behaviors and to provide the resulting fault modeling. Defects considered are modeled by single-cell and double-cell faults. The Figure 2.22 gives the resulting single-cell *TAS-MRAM* fault modeling for resistive-bridge defect injection with respect to defect size.

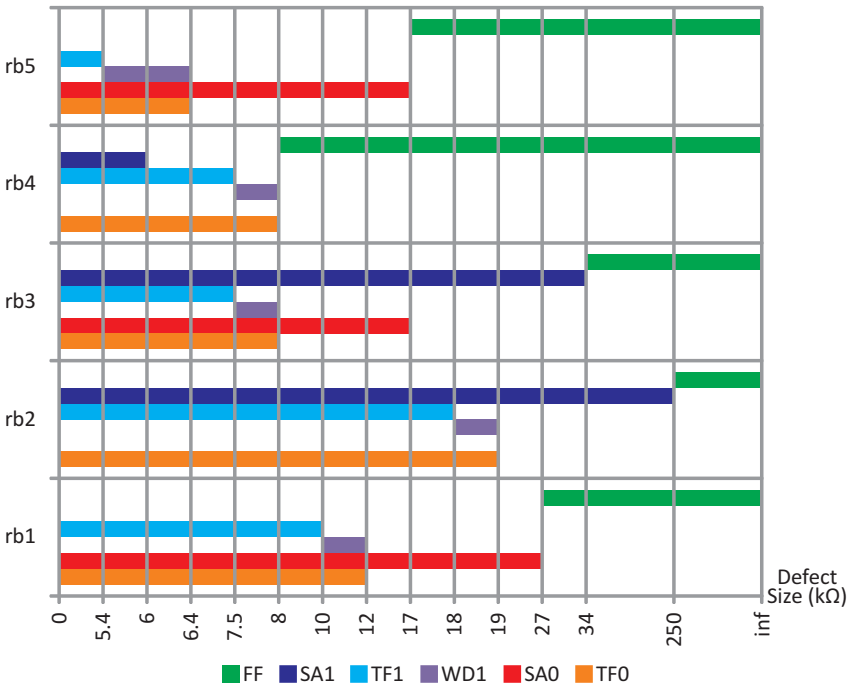


FIGURE 2.22 SINGLE-CELL TAS-MRAM FAULT MODELING WITH RESPECT TO RESISTIVE-BRIDGE DEFECT SIZE

Based on these results, another important contribution of this work is the development of a 14 N March test algorithm that target all faults related to defects.

$$\Updownarrow(w0);\Uparrow(r0,w1);\Uparrow(w1,r1,w0,r0,w1);\Uparrow(w0,r0);\Uparrow(w1,r1);\Downarrow(r1,w1)$$

For more details, I have attached in the fourth part of this report the main journal paper I produced in this field (reference [RE24]).

5 FAULT TOLERANCE

Digital systems have transitioned from specialized applications to ubiquitous mass products. Today, a consumer mobile device may contain a processor with higher computing power than a super computer in the early 1990s. This revolution has been conducted by the evolution of CMOS technology, which allows the production of smaller and cheaper Integrated Circuits (*IC*) with higher performance and lower power consumption. While supporting the need for competitive mass products, this evolution also influences the reliability of digital systems. Increasing occurrence rate of faults and errors during manufacturing processes and circuit lifetime makes robustness one of the upcoming key requirements in many application areas, including safety critical applications and mass products.

In this sub-section, I develop the main contributions carried out on fault tolerance. These works are related to PhD thesis of Julien Vial and Duc Anh Tran. I first start by presenting the main fault tolerant architectures. Then, I present the first contribution related to the *TMR* (Triple Modular Redundancy) architecture, especially its usage for *SoC* yield improvement. Then, I introduce the hybrid fault tolerant architecture we developed for transient and permanent fault detection and correction.

Problem Formulation

To increase the yield for future VLSI systems, fault tolerant architectures have been proposed as a potential solution. Fault tolerant architectures are commonly used to tolerate on-line faults, *i.e.* faults that appear during the normal functioning of the system irrespective of their transient or permanent nature. In the near future, fault tolerant architectures could also be used to tolerate permanent defects due to an imperfect manufacturing process.

Fault tolerant architectures use redundancies. Redundancy is the property of having more resources than needed to perform a given function, which are therefore used to tolerate defects. Fault tolerance architectures are generally classified depending on the type of redundant resources. Basically four types of redundancy are considered:

- Hardware redundancy: It consists in modifying the design by adding additional hardware. For example, instead of having a single processor, three processors are embedded to perform the same operation. The failure of one processor is tolerated thanks to a voter that chooses the majority outputs. This is the basic principle of a *TMR* architecture.
- Software redundancy: The error detection and recovery are based on replicating application processes on a single or multiple computers.
- Information redundancy: Additional data are used to tolerate faults. For example, the use of error-correcting codes requires extra bits that need to be added to the original data bits. Depending on the dimension of extra data and the used code, an error can be either detected or corrected. This kind of redundancy is particularly used in signal transmission technologies. Nevertheless, the use of error-correcting codes in logic cores has non-negligible impact on the design and requires a high area overhead.
- Temporal redundancy: It consists in forcing the system (or a sub-system) to repeat a given operation and then compare the results with those of the previous operation. Such a redundancy is able to tolerate transient or intermittent errors but not permanent errors.

In this field, our contributions are:

- A full analysis of the *TMR* architecture to tolerate permanent faults
- The proposition of a new fault tolerant architecture targeting transient and permanent faults detection and correction.

TMR for Yield Improvement

In this work, we considered hardware redundancy for achieving yield ramp-up benefits. As a case study, we considered the well-known *TMR* fault tolerant architecture in order to tolerate manufacturing defects while increasing the yield (see Figure 2.23).

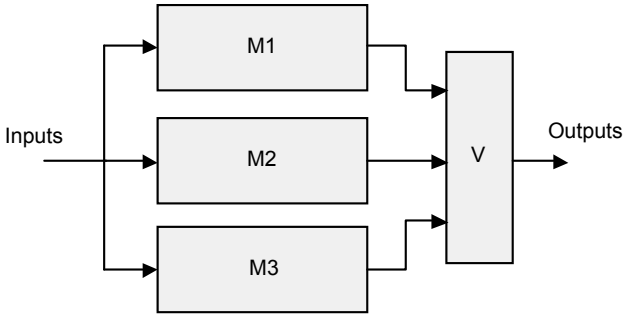


FIGURE 2.23 TMR PRINCIPLE

We have first determined the set of conditions to be satisfied in order to successfully resort to *TMR* to ramp-up the yield. We have taken into account a *SoC* case study made with logic cores and memory cores. After computing the yield using the *Poisson* distribution, implementing *TMR* architectures for logic cores can improve the overall *SoC* yield if the two following conditions are satisfied:

$$Y_{SoC} \leq 1/A_O$$

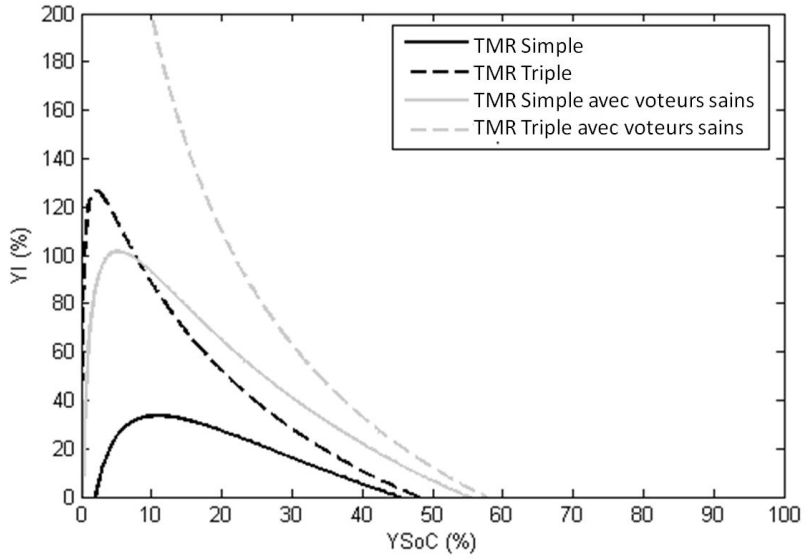
$$Y_{SoCTMR} = e^{(A_O - M)\ln Y_{SoC}} \times \left(1 - 3(1-M)\ln Y_{SoC} + \sum_{i=2}^{\infty} R^{C_i^2} \times \frac{\left[-3(1-M)\ln Y_{SoC}\right]^i}{i!}\right) \times Y_M$$

where:

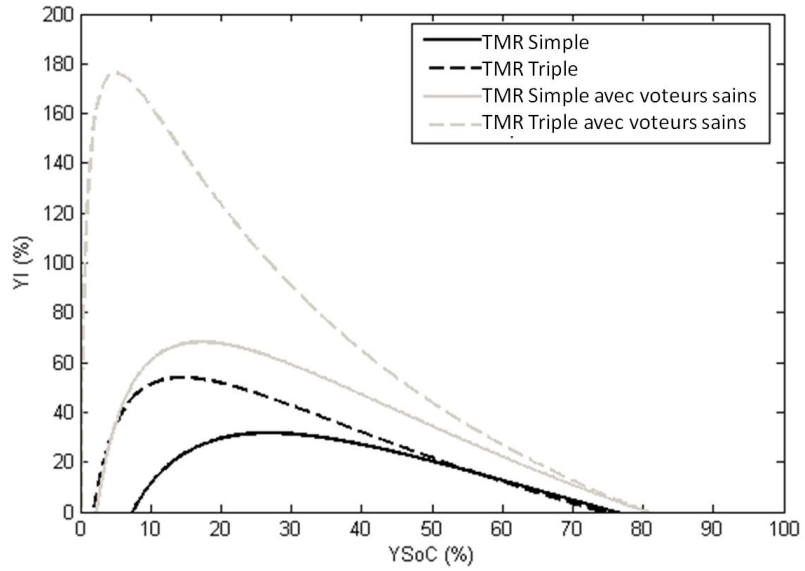
A_0 is the area overhead of the *TMR* architecture.
M is the memory occupancy ratio in the *SoC*.
Y_{SoC} is the overall *SoC* yield.
R being the probability that two defects are tolerated.
Y_M is the yield of memory cores in the *SoC*.

The first condition is related to the area overhead needed to implement *TMR* architectures for logic cores. The second one is related to A_O, M and R. A_O and M are easily computed but R requires determining the percentage of tolerated couple of defect. In fact, the problem is how can we determine the percentage of tolerated couple of defects for a given *TMR* architecture of logic cores. To evaluate the percentage of tolerated couple of defect we generated test patterns able to detect all testable fault pairs. The remaining fault pairs are untestable.

To illustrate and prove the interest of using *TMR* architectures, let us considered, as case study, two benchmark circuits (c5315 with M = 70% and b05 with M = 90%) as the logic cores in a *SoC*. We have computed the yield improvement (Y_I) reachable if a fault-tolerant *SoC* (using *TMR* for logic cores) is manufactured instead of a classical *SoC* (only memory cores are fault-tolerant). The graphs in Figures 2.24.a and 2.24.b show the yield improvement for the two *SoC* examples. In each graph, two *TMR* implementations are considered; *Basic TMR* where only one voter is used and *Triple TMR* where three voters are embedded.



a)



b)

FIGURE 2.24 YIELD IMPROVEMENT FOR A) C5315 WITH M = 70% AND B) B05 WITH M = 90%

For example, let us consider the b05 benchmark circuit used as unique logic core. From Figure 2.24, if the initial yield Y_{SoC} = 30%, the yield improvement (Y_I) is about 31.28% for a Basic *TMR* implementation (59.17% when voters are fault-free) and about 42.69% for a Triple *TMR* implementation (90.49% when voters are fault-free). These results clearly show the interest of using *TMR* architectures for *SoC* yield improvement.

Hybrid Fault Tolerant Architecture

The proposed hybrid fault tolerant architecture uses three types of redundancy: information redundancy for error detection, temporal redundancy for transient error tolerance and hardware redundancy for permanent error correction. Figure 2.25 shows the structural overview of the hybrid fault-tolerant architecture. The architecture employs three copies of combinational logic module (*CL1*, *CL2* and *CL3*). Input demultiplexer (*Demux*) and output multiplexer (*Mux*) are used to select two running *CLs* and to put the third *CL* on standby mode during normal operations. The hybrid fault-tolerant is driven by a control logic module, which controls different configurations of the architecture, *i.e.* decides which two *CLs* are running in parallel.

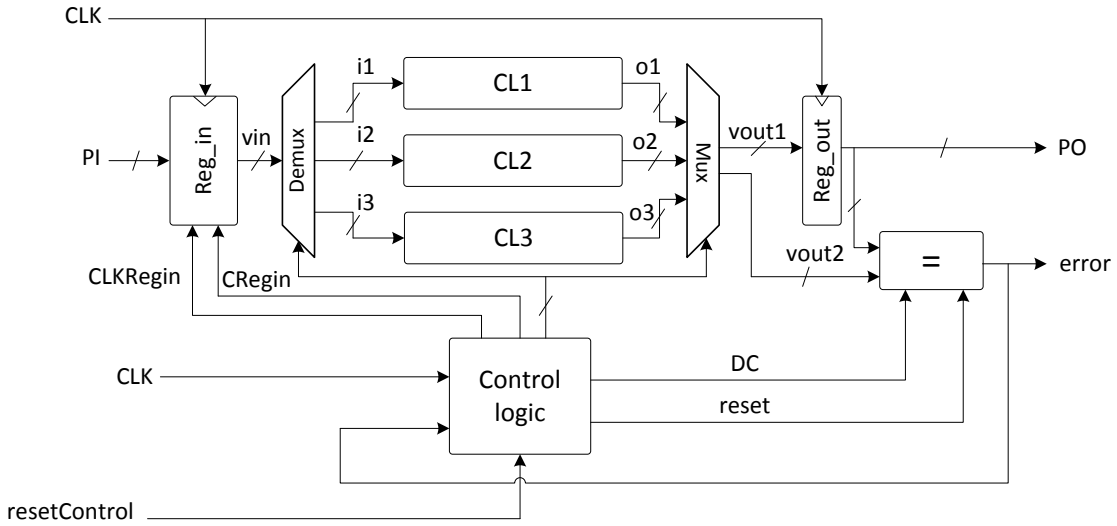


FIGURE 2.25 THE HYBRID FAULT-TOLERANT ARCHITECTURE

Error detection is done by comparing outputs of the two running *CLs* with the help of a pseudo-dynamic comparator in order to improve transient error detection. Figure 2.26 shows the complete architecture of the proposed pseudo-dynamic comparator. Similarly to a traditional static comparator, the pseudo-dynamic comparator is composed of two stages: comparison and accumulation. The comparison stage consists of static 2-input XOR gates while the accumulation stage is modified from the one of the static comparator. Static OR gates, in the first layer of the static OR-tree, are replaced by *DOR* (Dynamic OR) gates. The rest of the static OR-tree is left intact. Compared to the static comparator, the pseudo dynamic comparator has two more inputs, which control *reset* and *DC* inputs of the *DOR* gates.

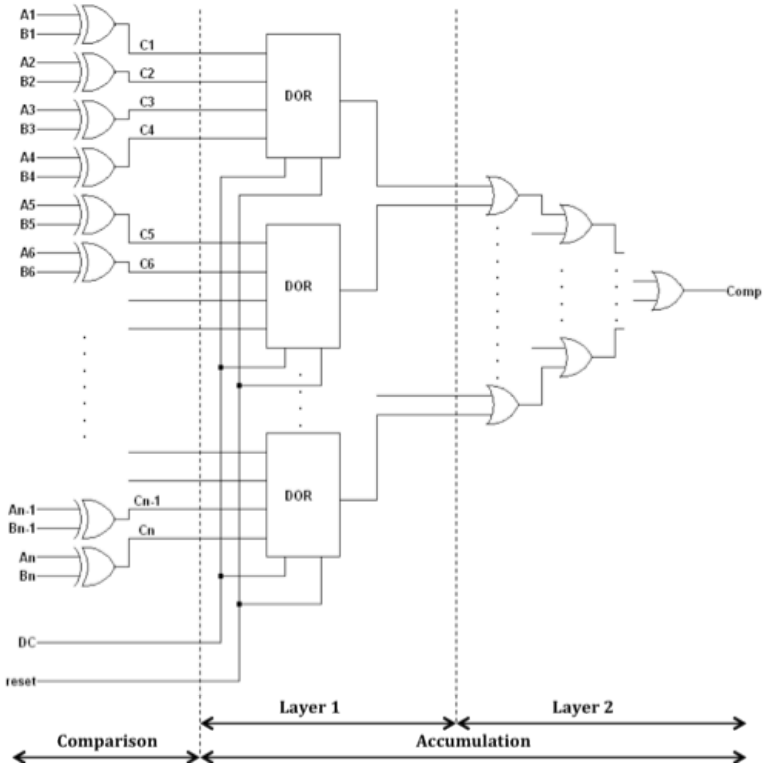


FIGURE 2.26 PSEUDO DYNAMIC COMPARATOR ARCHITECTURE.

To highlight the functioning of the proposed approach, Figure 2.27 shows a simulation in presence of a transient fault emulated as a glitch injected to fault signal at the beginning of the 10th period (from t = 90ns to t = 100ns). Consequently, the captured value in the output register and one of the running CLs' outputs are different at the beginning of the 10th period. Besides, in this simulation, primary input vector *PI* is kept unchanged during two *CLK* periods of error detection and correction. In Figure 2.27, we can observe that error signal turns to logic '1' signaling that the comparator has different values during the comparison window. During the same period between t = 90ns and t = 100ns, *CL1* is put in stand-by (stable logic 00000000 at *i1*) while *CL3* is turn on (*i3* receives captured primary input). The re-configuration successfully finishes before the beginning of new *CLK* period. At next *CLK* positive edge (t = 100ns), the previous value of primary input (33EC884A) is applied to *CL2* and *CL3*. This shows that the input register and the control logic module have correctly triggered a re-computation. The re-computation finishes before next *CLK* edge at t = 110ns. As *vout2* and *PO* are identical, error returns to logic '0' signaling that the captured output is correct. The transient error is tolerated by the architecture with two additional *CLK* periods.

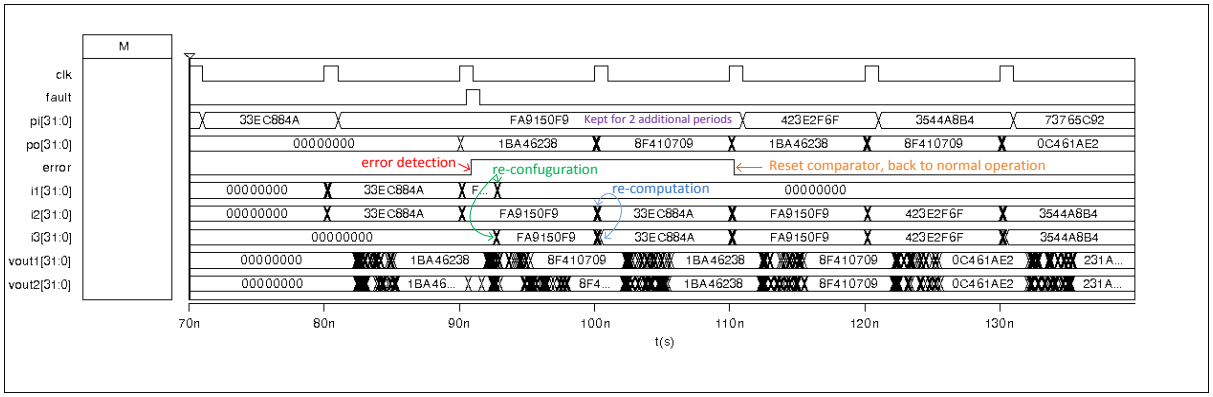


FIGURE 2.27 PSEUDO DYNAMIC COMPARATOR ARCHITECTURE.

Comparisons with *TMR* architectures using ISCAS'85 and ITC'99 benchmark circuits have been also made. Results show that the proposed hydride architecture reduces power consumption by about 33% while keeping area overhead as low as 3%-6%.

For more details, I have attached in the fourth part of this report one of the main journal paper I produced in this field (reference [RE14]).

6 CONTRIBUTION SUMMARY AND PERSPECTIVES

To summarize the different contributions I did in the field of test and reliability of SoC let us consider a basic SoC example made of logic IPs (microprocessor and logic cores) and memory IPs (volatile and non-volatile memory cores).

Concerning logic IP test I contributed to the definition of high effective test sequences able to test different fault models and also to the development of a hardware test pattern generator able to produce such effective test sequence in a BIST environment. I also worked in the field of low power testing, especially for the test per scan environment where main contributions were related to the reduction of the peak power during the test cycle by using scan-chain reordering and specific X-filling approaches.

My main research activities were devoted to the memory testing part where I addressed three memory technologies. For the SRAM, I fully analyses the different elements that constitute the memory architecture, *i.e.* core-cells and I/O circuitry. Main results are a full methodology to analyze the impact of actual defects and to propose dedicated test algorithms. Diagnosis approaches where also developed to target specific memory elements. Flash memory testing where also addressed. In this field, our main contribution was the development of effective models for different Flash array organization (NOR and NAND array). Proposed models are suitable for the analysis of actual defects that may affect the Flash memory but also to help the design phase by providing suitable information such as technology sizing and characterization of programming methods. Always in the memory test field, more recently I worked with an emerging non-volatile memory technology, the TAS-MRAM technology for which we fully analyze the impact of manufacturing defects and proposed an effective test algorithm.

Reliability field was addressed for logic cores where we have firstly analyzed the interest of the *TMR* architecture for the yield improvement. With this study, we highlight the main conditions suitable for the *TMR* usage for an *SoC*. More recently, we have developed a hybrid fault tolerant architecture that uses information, timing and hardware redundancies. Compare to *TMR*, this new approach is able to detect and correct transient and permanent faults as well.

Based on these different activities some ongoing works and perspectives are exposed in the following sub-sections.

Perspectives on Logic IP Test

Perspectives in this field are mainly related to delay fault testing. We have demonstrated that taking into account physical design issues such as multi-aggressor crosstalk, Power Supply Noise (*PSN*) and Ground Bounce (*GB*) during test pattern generation allow us to provide high quality input test patterns with a maximum delay difference about 80% in comparison with standard path delay ATPG test methods. The developed exhaustive test pattern generation approach, shown in Figure 2.28, is executed in seven stages: (i) circuit netlist creation (ii) selection of critical paths, (iii) placement and routing of circuit netlist, (iv) X-bit pattern generation, (v) identification of multi-aggressors, (vi) X-bit filling by backtrace approach, and (vii) path delay measurement.

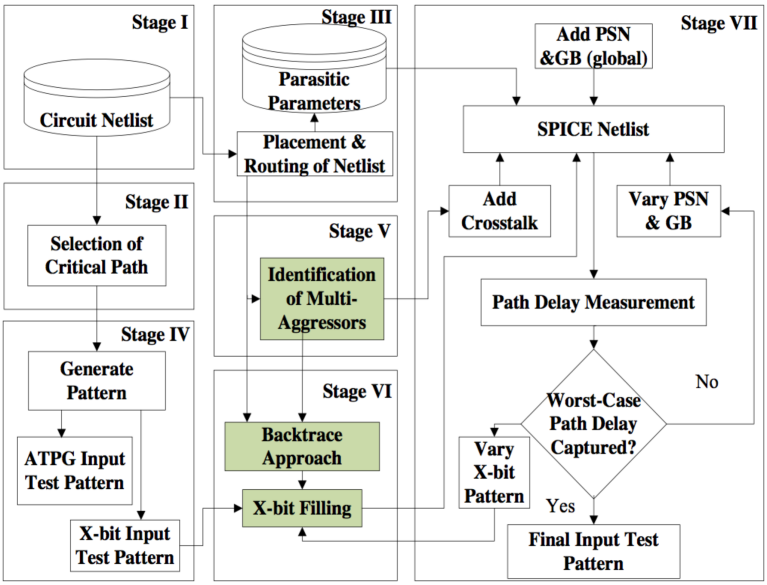


FIGURE 2.28 PHYSICAL DESIGN AWARE PATTERN GENERATION METHOD

We are currently working in this this field with, as main target, the proposition of an ATPG method able to produce high quality input test patterns with a maximum delay difference.

Another perspective on delay fault testing is related to the ongoing study I supervised on at-speed test problematic for test chips. Here, the goal is to develop an innovative at-speed test strategy for test chips used for the development of future nanometer technologies. The proposed strategy should lead to novel test generation and *DfT* techniques able to capture all defects that might be found in prototypes, but through preliminary validation on test chips dedicated to process development. Another important feature of the proposed test strategy will be to ease the identification and location of root causes of failures (process issues identification). Specific logic diagnostic approaches will be developed to this purpose.

Perspectives on Memory Test

In this field perspectives are mainly related to non-volatiles memory technologies. Non-volatile memory market is one of vectors that drive the semiconductor industry. Nomadic devices such as cellular phones, music players, and embedded systems such as micro controllers integrate an important amount of non-volatile memory. Until now, this niche market has been dominated by Flash memories. Unfortunately, Flash memories have a few unpleasant features like slow write memory access, poor endurance and demand for high voltage power supply. New non-volatile memories represent an alternative to Flash memories since they have many advantages: speed, density, non-volatility, low power consumption, scalability and endurance. Table 2.6 gives an overview of the different properties of various memory technologies.

TABLE 2.6 FIGURE OF MERIT OF THE VARIOUS KINDS OF RANDOM ACCESS MEMORIES: DYNAMIC (DRAM), STATIC (SRAM), AND FLASH ARE BASED ON SEMICONDUCTOR WHILE FERROELECTRIC (FERAM), PHASE-CHANGE (PCRAM), MAGNETIC (MRAM), OXIDE RESISTIVE RAM (OXRAM) AND CONDUCTIVE BRIDGING RAM (CBRAM) ARE NEW CONCEPTS

	Memory Technology							
	DRAM	**SRAM**	**FLASH**	**FeRAM**	**PCRAM**	**MRAM**	**OxRAM**	**CBRAM**
Write speed	Moderate	Fast	Slow	Moderate	Moderate	Fast	Fast	Fast
Read speed	Moderate	Fast	Fast	Moderate	Fast	Fast	Fast	Fast
Density	High	Low	High	Medium	High	High	High	High
Endurability	Good	Good	Poor	Poor	Good	Good	Good	Good
Power	High	Low	Low	Low	Low	Low	Low	Low
Refresh	Yes	No	No	No	No	No	No	No
Retention	No	No	Yes	Partially	Yes	Yes	Yes	Yes
Scalability	Bad	Good	Good	Medium	Good	Good	Good	Good
Write/Erase	Charge (Capacitance)	CMOS Logic	Charge (Tunneling)	Ferroelectric	Phase Transition	Magnetization	Resistive Switching	Resistive Switching

Based on this comparative study, *MRAM* and Resistive-*RAM* (*ReRAM: OxRAM* and *CBRAM*) seem to be the most promising next-generation candidates to succeed Flash memories but there are material, production, test and reliability issues associated with these technologies.

Firstly, *MRAMs* will be the main target, especially the new technology development related to the multiple-bit *MRAM*. In that case, the idea is to have not only two resistance levels (*Rmin* and *Rmax*), but multiple resistance levels to store multiple-bits in a single *MTJ*. *STT MRAM* technology is also becoming a mature technology and thus can be investigate for test perspectives.

ReRAM concept is also seen as one of the most promising candidate to replace Flash memories. The basic idea of this technology is that a dielectric, which is normally insulating, can be made to conduct through a filament or conduction path formed after application of a sufficiently high voltage. The conduction path formation can arise from different mechanisms; Thermo-Chemical Mechanism (*TCM*), Electro-Chemical metallization Mechanism (*ECM*) and Valence Change Mechanism (*VCM*). Defect densities, failure mechanisms and fault models of *OxRAMs* and *CBRAMs* are yet to be investigated and are thus part of my future works.

Perspectives on Reliability

In this field, we are implementing the proposed hybrid architecture to the case of pipeline architectures. As first development, we have extended the initial approach to the case of a pipeline structure as shown in Figure 2.29. As initially proposed each *CL* stages in the pipeline are triplicated and pseudo-dynamic comparators are added. The control logic module has been modified in a way to manage both error detection and correction while preserving the normal pipeline functionality.

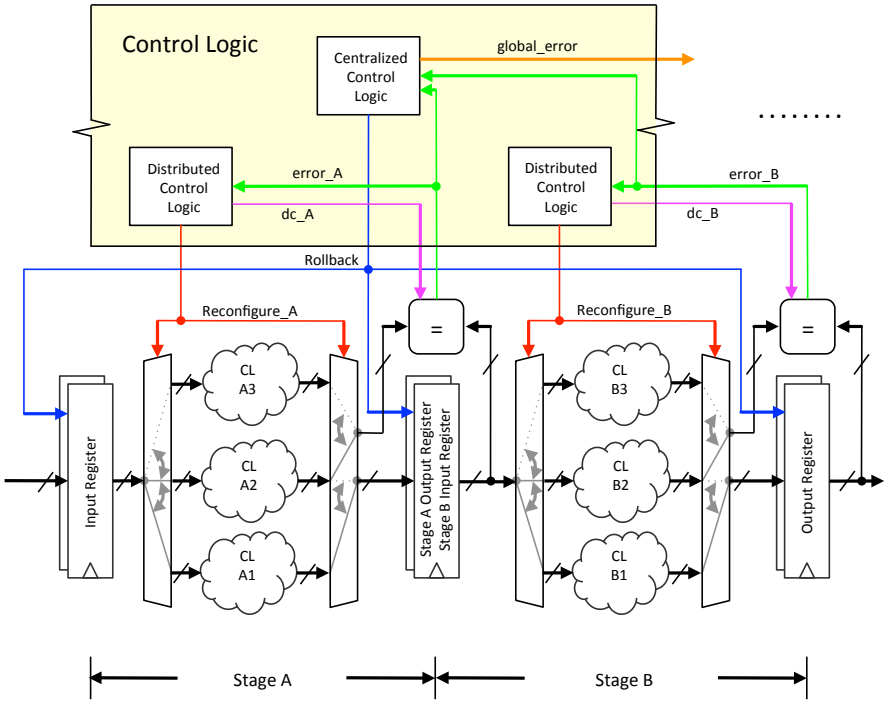


FIGURE 2.29 PIPELINED HYBRID FAULT-TOLERANT ARCHITECTURE

On-going works are related to the implementation of the pipeline hybrid fault tolerant architecture to hardened combinational parts of a *MIPS* microprocessor. Preliminary results are encouraging since our approach is only 5% more costly *w.r.t. TMR* in terms of area while offering a significant reduction in power, which is about 40%.

Perspectives in this field are first related to the evaluation of the fault tolerance capability of the hybrid architecture. Then, the hybrid architecture must be embedded in an *FPGA* to run programs and hardware fault injectors to estimate the effectiveness of the proposed solution.

PARTIE 3 : PRODUCTION SCIENTIFIQUE

Cette partie présente la liste détaillée de mes publications de recherche.

Afin de comprendre l'ordre des auteurs dans la liste suivante, il est important de connaitre la politique de publication de l'équipe. Jusqu'en 2006, nous utilisions l'ordre alphabétique ce qui explique ma position en tant que dernier auteur sur les publications relatives à mes travaux de thèse ainsi que sur celles des premières thèses que j'ai encadrées. Depuis 2007, suite aux recrutements d'Alberto Bosio et Luigi Dilillo dans l'équipe, nous plaçons systématiquement l'encadrant principal en deuxième position après le thésard, et le classement des autres auteurs reste un classement alphabétique. De plus, lors de publications en collaboration avec d'autres équipes de recherche ou industries, nous plaçons majoritairement les membres extérieurs à la fin de la liste des auteurs.

Il est à noter que les références [CO14], [CO17] et [CO54] ont été primés au titre du meilleur article des congrès « IEEE European Test Symposium » en 2004, « IEEE Design and Diagnostics of Electronic Circuits and Systems » en 2005 et « International Conference on Advances in System Testing and Validation Lifecycle » en 2009. L'article référencé [CO25] a reçu la médaille de bronze du congrès « IEEE Conference on Ph.D. Research in Microelectronics and Electronics » en 2006. La référence [O1] est un ouvrage scientifique d'environ 200 pages relatant les activités du groupe dans le cadre du test des mémoires SRAM.

De plus, les 18 publications les plus citées (source « Google Scholar ») sont présentées par thèmes de recherche sur le Tableau 3.1.

TABLEAU 3.1 RÉPARTITION THÉMATIQUE DES 18 RÉFÉRENCES LES PLUS CITÉES

Thèmes de Recherche	**Publications les plus citées**
Test de Pannes Temporelles	[CO3], [RE2], [RE3], [RE4]
Test Faible Consommation	[CO11], [C26]
Test des Mémoires SRAM	[O1], [RE6], [CO8], [CO13], [CO14], [CO15], [CO18], [CO19], [CO20], [CO32]
Tolérance aux Fautes	[CO46]
Diagnostic Logique	[CO37]

1 THESE DE DOCTORAT

[TH1] "Test Intégré des Circuits Digitaux : Analyse et Génération de Séquences Aléatoires Adjacentes"

Soutenance : le 14 Novembre 2001, à l'Université Montpellier II – LIRMM

Jury :

René David, Directeur de Recherche Émérite, INPG Grenoble, Examinateur
Patrick Girard, Chargé de Recherche CNRS, LIRMM, Examinateur
Christian Landrault, Directeur de Recherche CNRS, LIRMM, Président
Michaël Nicolaidis, Directeur de Recherche CNRS, TIMA, Rapporteur
Serge Pravossoudovitch, Professeur, Univ. Montpellier II, Directeur de Thèse
Pascale Thevenod-Fosse, Directeur de Recherche CNRS, LAAS, Rapporteur

Résumé :

Cette thèse s'inscrit dans le cadre du test intégré des circuits digitaux et plus particulièrement dans la problématique nouvelle induite par les rendements de fabrication et les phénomènes particuliers apparaissant dans les technologies submicroniques. En effet, dans ces technologies, l'importance relative de défaillances, non représentées par le modèle classique de collage, peut devenir prépondérante. Ainsi, pour obtenir des séquences de test ayant une couverture de défauts satisfaisante, la prise en compte d'autres modèles de pannes tels que les courts-circuits et les délais devient indispensable. L'utilisation de ces modèles induit des propriétés particulières de détection liées à la structure même des séquences de test. L'étude présentée dans la première partie de ce manuscrit porte précisément sur l'analyse comparative des qualités de détections de divers types de séquences de test. Nous montrons ainsi que les séquences aléatoires adjacentes (séquences dites RSIC pour « Random Single Input Change ») sont particulièrement efficaces lorsque l'on considère, en complément du modèle de collage, les modèles de court-circuit et délai. La deuxième partie de ce manuscrit est quant à elle consacrée à la réalisation matérielle d'un générateur intégré produisant de telles séquences aléatoires adjacentes.

2 OUVRAGES

[O1] ***"Advanced Test Methods for SRAMs: Effective Solutions for Dynamic Fault Detection in Nanoscaled Technologies"***
A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel
Publié par Springer Science, ISBN 978-1-4419-0937-4, 2009

3 CONTRIBUTIONS A OUVRAGE

[OU1] ***"Random Adjacent Sequences: An Efficient Solution for Logic BIST"***
R. David, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
SoC Design Methodology, pp. 413-424
Publié par Kluwer Academic Publishers, ISBN 1-4020-7148-5, 2002.

[OU2] ***"Scan Cell Reordering for Peak Power Reduction during Scan Test Cycles"***
N. Badereddine, P. Girard, S. Pravossoudovitch, A. Virazel, C. Landrault
VLSI-Soc: From Systems to Silicon, pp. 267-281
Publié par Springer Science, ISBN 978-0-387-73661-7, 2007

4 REVUES SCIENTIFIQUES AVEC COMITE DE LECTURE

[RE1] ***"A Scan-BIST Structure to Test Delay Faults in Sequential Circuits"***
P. Girard, C. Landrault, V. Moreda, S. Pravossoudovitch, A. Virazel
Journal of Electronic Testing Theory and Applications, vol 14, No 1/2, pp 95-102
Revue publiée par Kluwer Academic Publishers, ISNN 0923-8174, Avril 1999

[RE2] ***"Delay fault testing: Choosing Between Random SIC and Random MIC Test Sequences"***
A. Virazel, R. David, P. Girard, C. Landrault, S. Pravossoudovitch
Journal of Electronic Testing Theory and Applications, vol 17, No 3/4, pp 233-241
Revue publiée par Kluwer Academic Publishers, ISNN 0923-8174, Juin 2001

[RE3] ***"Hardware Generation of Random Single Input Change Test"***
R. David, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
Journal of Electronic Testing Theory and Applications, vol 18, No 2, pp 145-157
Revue publiée par Kluwer Academic Publishers, ISNN 0923-8174, Avril 2002

[RE4] ***"High Defect Coverage with Low Power Test Sequences in a BIST Environment"***
P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel, H.-J. Wunderlich
IEEE Design & Test of Computers, vol 19, No 5, pp 44-52
Revue publiée par IEEE Computer Society Press, ISSN 0740-7475, Septembre 2002

[RE5] ***"Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test"***
S. Borri, M. Hage-Hassan, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel
Journal of Electronic Testing Theory and Applications, vol 21, No 2, pp 169-179
Revue publiée par Springer Science, ISNN 0923-8174, Avril 2005

[RE6] ***"Efficient March Test Procedure for Dynamic Read Destructive Fault Detection in SRAM Memories"***
L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan
Journal of Electronic Testing Theory and Applications, vol 21, No 5, pp 551-561
Revue publiée par Springer Science, ISNN 0923-8174, Octobre 2005

[RE7] ***"A Gated Clock Scheme for Low Power Testing of Logic Cores"***
Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, A. Virazel
Journal of Electronic Testing Theory and Applications, vol 22, No 1, pp 89-99
Revue publiée par Springer Science, ISNN 0923-8174, Février 2006

[RE8] ***"ADOFs and Resistive-ADOFs in SRAM Address Decoders: Test Conditions and March Solutions"***
L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan
Journal of Electronic Testing Theory and Applications, vol 22, No 3, pp 287-296
Revue publiée par Springer Science, ISNN 0923-8174, June 2006

[RE9] ***"Analysis and Test of Resistive-Open Defects in SRAM Pre-Charge Circuits"***
L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, M. Bastian
Journal of Electronic Testing Theory and Applications, vol 23, No 5, pp 435-444
Revue publiée par Springer Science, ISNN 0923-8174, octobre 2007

[RE10] ***"A Selective Scan Slice Encoding Technique for Test Data Volume and Test Power Reduction"***
N. Badereddine, Z. Wang, P. Girard, K. Chakrabarty, A. Virazel, S. Pravossoudovitch, C. Landrault
Journal of Electronic Testing Theory and Applications, vol 24, No 4, pp 353-364
Revue publiée par Springer Science, ISNN 0923-8174, aout 2008

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L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan

Journal of Integrated Circuits and Systems, vol 3, No 1, pp 7-12
Revue publiée par SBC, ISNN 1807-1953, mars 2008

[RE12] ***"A SPICE-Like 2T-FLOTOX Core-Cell Model for Defect Injection and Faulty Behavior Prediction in eFlash"***
O. Ginez, J.-M. Daga, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
Journal of Electronic Testing Theory and Applications, vol 25, No 2-3, pp 127-144
Revue publiée par Springer Science, ISNN 0923-8174, juin 2009

[RE13] ***"Analysis of Resistive-Open Defects in SRAM Sense Amplifiers"***
A. Ney, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel, M. Bastian
IEEE Transactions on VLSI Systems, vol. 17, No 10, pp 1556-1158
Revue publiée par IEEE, ISSN 1063-8210, octobre 2009

[RE14] "***Is TMR Suitable for Yield Improvement?"***
J. Vial, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
IET Computers and Digital Techniques, vol. 3, No 6, pp 581-592
Revue publiée par IET, ISSN 1751-8601, novembre 2009

[RE15] ***"A Comprehensive Framework for Logic Diagnosis of Arbitrary Defects"***
A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel
IEEE Transactions on Computers, vol. 59, No 3, pp 289-300
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[RE16] ***"A Comprehensive Analysis of Transition Fault Coverage and Test Power Dissipation for LOS and LOC Schemes"***
F. Wu, L. Dilillo, A. bosio, P. Girard, S. Pravossoudovitch, A. Virazel, M. Tehranipoor, X. Wen, N. Ahmed
Journal of Low Power Electronics, vol. 6, No 2, pp 359-374
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[RE17] ***"SoC yield Improvement - Using TMR Architectures for Manufacturing Defect Tolerance in Logic Cores"***
J. Vial, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch
International Journal on Advances in Systems and Measurements, vol. 3, No 1&2, pp. 1-10
Revue publiée par IARIA, ISSN 1942-261x, 2010

[RE18] ***"Analysis and Fault Modeling of Actual Resistive Defects in ATMELtm eFlash Memories"***
P.-D. Mauroux, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, B. Godard, G. Festes, L. Vachez
Journal of Electronic Testing Theory and Applications, vol 28, No 2, pp 215-228
Revue publiée par Springer Science, ISNN 0923-8174, avril 2012

[RE19] ***"Impact of Resistive-Bridging Defects in SRAM at Different Technology Nodes"***
R. A. Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, N. Badereddine
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[RE20] ***"Uncorrelated Power Supply Noise and Ground Bounce Consideration for Test Pattern Generation"***
A. Todri, A. Bosio, L. Dilillo, P. Girard, A. Virazel
IEEE Transactions on VLSI Systems, DOI 10.1109/TVLSI.2012.2197427
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[RE21] ***"A Study of Tapered 3-D TSVs for Power and Thermal Integrity"***
A. Todri, S. Kundu, P. Girard, A. Bosio, L. Dilillo, A. Virazel
IEEE Transactions on VLSI Systems, vol. 21, No 2, pp 306-319
Revue publiée par IEEE, ISSN 1063-8210, février 2013

[RE22] ***"Testing a Commercial MRAM under Neutron and Alpha Radiation in Dynamic Mode"***
G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, A. Todri, A. Virazel, S. Mcclure, A. Touboul, F. Wrobel, F Saigne
IEEE Transaction on Nuclear Science, vol. 99, pp 1-6
Revue publiée par IEEE, ISSN 0018-9499, février 2013

[RE23] ***"Globally Constrained Locally Optimized 3D Power Delivery Networks"***
A. Todri, S. Kundu, P. Girard, A. Bosio, L. Dilillo, A. Virazel,
IEEE Transaction on Very Large Scale Integration Systems,
Digital Object Identifier 10.1109/TVLSI.2013.2283800, octobre 2013

[RE24] ***"A Complete Resistive-Open Defect Analysis for Thermally Assisted Switching MRAMs"***
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri, J.Alvarez-Herault et K. McKay,
IEEE Transaction on Very Large scale Integration Systems,
Digital Object Identifier 10.1109/TVLSI.2013.2294080, 2014

[RE25] ***"Evaluating a Radiation Monitor for Mixed-Field Environments based on SRAM Technology"***
G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Todri, A. Virazel, J. Mekki, M. Brugger, F. Wrobel, F. Saigné
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[RE26] ***"A New Hybrid Fault-Tolerant Architecture for Digital CMOS Circuits and Systems"***
D. A. Tran, A. Virazel A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, H.-J. Wunderlich
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G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, A. Todri, A. Virazel, J. Mekki, M. Brugger, F. Wrobel, F. Saigné
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[RE28] ***"Multiple Cell Upset Classification in Commercial SRAMs"***
G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Todri, A. Virazel, H. Puchner, C. Frost, F. Wrobel and F.Saigné
in press, IEEE Transaction on Nuclear Science, 2014

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[CO1] ***"A new Scan-BIST structures to test delay faults in sequential circuits"***
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[CO2] ***"A BIST structure to test delay faults in a Scan environment"***
P. Girard, C. Landrault, V. Moreda, S. Pravossoudovitch, A. Virazel
ATS'1998 : Asian Test Symposium, Singapore, 25-27 novembre 1998
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[CO3] ***"Delay fault testing: Choosing Between Random SIC and Random MIC Test Sequences"***
A. Virazel, R. David, P. Girard, C. Landrault, S. Pravossoudovitch
ETW'2000: European Test Workshop, Cascais, Portugal, 23- 26 mai 2000
Actes publiés par IEEE Computer Society Press, ISBN 0-7695-0701-8, pp 9-14

[CO4] ***"Comparison between Random and Pseudo-Random Generation for BIST of Delay, Stuck-at and Bridging Faults"***
P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel

IOLTW'2000: Int. On-Line Testing Workshop, Palma de Mallorque, Espagne, 3-5 juillet 2000
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ETW'2001: European Test Workshop, Stockholm, Suéde, 29 mai – 1ier juin 2001,
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[CO6] ***"RSIC Generation: A Solution for Logic BIST"***
R. David, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
VLSI-SOC'2001: 11th IFIP International Conf. on VLSI, Montpellier, France, 3-5 décembre 2001,
Actes publiés par LIRMM, ISBN 2-9517461-0-5, pp 111-117

[CO7] ***"An On-Chip Generator for High Defect Coverage"***
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VTS'2002 : VLSI Test Symposium, Monterey (CA), USA, 26 avril – 2 mai 2002,
Actes publiés par IEEE Computer Society Press, ISBN 0-1093-0167, pp. 145-150

[CO8] ***"Defect-Oriented Dynamic Fault Models for Embedded SRAMs"***
S. Borri, M. Hage Hassan, P. Girard, S. Pravossoudovitch, A. Virazel
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[CO9] ***"Comparison of Open and Resistive-Open Defect Test Conditions in SRAM Address Decoders"***
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[CO10] ***"Design of Routing-Constrained Low Power Scan Chains"***
Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, A. Virazel
DELTA'2004 : Workshop on Electronic Design, Test and Applications, Perth, Australia, 28-30 janvier 2004
Actes publiés par IEEE Computer Society Press, ISBN 0-7695-2081-2, pp 287-292

[CO11] ***"Design of Routing-Constrained Low Power Scan Chains"***
Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, A. Virazel
DATE'2004 : Design Automation and Test in Europe, Paris, France, 16-20 février 2004
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[CO12] ***"March Tests Improvements for Address Decoder Open and Resistive Open Fault Detection"***
L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan
LATW'2004 : Latin American Test Workshop, Cartagena, Colombia, 8-10 mars 2004
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[CO13] ***"March iC-: An Improved Version of March C- for ADOFs Detection"***
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SETS'2006: South European Test Seminar, Neustift, Tyrol, Austria, 27-31 mars 2006

[DR23] ***"Unified Diagnostic Method Focusing Several Fault Models"***
A. Rousset, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel
SETS'2006: South European Test Seminar, Neustift, Tyrol, Austria, 27-31 mars 2006

[DR24] ***"Réduction de la consommation de Puissance de Pic Pendant le Test Série"***
N. Badereddine, P. Girard, S. Pravossoudovitch, A. Virazel, C. Landrault
DOCTISS'06: Journées des Doctorants de l'Ecole Doctorale I2S, Montpellier, France, 13 avril 2006

[DR25] "Technique Structurelle d'Affectation des Bits Non Spécifiés en Vue d'une Réduction de la Puissance de Pic Pendant le Test Série"
N. Badereddine, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel, H.-J. Wunderlich
JNRDM'06: IXI Journées Nationales du Réseau Doctoral de Microélectronique, Renne, France, 10-12 mai 2006

[DR26] ***"Méthode unifiée de diagnostic ciblant l'ensemble des modèles de fautes"***
A. Rousset, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel
JNRDM'06: IXI Journées Nationales du Réseau Doctoral de Microélectronique, Renne, France, 10-12 mai 2006

[DR27] ***"Structural Power-Aware Assignment of Xs for Peak Power Reduction during Scan Testing"***
N. Badereddine, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel, H.-J. Wunderlich
ETS'2006 : European Test Symposium, Southampton, UK, 21-25 mai 2006

[DR28] ***"Failure Mechanisms due to Process Variations in Nanoscale SRAM Core-Cells"***
P. Girard, S. Pravossoudovitch, A. Virazel, M. Bastian
ETS'2006 : European Test Symposium, Southampton, UK, 21-25 mai 2006

[DR29] ***"Unified Diagnostic Method Targeting Several Fault Models"***
A. Rousset, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel
VLSIsoc'06: PhD Forum at IFIP International Conference on Very Large Scale Integration, Nice, France, 16-18 octobre, 2006

[DR30] ***"Diagnostic Multi-Modèles des Circuits Logiques"***
A. Rousset, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel
MAJECSTIC'06: Manifestation des Jeunes Chercheurs STIC, Lorient, France, 22-24 novembre, 2006

[DR31] ***"Test and Testability of Redundant Circuits"***
J. Vial, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
SETS'2007: South European Test Seminar, Sestrière, Italie, 27 février - 1 mars 2007

[DR32] ***"A comprehensive diagnosis methodology targeting several fault models"***
A. Rousset, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
SETS'2007: South European Test Seminar, Sestrière, Italie, 27 février - 1 mars 2007

[DR33] ***"Impact of threshold voltage deviation in SRAM Core-Cells"***
A. Ney, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
SETS'2007: South European Test Seminar, Sestrière, Italie, 27 février - 1 mars 2007

[DR34] "Test des Mémoires Flash Embarquées : Analyse de la perturbation entre cellules FloTOx voisines durant une phase de programmation"
O. Ginez, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel, J.-M. Daga
JNRDM'07: Journées Nationales du Réseau Doctoral de Microélectronique, Lille, France, 14-16 mai 2007

[DR35] ***"Embedded Flash Testing"***
O. Ginez, J.-M. Daga, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
GDR SOC-SIP'07: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2007

[DR36] ***"Test et testabilité de structures numériques tolérantes aux fautes"***
J. Vial, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
GDR SOC-SIP'07: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2007

[DR37] ***"Resistive-Open Defect Influences in SRAM I/O Circuitry"***
A. Ney, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel, M. Bastian
GDR SOC-SIP'07: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2007

[DR38] ***"Méthode de diagnostic unifiée pour circuits intégrés numériques"***
A. Rousset, A. Bosio, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel
GDR SOC-SIP'07: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2007

[DR39] ***"Yield Improvement, Fault-Tolerance to the Rescue? "***
J. Vial, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
SETS'2008: South European Test Seminar, University Center Obergurgl, Austria, 18-22 mars 2008

[DR40] ***"Améliorer le Rendement grâce aux Structures Tolérantes aux Fautes"***
J. Vial, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
DOCTISS'08: Journées des Doctorants de l'Ecole Doctorale I2S, Montpellier, France, 2008

[DR41] ***"Utilisation de structures tolérantes aux fautes pour augmenter le rendement"***
J. Vial, C. Landrault, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel
JNRDM'08: Journées Nationales du Réseau Doctoral de Microélectronique,

[DR42] ***"Tolérer Plus pour Fabriquer Plus"***
J. Vial, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
GDR SOC-SIP'08: Colloque GDR SoC-SiP, Paris, France, 4-6 juin 2008

[DR43] ***"A History-Based Technique for Faults Diagnosis in SRAMs"***
A. Ney, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, M. Bastian
GDR SOC-SIP'08: Colloque GDR SoC-SiP, Paris, France, 4-6 juin 2008

[DR44] ***"Test and Reliability of NAND Flash Memories"***
P.-D. Mauroux, A. Virazel, P. Girard, S. Pravossoudovitch
SETS'2009: South European Test Seminar, 2009

[DR45] ***"Analysis of Resistive-Bridging Defects in SRAM Core-Cell: Impact within the Core-Cell and in the Memory Array"***
R. Alves Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, N. Badereddine
ETS'2009 : European Test Symposium, Sevilla, Spain, 25-29 mai 2009.

[DR46] ***"A Logic Diagnosis Approach for Sequential Circuits"***
Y. Benabboud, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, L. Bouzaida and I. Izaute
ETS'2009 : European Test Symposium, Sevilla, Spain, 25-29 mai 2009.

[DR47] ***"SoC Yield Improvement for Future Nanoscale Technologies"***
J. Vial, A. Virazel, A. Bosio, L. Dilillo, P. Girard, C. Landrault, S. Pravossoudovitch
ETS'2009 : European Test Symposium, Sevilla, Spain, 25-29 mai 2009.

[DR48] ***"Trade-off between Power Dissipation and Delay Fault Coverage for LOS and LOC Testing Schemes"***
F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, X. Wen
LPonTR'09: 2nd International Workshop on Impact of Low-Power design on Test and Reliability, Sevilla, Spain, 29 mai 2009.

[DR49] ***"Test des Mémoires FLASH NAND"***
P.-D. Mauroux, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch
GDR SOC-SIP'09: Colloque GDR SoC-SiP, Paris, France, 10-12 juin 2009

[DR50] ***"SRAM Core-cell Quality Metrics"***
R. Alves Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel
GDR SOC-SIP'09: Colloque GDR SoC-SiP, Paris, France, 10-12 juin 2009

[DR51] ***"Trade-off between Power Dissipation and Delay Fault Coverage For LOS and LOC Testing Schemes"***
F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel
GDR SOC-SIP'09: Colloque GDR SoC-SiP, Paris, France, 10-12 juin 2009

[DR52] ***"Setting Test Conditions for Detecting Faults Induced by Random Dopant Fluctuation in SRAM Core-Cells"***
R. Alves Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, N. Badereddine
VARI'10: European Workshop on CMOS Variability, Montpellier, France, 26-27 mai 2010

[DR53] ***"Power Reduction Through X-filling of Transition Fault Test Vectors for LOS Testing"***
F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, X. Wen
LPonTR'10: 3rd International Workshop on Impact of Low-Power design on Test and Reliability, Prague, Czech Republic, 27-28 mai 2010.

[DR54] ***"Analysis and Fault Modeling of Actual Resistive Defects in Flash Memories"***
P.-D. Mauroux, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch
JNRDM'10: Journées Nationales du Réseau Doctoral de Microélectronique. Montpellier, France, 7-9 juin 2010

[DR55] ***"Analyse et modélisation des défauts résistifs affectant les mémoires Flash"***
P.-D. Mauroux, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, B. Godard, G. Festes, L. Vachez
GDR SOC-SIP'10: Colloque GDR SoC-SiP, Cergy, France, 9-11 juin 2010

[DR56] ***"Test Relaxation and X-filling to Reduce Peak Power During At-Speed LOS Testing"***
F.Wu, L.Dilillo, A.Bosio, P.Girard, S. Pravossoudovitch, A. Virazel, M. Tehranipoor, K. Miyase, X. Wen, N. Ahmed
GDR SOC-SIP'10: Colloque GDR SoC-SiP, Cergy, France, 9-11 juin 2010

[DR57] ***"Tolérance aux Fautes et Rendement de Fabrication"***
D. A. Tran, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, H-J Wunderlich
GDR SOC-SIP'10: Colloque GDR SoC-SiP, Cergy, France, 9-11 juin 2010

[DR58] ***"Robustness Improvement of Digital Circuits A New Hybrid Fault Tolerant Architecture"***
D. A. Tran, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, H.-J. Wunderlich
JNRDM'11: Journées Nationales du Réseau Doctoral de Microélectronique, Paris, France, 23-25 mai 2011

[DR59] ***"A Hybrid Fault Tolerant Architecture for Robustness Improvement of Digital Circuits"***
D. A. Tran, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, H-J Wunderlich
GDR SOC-SIP'11: Colloque GDR SoC-SiP, Lyon, France, 15-17 juin 2011

[DR60] ***"Test and Reliability of Magnetic Random Access Memories"***
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch
GDR SOC-SIP'11: Colloque GDR SoC-SiP, Lyon, France, 15-17 juin 2011

[DR61] ***"Optimized March Test Flow for Detecting Memory Faults in SRAM Devices Under Bit Line Coupling"***
L. Zordan, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, N. Badereddine
GDR SOC-SIP'11: Colloque GDR SoC-SiP, Lyon, France, 15-17 juin 2011

[DR62] ***"Variability Analysis of an SRAM Test Chip"***
R. Alves Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, N.

Badereddine
ETS'2011 : European Test Symposium, Trondheim, Norvège, 23-27 mai 2011

[DR63] ***"Simultaneous Power and Thermal Integrity Analysis for 3D Integrated Systems"***
A. Todri, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel
LPonTR'2011 : IEEE International Workshop on Impact of Low-Power design on Test and Reliability European Test Symposium, Trondheim, Norvège, 26-27 mai 2011

[DR64] ***"Mapping Test Power to Functional Power Through Smart X-Filling for LOS Scheme"***
F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, M. Tehranipoor, K. Miyase, X. Wen, N. Ahmed
LPonTR'2011 : IEEE International Workshop on Impact of Low-Power design on Test and Reliability, Trondheim, Norvège, 26-27 mai 2011

[DR65] ***"A Robust Infrastructure for Data Collection and Transfer for a Distributed SRAM-based Neutron Detection Platform"***
L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel
DDT'2011 : 1st Workshop on Dependability Issues in Deep-submicron Technologies, Trondheim, Norvège, 26-27 mai 2011

[DR66] ***"Analysis of Resistive-Open Defects in TAS-MRAM Array"***
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Tordri, G. Prenat, K. Mackay
ITC'11: International Test Conference, Anaheim, USA, 18-23 septembre 2011

[DR67] ***"Resistive-Open Defects Affecting Bit-Line Selection in TAS-MRAM Architectures "***
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri
JNRDM'12: Journées Nationales du Réseau Doctoral de Microélectronique, Marseille, France, 18-20 mai 2012

[DR68] ***"Electro-Thermal Analysis of 3D Power Delivery Networks"***
A. Todri, A. Bosio, L. Dilillo, P. Girard, A. Virazel
DAC'12 : Design Automation Conference, Work-In-Progress Session, San Fransisco, USA, 3-7 Juin 2012

[DR69] ***"Defect Localization Through an Effect-Cause based Intra-Cell Diagnosis"***
Z. Sun, A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel, E. Auvray
GDR SOC-SIP'12: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2012

[DR70] ***"Impacts of Resistive-Open Defects in the Word-Line Selection of TAS-MRAMs"***
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri
GDR SOC-SIP'12: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2012

[DR71] ***"Through-Silicon-Via Resistive-Open Defect Analysis"***
C. Metzler, A. Todri, A. Bosio, L. Dilillo, P. Girard, A. Virazel
GDR SOC-SIP'12: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2012

[DR72] ***"Adaptive Voltage Scaling via Effective On-Chip Timing Uncertainty Measurements"***
M. Valka, A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel, P. Debaud
GDR SOC-SIP'12: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2012

[DR73] ***"Dynamic Mode Testing of SRAMS under Neutron Radiation"***
G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, A. Todri, A. Virazel
GDR SOC-SIP'12: Colloque GDR SoC-SiP, Paris, France, 13-15 juin 2012

[DR74] ***"Improving Defect Localization Accuracy by means of Effect-Cause Intra-Cell Diagnosis at Transistor Level"***
Z. Sun, A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel, E. Auvray
SDD'12 : International Workshop on Silicon Debug and Diagnosis, Anaheim, USA, 8-9 novembre 2012

[DR75] ***"Performance Evaluation of Capacitive defects on TAS-MRAMs"***
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri
GDR SOC-SIP'13: Colloque GDR SoC-SiP, Lyon, France, 10-12 juin 2013

[DR76] ***"Investigating Multiple-Cell-Upsets on a 90mn SRAM"***
G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, A. Todri, A. Virazel
GDR SOC-SIP'13: Colloque GDR SoC-SiP, Lyon, France, 10-12 juin 2013

[DR77] ***"Fault-Effect Propagation Based Intra-cell Scan Chain Diagnosis"***
Z. Sun, A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel, E. Auvray
GDR SOC-SIP'13: Colloque GDR SoC-SiP, Lyon, France, 10-12 juin 2013

[DR78] ***"A Fault-tolerant Architecture for Pipelined Microprocessor Cores"***
A. Wali, A. Virazel A. Bosio, L. Dilillo, P. Girard
GDR SOC-SIP'14: Colloque GDR SoC-SiP, Paris, France, 11-13 juin 2014

[DR79] ***"A Comprehensive Evaluation of Functional Programs for Power-Aware Test"***
A. Touati, A. Bosio, L. Dilillo, P. Girard, A. Virazel
GDR SOC-SIP'14: Colloque GDR SoC-SiP, Paris, France, 11-13 juin 2014

[DR80] ***"Crosstalk and Supply Noise - Aware Pattern Generation for Delay Testing"***
A. Asokan, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel
GDR SOC-SIP'14: Colloque GDR SoC-SiP, Paris, France, 11-13 juin 2014

PARTIE 4 : ARTICLES SIGNIFICATIFS

Cette partie présente 5 articles majeurs convrant mes thématiques de recherche.

Thème : Test de Pannes Temporelles

[RE4] ***"High Defect Coverage with Low Power Test Sequences in a BIST Environment"***
P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel, H.-J. Wunderlich
IEEE Design & Test of Computers, vol 19, No 5, pp 44-52
Revue publiée par IEEE Computer Society Press, ISSN 0740-7475, Septembre 2002

Thème : Test de Mémoires

[RE5] ***"Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test"***
S. Borri, M. Hage-Hassan, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel
Journal of Electronic Testing Theory and Applications, vol 21, No 2, pp 169-179
Revue publiée par Springer Science, ISNN 0923-8174, Avril 2005

[RE12] ***"A SPICE-Like 2T-FLOTOX Core-Cell Model for Defect Injection and Faulty Behavior Prediction in eFlash"***
O. Ginez, J.-M. Daga, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
Journal of Electronic Testing Theory and Applications, vol 25, No 2-3, pp 127-144
Revue publiée par Springer Science, ISNN 0923-8174, juin 2009

[RE24] ***"A Complete Resistive-Open Defect Analysis for Thermally Assisted Switching MRAMs"***
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri, J.Alvarez-Herault et K. McKay,
IEEE Transaction on Very Large scale Integration Systems,
Digital Object Identifier 10.1109/TVLSI.2013.2294080, 2014

Thème : Tolérance aux Fautes

[RE14] **"*Is TMR Suitable for Yield Improvement?*"**
J. Vial, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel
IET Computers and Digital Techniques, vol. 3, No 6, pp 581-592
Revue publiée par IET, ISSN 1751-8601, novembre 2009

High Defect Coverage with Low-Power Test Sequences in a BIST Environment

Patrick Girard, Christian Landrault, and Serge Pravossoudovitch
LIRMM

Arnaud Virazel and Hans-Joachim Wunderlich
University of Stuttgart

A new technique, random single-input change (RSIC) test generation, generates low-power test patterns that provide a high level of defect coverage during low-power BIST of digital circuits. The authors propose a parallel BIST implementation of the RSIC generator and analyze its area-overhead impact.

TESTING RANKS among the most expensive and difficult aspects of the circuit design cycle, driving the need for innovative solutions. To this end, researchers have proposed built-in self-test (BIST) as a powerful DFT technique for addressing highly complex VLSI testing problems. BIST designs include on-chip circuitry to provide test patterns and analyze output responses. Performing tests on the chip greatly reduces the need for complex external equipment.

The most commonly used fault model for BIST of digital systems is the classical single stuck-at fault model. However, in the new CMOS nanometer technologies, defects do not always behave as stuck-at faults do.[1] Therefore, test generation based on the stuck-at model alone is no longer sufficient for obtaining high defect coverage.[2] A straightforward solution covering many misbehaviors that can occur in digital circuits would be to use multiple test generation techniques, each targeting a specific fault type (such as stuck-at, delay, or bridging). However, this solution is costly and impractical from a BIST viewpoint.

An alternative solution might be the use of a single on-chip test pattern generator providing "universal" test sequences—sequences that target both conventional (stuck-at) and unconventional (delay, bridging, and stuck-open) fault types. The problem with this solution is that test application consumes excessive power because switching activity is significantly higher during test than during system mode.[3] A standard test pattern sequence produced by a linear feedback shift-register (LFSR) consists of random multiple-input change (RMIC) patterns with a switching-activity rate of 0.5 (that is, an equal likelihood of 0 and 1). In this article, we propose a new BIST test generation technique that reduces the switching activity of test patterns generated during BIST while increasing the defect coverage. The technique, called random single-input change (RSIC), generates test patterns capable of detecting many different faulty behaviors. Moreover, RSIC test sequences have a low rate of switching activity.

Basic definitions

Fault models describe a faulty system's logical behavior. In our work, we use the bridging, path delay, and single stuck-at fault models to analyze the effectiveness of test sequences produced by RSIC generation.

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Fault models

We can view a bridging fault as an unintentional short between two lines. This short can be a nonresistive short, such that the two lines are always brought into equilibrium at the same potential, or a resistive short, such that the shorted lines have different potentials. Researchers have proposed several models for resistive and nonresistive bridging faults, based on the popular wired-AND and wired-OR models used to model the effects of bridging faults in bipolar logic.[4] Although the coverage of a bridging fault by both wired-AND and wired-OR behavior does not always guarantee detection, these models are easy to use for bridging-fault simulation. To allow experiments with a larger number of benchmark circuits, the work described in this article used such models to represent bridging defects.

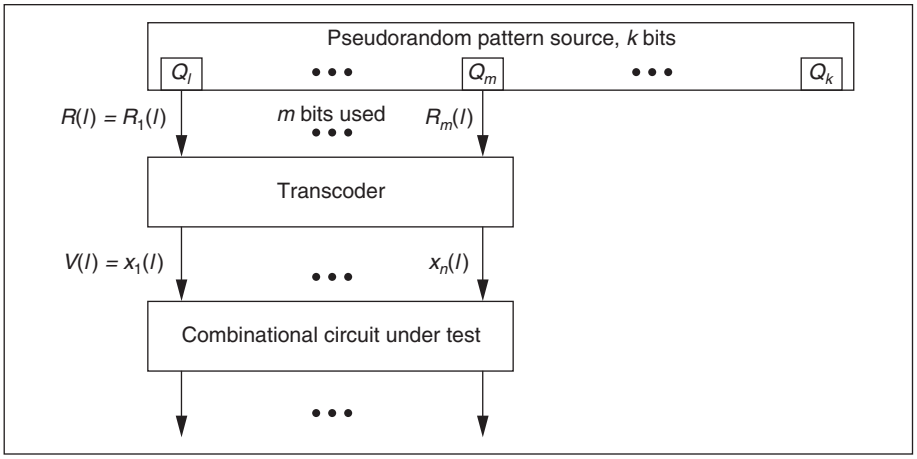

Figure 1. Generation principle of an RSIC test sequence.

Some defects in a manufactured circuit do not affect its logic function; rather, they change its delays, thus changing its operating speed. These are delay defects, and a widely studied delay fault model is the path delay fault model.[5] The main advantage of the path delay fault model is that it models the distributed delay defects more accurately than other delay fault models, particularly the gate delay fault model.

A test for a path is robust if it can detect a delay fault on that path irrespective of other delays and delay faults in the circuit; otherwise, it is nonrobust.[5] A robust test is preferable because a single defect usually affects many paths.

Test sequences

Two-pattern tests might differ in multiple bit positions. In that case, they are called multiple-input change (MIC) pattern pairs. Test pairs that differ in only one bit position are called single-input change (SIC) pattern pairs. We now define what an RSIC sequence should be in theory. Let

$$S = V(1)V(2) \ldots V(l) \ldots V(L)$$

be a test sequence composed of L successive n-bit vectors $V(l)$. Each vector takes a value from the set

$$V = \{V_0, V_1, \ldots, V_{2^n-1}\}$$

where V_j corresponds to the n-bit vector $(x_1, x_2, \ldots, x_n)$ associated with decimal value j. For example, for $n = 5$, $V_9 = 01001$; that is, $x_1 = x_3 = x_4 = 0$ and $x_2 = x_5 = 1$. In an RMIC sequence, the probability $\Pr[V(l) = V_j] = 2^{-n}$ for any l and any j, and the probability $\Pr[V(l) = V_j]$ is independent of the values $V(i)$, where $i = 1, 2, \ldots, l-1$.

In an RSIC sequence, this probability is

$$\Pr[V(l) = V_j \mid V(l-1) = V_k] = 1/n, \quad \text{if and only if } |j-k| = 2^a \qquad (1)$$

where $a \in \{0, n-1\}$. In other words, for any $l > 0$, $V(l)$ differs from $V(l-1)$ by exactly one bit randomly drawn, and this bit must be independent of the bits previously drawn.

Hardware generation of random test sequences

Figure 1 represents the basic RSIC generation principle.[6] The structure uses a k-bit random source, which can be a random number obtained from a maximal-length LFSR. The value of vector $Q_1Q_2 \ldots Q_k$ changes at each clock cycle of the test session. At each time l, the transcoder uses a subset of m bits ($m \le k$). The transcoder transforms vector $R(l) = R_1(l)R_2(l) \ldots R_m(l)$ into n-bit vector $V(l) = x_1(l)x_2(l) \ldots x_n(l)$,

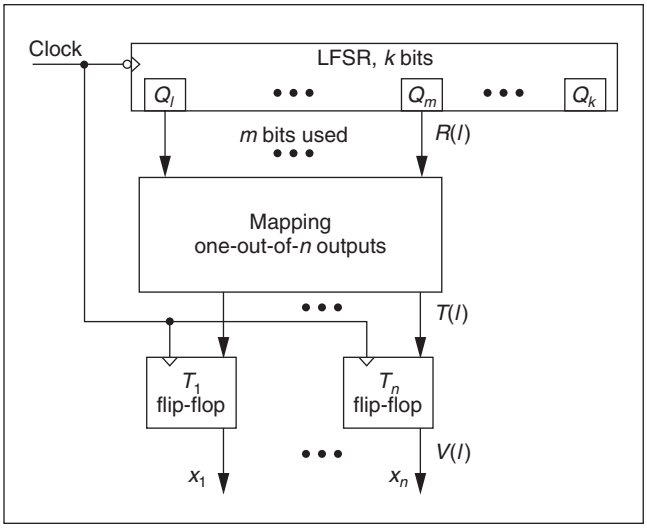

Figure 2. Hardware generation of an RSIC test sequence.

which is applied to a combinational circuit under test. The definition of an RSIC sequence requires the following conditions:

- $R(l)$ is independent of $R(l-1)$.
- The transcoding between $R(l)$ and $V(l)$ satisfies Equation 1, at least approximately.
- The period of sequence $S = V(1)V(2) \ldots V(l) \ldots V(L)$ is at least equal to test length L.

The period of the RSIC sequence generated from an appropriate structure according to the RSIC principle is $2 \times (2^k - 1)$,[6] if length k of the pseudorandom source obeys the relationship $2 \times (2^k - 1) > L$; that is,

$$k > \log_2(L/2 + 1) \approx \log_2(L/2)$$

Researchers have proposed structures for generating RMIC sequences in which two consecutive patterns are independent. René David[7] obtains RMIC test sequences from a combination of LFSRs in which more than one shifting (σ) occurs between two consecutive vectors.

Similarly, David obtains RSIC test sequences from the hardware structure shown in Figure 2. This structure maps vector $R(l)$ coming from the modified LFSR into a one-out-of-n vector $T(l)$ and applies every component of $T(l)$ to the input of a T flip-flop. Hence, given random vector $R(l)$, this mapping implies random trigger input $T_i(l) = 1$ and other trigger inputs $T_j(l) = 0$ for $j \neq i$. Therefore, $V(l)$ is similar to $V(l-1)$ apart from the value of x_i. The mapping cell must be a one-out-of-n decoder.

This hardware RSIC generator has the following theoretical properties:

- The LFSR is of maximal length (period $2^k - 1$), and $2 \times (2^k - 1) > L$;
- $m \geq \lceil \log_2 n \rceil$;
- the number of shifts σ is such that $1 \leq \sigma < 2^k - 1$, and σ does not share a common factor with $2^k - 1$; and
- b_j is the number of m-bit vectors associated with T_j:

$$\max_{j \in \{1,\ldots,n\}} b_j - \min_{j \in \{1,\ldots,n\}} b_j \leq 1.$$

RSIC test efficiencies

We performed tests to compare the effectiveness of RSIC test sequences with that of RMIC sequences in terms of delay, bridging, and single stuck-at fault coverage.

Delay fault testing

For delay fault testing, we used a case study corresponding to experiments performed with the combinational part of circuit s382 of the 1989 International Symposium on Circuits and Systems (ISCAS) benchmark set. We base our performance evaluation of the RSIC and RMIC test sequences on results we obtained using a deterministic automatic test-pattern generation (ATPG) tool. We use the following notations:

- *FC_ATPG robust*. Robust fault coverage obtained.
- *FC_ATPG nonrobust*. Nonrobust fault coverage obtained.
- *Ld*. Test length obtained by an ATPG tool on the path delay fault model with a complete efficiency.

Using the ATPG information, we computed the results provided by fault simulation with the RSIC and RMIC test sequences. We obtained the following efficiencies:

Table 1. Robust and nonrobust efficiencies of given RMIC and RSIC sequences run on a combinational part of the s382 benchmark circuit.

Multiple of deterministic test length	Length (no. of patterns)	RMIC sequence		RSIC sequence	
		Eff_R %	*Eff_NR* %	*Eff_R* %	*Eff_NR* %
—	10	12.78	16.49	1.70	1.63
—	100	25.57	52.04	14.35	15.40
Ld/4	349	30.97	73.97	24.57	25.61
Ld/2	699	33.09	86.78	43.47	46.05
Ld	1,398	33.24	91.01	52.84	57.22
2*Ld*	2,796	33.52	96.86	61.36	66.49
5*Ld*	6,990	33.52	99.31	76.56	84.33
10*Ld*	13,980	33.52	99.86	81.53	90.32
20*Ld*	27,960	33.52	99.86	86.65	96.19
50*Ld*	69,900	33.52	99.86	89.06	98.64
100*Ld*	139,800	33.52	99.86	90.19	99.73
—	1,000,000	33.52	99.86	90.48	100.00

- *Eff_R*. The robust fault efficiency achieved by RSIC or RMIC test sequences is

  $$Eff\_R = 100 \times (FC\ robust / FC\_ATPG\ robust)$$

  where *FC robust* is the fault coverage achieved by the fault simulation.
- *Eff_NR*. The nonrobust fault efficiency achieved by RSIC or RMIC test sequences is

  $$Eff\_R = 100 \times (FC\ nonrobust / FC\_ATPG\ nonrobust)$$

  where *FC nonrobust* is the fault coverage achieved by the fault simulation.

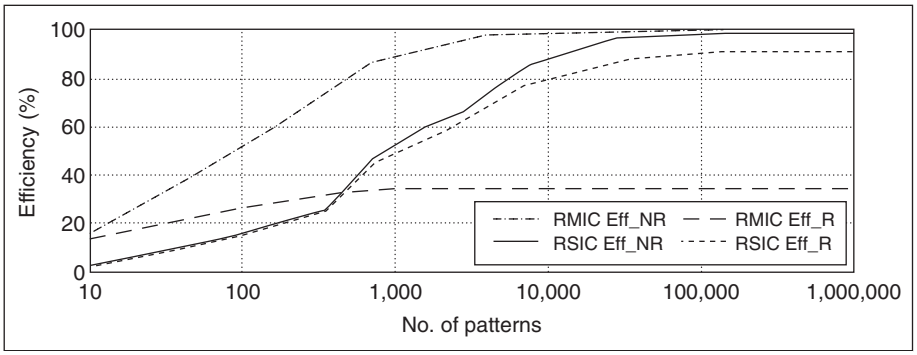

Figure 3. Efficiency comparison of RMIC and RSIC sequences on the s382 benchmark circuit.

Basic results. Table 1 presents simulation results obtained from one RMIC sequence and one RSIC sequence. The table shows results for various test lengths as multiples of required deterministic test length *Ld*. Figure 3 is a graphical representation of the results given in Table 1.

From these results, we make the following observations:

- The RSIC sequence's robust efficiency is close to its nonrobust efficiency, whereas there is a huge gap between these efficiencies for the RMIC sequence. The reason is that most of the tests in the RSIC sequence are robust because of the adjacency of successive vectors.
- For very short test lengths (which are uninteresting in practice), the RSIC test sequence's fault efficiencies are lower than those of the RMIC sequence. For medium-range test lengths, the RMIC sequence's nonrobust efficiency is higher than that of the RSIC sequence, whereas the RSIC sequence is higher in robust efficiency.
- For long test lengths, the RSIC test sequence can equal the RMIC sequence in nonrobust efficiency, but it is much higher in robust efficiency.

Table 2. Actual efficiencies for various success rate (S_{NR}) assumptions.

	RMIC sequence			RSIC sequence		
Length (no. of patterns)	*EFF* (S_{NR} = 10%)	*EFF* (S_{NR} = 50%)	*EFF* (S_{NR} = 90%)	*EFF* (S_{NR} = 10%)	*EFF* (S_{NR} = 50%)	*EFF* (S_{NR} = 90%)
10	12.60	13.98	15.36	1.63	1.60	1.58
50	21.92	27.88	33.83	8.51	8.78	9.06
100	26.98	36.82	46.66	13.86	14.25	14.64
349	33.69	49.67	65.65	23.66	24.05	24.43
699	36.72	56.67	76.62	41.92	42.88	43.84
1,398	37.24	58.71	80.18	51.08	52.71	54.34
2,796	38.03	61.57	85.11	59.32	61.23	63.13
6,990	38.26	62.71	87.16	74.14	77.03	79.91
13,980	38.31	62.96	87.61	79.01	82.27	85.54
27,960	38.31	62.96	87.61	83.98	87.53	91.07
69,900	38.31	62.96	87.61	86.30	89.86	93.42
139,800	38.31	62.96	87.61	87.38	90.92	94.47
1,000,000	38.31	62.96	87.61	87.65	91.19	94.73

In summary, the RMIC sequence achieves better nonrobust efficiency, and the RSIC sequence achieves better robust efficiency (for medium-range test lengths). Later, we try to find a criterion for selecting the best test sequence to target both robust and nonrobust efficiency.

Actual efficiency. During test application, an uncertainty arises as to what proportion of nonrobustly tested faults a sequence really detects. We define actual efficiency (*EFF*) as

$$EFF(S) = Eff\_NR \times S \quad (2)$$

Success rate S is the proportion of faults really detected during the test. For a robust test set, the success rate is $S_R = 1.0$, and *FC_robust* is the portion of the corresponding faults. The portion of faults that are nonrobustly testable but do not have a robust test pattern is *FC_nonrobust* – *FC_robust*, and the corresponding test set has success rate $S_{NR} < 1.0$. Hence, the overall success rate is

$$\begin{aligned} S &= FC\_robust \times S_R + (FC\_nonrobust - FC\_robust) \times S_{NR} \\ &= FC\_robust \times (1.0 - S_{NR}) + FC\_nonrobust \times S_{NR} \end{aligned}$$

Table 2 shows the efficiency results of applying Equation 2 to circuit s382 for the RMIC and RSIC test sequences and for S_{NR} = 10%, 50%, and 90%. For a long test length, actual efficiency is higher for the RSIC sequence than for the RMIC sequence, for all assumed values of S_{NR}.

These results demonstrate that even with a lower nonrobust delay fault coverage, RSIC test sequences often produce better test quality than do RMIC delay test sequences. This conclusion, drawn from a study of circuit s382, is also valid for most of the ISCAS89 benchmark circuits.[8]

Stuck-at and bridging fault testing

Table 3 shows that for stuck-at fault coverage, the effectiveness of RSIC generation in comparison with RMIC generation mainly depends on the test sequence's length. For lengths of 10,000, the fault efficiency of RMIC test sequences is slightly higher than that of RSIC test sequences. This is also true for lengths below 10,000. But when the length increases beyond 10,000, the efficiency of RSIC test sequences becomes comparable to that of RMIC test sequences. For a test length equal to that used for delay fault testing, the fault efficiency is nearly the same for both types of sequences.

The same conclusion is true for bridging-fault coverage, as Table 4 shows. For each

Table 3. Comparison of RSIC and RMIC generation for single stuck-at fault coverage.

Circuit	No. of faults	Length (no. of patterns)	RSIC efficiency (%)	RMIC efficiency (%)	Length (no. of patterns)	RSIC efficiency (%)	RMIC efficiency (%)
s386	360	10,000	100.00	100.00	73,600	100.00	100.00
s420	424	10,000	77.12	83.25	132,200	96.10	97.88
s510	538	10,000	100.00	100.00	136,600	100.00	100.00
s1238	1,332	10,000	90.99	97.94	499,200	99.84	100.00
s1494	1,489	10,000	99.66	99.94	351,800	100.00	100.00

Table 4. Comparison of RSIC and RMIC generation for bridging-fault coverage.

			RSIC sequences		RMIC sequences	
Circuit	No. of faults	Length (no. of patterns)	WAND&WOR coverage (%)	WAND||WOR coverage (%)	WAND&WOR coverage (%)	WAND||WOR coverage (%)
s386	390	73,600	99.23	100.00	99.23	100.00
s420	521	132,200	81.23	97.59	81.96	98.89
s510	1,073	136,600	100.00	100.00	100.00	100.00
s1238	2,924	499,200	99.90	100.00	99.90	100.00
s1494	3,851	351,800	99.95	100.00	99.95	100.00

bridging fault, we considered the following behaviors: WAND (wire-AND), WOR (wire-OR), WAND&WOR (the fault is tested if both behaviors are tested), and WAND||WOR (the fault is tested if at least one of the two behaviors is tested). Table 4 reports the results for the most representative WAND&WOR and WAND||WOR models.

RSIC generator implementation

A classical BIST architecture must incorporate a test pattern generator (TPG), a test response evaluator (TRE), and a BIST control unit. State-of-the-art implementations use either of two basic BIST execution options: the serial (test-per-scan) scheme or the parallel (test-per-clock) scheme.[9]

In serial BIST, the TPG shifts test vectors into a serial scan path and then applies them to the circuit under test. Next, it loads test responses into the scan chain and shifts them out to the TRE while shifting in a new test.

In parallel BIST, the TPG applies test vectors at every clock cycle. In the same clock cycle, the TRE captures test responses. This scheme leads to shorter test times than the test-per-scan scheme because the TPG generates a new test pattern in each clock cycle. This scheme can perform a high-speed test at system frequency without any clock delays for shifting. The parallel scheme's drawbacks are its hardware overhead and performance degradation.

BIST environment

The delay-fault detection capability offered by parallel BIST led us to propose a parallel BIST hardware implementation of the RSIC generator. Our test-per-clock design uses modified system registers including built-in logic block observers (BILBOs)[10] and concurrent built-in logic block observers (CBILBOs).[11]

Figure 4a (next page) presents the original circuit, which contains a combinational logic block, an internal state register, and registers at the primary inputs and outputs. Figure 4b shows the standard parallel BIST approach, which changes the input and output registers into BILBOs and the state register into a CBILBO.

Figure 4c shows our RSIC implementation. Here, we added a *k*-stage LFSR and mapping logic. The *k*-stage LFSR is a classical primitive polynomial LFSR. The mapping logic is a simple combinational structure allowing an *m*-bit vector provided by the LFSR to be mapped into

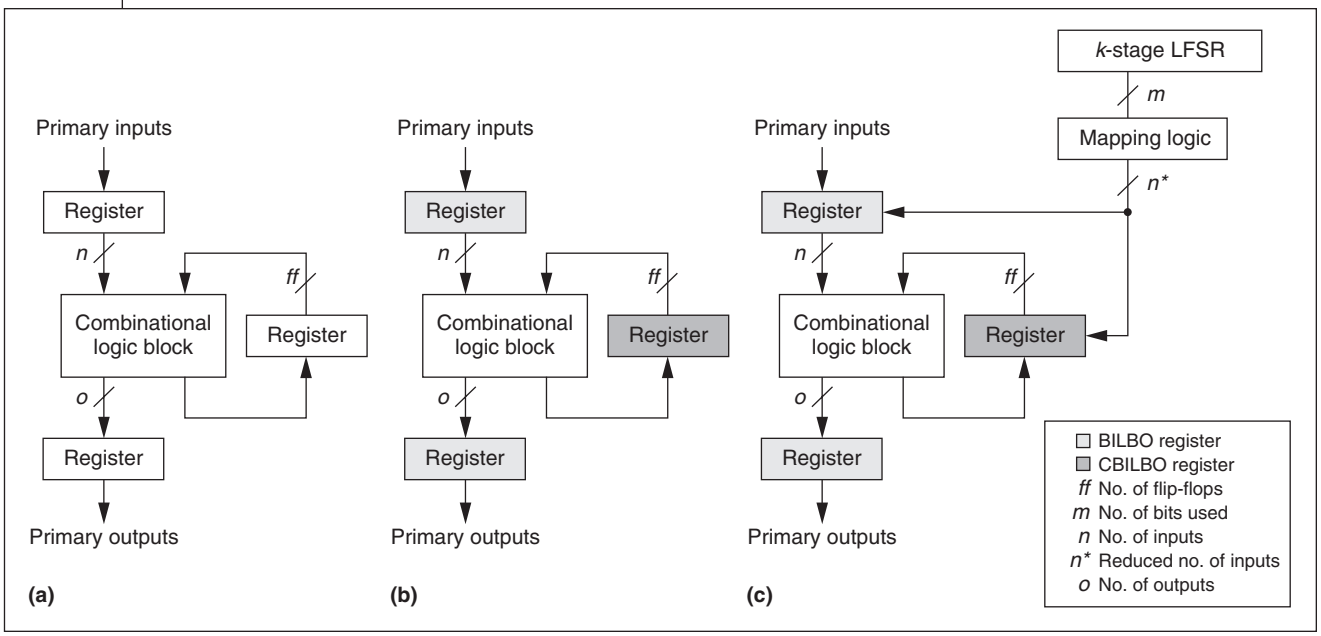

Figure 4. BIST implementations: original (a), classical parallel (b), and RSIC (c) designs.

a one-out-of-*n* vector. We further reduced this logic by identifying compatible inputs of each circuit. Compatible inputs are inputs that belong to the circuit's output cones.[12] We thus reduced the test of an *n*-input circuit to the test of an *n**-input circuit and also reduced the test length. Moreover, we modified the standard BILBO and CBILBO cells to enable hardware generation of RSIC test sequences from the structure in Figure 2 (in T flip-flop mode).

Area overhead

Table 5 shows the proposed RSIC generator's gate count overhead. The column *Cell_area* presents an estimate of the area (in cells only) in each original circuit. Column S_1 reports the area required to modify the registers into BILBOs and CBILBOs, as in the design in Figure 4b. Column S_2 gives the additional area required to transform the original circuit into an RSIC BIST design, as in Figure 4c. The last two columns show the area overhead the RSIC generator imposes on a conventional BILBO architecture, as determined by these two equations:

$$Cost_1 = S_2/S_1$$

$$Cost_2 = (S_2 + Cell\_area)/(S_1 + Cell\_area)$$

$Cost_1$ is the factor by which the RSIC hardware is larger than the RMIC hardware, and $Cost_2$ is the factor by which an RSIC-testable circuit is larger than a circuit with standard BIST.

The $Cost_2$ results show that the additional cost required to generate RSIC test sequences for each circuit is between 19% and 13% for the largest ISCAS89 circuits (s5378 through s38584). This percentage decreases as the circuit size increases. From these results, we can conclude that the RSIC generation method is a practical way to reach a high level of defect coverage for digital-circuit BIST.

Because of the RSIC generation technique's effectiveness, we plan to extend it to system-on-a-chip designs. In SoCs, an embedded processor could use software to generate RSIC sequences. This might increase test application time, but it would not require any extra hardware. ■

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Table 5. Area overhead of the RSIC generator.

Circuit	No. of primary inputs	No. of primary outputs	No. of flip-flops	*Cell_area* (gate equivalents)	S_1 (gate equivalents)	S_2 (gate equivalents)	$Cost_1$	$Cost_2$
s510	25	7	6	435.5	190.5	456.0	2.394	1.424
s526	24	6	21	444.5	286.5	552.0	1.927	1.363
s641	54	24	19	789.0	488.5	867.0	1.775	1.296
s713	54	23	19	813.0	484.0	862.5	1.782	1.292
s820	23	19	5	698.5	228.5	490.5	2.147	1.283
s832	23	19	5	707.5	228.5	490.5	2.147	1.280
s953	45	23	29	822.0	513.5	860.5	1.676	1.260
s1196	32	14	18	890.0	337.5	647.5	1.919	1.253
s1238	32	14	18	919.5	337.5	647.5	1.919	1.247
s1423	91	5	74	1,325.0	954.5	1,620.5	1.698	1.292
s1488	14	19	6	1,166.5	195.0	413.0	2.118	1.160
s1494	14	19	6	1,173.5	195.0	413.0	2.118	1.159
s5378	214	49	179	3,803.5	2,441.0	3,579.0	1.466	1.182
s9234	247	22	228	6,292.5	2,811.0	4,210.5	1.498	1.154
s13207	700	121	669	11,321.5	8,382.0	12,120.5	1.446	1.190
s15850	611	87	597	12,175.0	7,324.5	10,602.0	1.447	1.168
s35932	1,763	320	1,728	29,224.5	21,474.0	28,652.5	1.334	1.142
s38417	1,664	106	1,636	28,850.5	19,421.5	26,527.5	1.366	1.147
s38584	1,464	278	1,452	30,898.5	18,007.5	24,525.5	1.362	1.133

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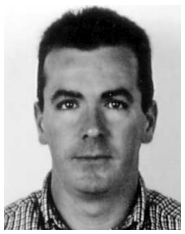

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Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test*†

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Abstract. This paper presents the results of resistive-open defect insertion in different locations of Infineon 0.13 μm embedded-SRAM with the main purpose of verifying the presence of dynamic faults. This study is based on the injection of resistive defects as their presence in VDSM technologies is more and more frequent. Electrical simulations have been performed to evaluate the effects of those defects in terms of detected functional faults. Read destructive, deceptive read destructive and dynamic read destructive faults have been reproduced and accurately characterized. The dependence of the fault detection has been put in relation with memory operating conditions, resistance value and clock cycle, and the importance of at speed testing for dynamic fault models has been pointed out. Finally resistive Address Decoder Open Faults (ADOF) have been simulated and the conditions that maximize the fault detection have been discussed as well as the resulting implications for memory test.

Keywords: memory testing, dynamic faults, address decoders, core-cells

1. Introduction

Functional faults traditionally employed in RAM testing, such as stuck-at, transition and coupling faults [9] are nowadays insufficient to give correct models of the effects produced by some defects that may occur in VDSM technologies. Advances in process manufacturing densities and memory architectures have carried the development of new fault models, which are tightly linked to the internal memory structure [1–3, 10, 20, 23]. These faults are not directly detectable with standard March algorithms and thus they need specific test sequences and, in some cases, *at-speed*

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tests, which are necessary especially for delay fault detection.

Many links have been established between delay faults and resistive-open defects [5, 14]. Resistive-opens generally cause timing-dependent faults. A two-pattern sequence is usually necessary to sensitize the faults, but, in contrast with stuck-open faults, detection of resistive-opens should be performed at-speed.

The occurrence of resistive-open defects has considerably increased in recent technologies, due to the presence of many interconnection layers and an ever-growing number of connections between each layer. In particular in [16] Intel reports that open/resistive vias are the most common root cause of test escapes in deep-submicron technologies.

Hence resistive-open defects are the primary target of this study. Resistive defects have been injected in the Infineon 0.13 μm synchronous embedded-SRAM family with the main purpose of verifying the presence of timing-dependent faults. Due to the internal self-timed architecture, two types of timing-dependent faults can be identified:

– Faults whose effect appears after more than one operation. The detection of these faults depends on the clock speed. We have investigated the presence of such faults by inserting resistive-opens in several locations of the memory core-cell.
– Faults affecting the memory external timings. These faults originate from defects in the non-self-timed parts of the memory periphery, thus they depend on input signals timings. In particular we have investigated the effects of resistive defects in the address pre-decoder.

For both types of faults, electrical simulations have been performed with many parameters such as defect size, supply voltage, operating temperature and process corner. Results reported in this paper demonstrate the sensitivity of embedded SRAMs to resistive-open defects and provide a characterization of these defects in terms of timing-dependent fault detection.

In Section 2 the simulation flow is described. Section 3 shows the most relevant results with regard to the identified fault models for each injected defect. Test implications are discussed in Section 4. Finally, Section 5 summarizes the results of the study and gives some directions for future works.

2. Simulation Flow

All electrical simulations have been performed with the Infineon internal SPICE-like simulator. A reference 8 K $\times$ 32 memory structure has been considered, organized as an array of 512 word lines $\times$ 512 bit lines. In order to reduce the simulation time, the simulations have been performed using a simplified version of the memory circuit that includes a reduced set of core-cells and all peripherals of the memory as pre-charge devices, sense amplifiers, write drivers, output buffers and the column and row address decoders.

2.1. Core-Cell Simulations

Several resistive-open defects have been analyzed in the memory core-cell. Fig. 1 depicts the scheme of a standard 6-transitors cell with six different resistive-open defects. The first criterion for the choice of the defect location is layout dependent. The defects have been injected in correspondence with the interconnections where there is a higher probability of their presence. Moreover, some locations have been discarded due to the symmetry of the structure. For example we have considered the defects only on one of the two inverters.

The whole operating environment range has been selected in order to maximize the fault detection probability. Hence simulations have been performed by the variation of the following parameters:

- Process corner: slow, typical, fast
- Supply voltage: 1.35 V, 1.5 V, 1.6 V
- Temperature: -40°C, 27°C, 125°C

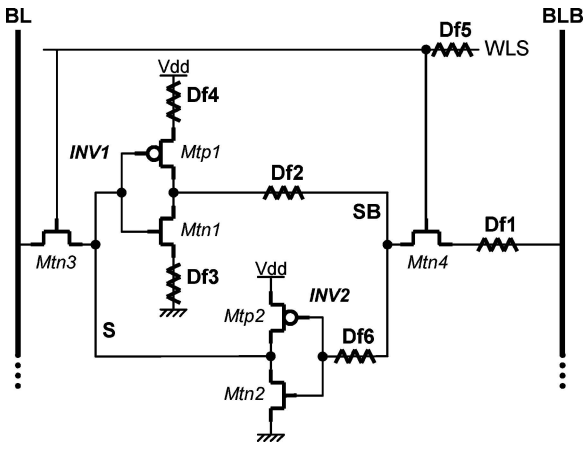

Fig. 1. Resistive-open defects injected in the memory core-cell.

- Resistance values have been chosen from few Ωs up to several MΩs since a large range of possible values have been reported [19].

When we have identified a timing-dependent behavior, we have performed more precise simulations in order to explore the connections between fault and memory timing parameters, such as clock cycle and address setup time.

2.2. *Address Decoder Simulations*

When a resistive-open defect appears between gates (inter-gate defects), it produces faults that can be detected by standard March tests. When the defect is located inside the gate (intra-gate defect) and in particular in the parallel plan of transistors, it produces dynamic fault due to its sequential behavior [21]. Referring to the NOR-gate of Fig. 2, such a defect has been located in the drain of transistor TN1 and it may produce a delay during the pull-down of node ZA0. This fault is a dynamic one because it needs a specific sequence of operations (read and write) with a specific address sequence.

In the memory under study, only the X and Y predecoders are subject to this fault, since the remaining part of the decoder is activated by an internally generated enable signal and is thus insensitive to the specific address sequence. Hence a resistive defect has been injected in the pull-down path of the NOR-based word line pre-decoder. Referring to Fig. 2, the fault has to be sensitized by applying a $0 \rightarrow 1$ transition on the A0 input, and keeping A1 at zero. This means that WL0 is selected, followed by WL1. Normally when a new word line is selected the previous one is automatically de-selected. If a resistive defect is present, the ZA0 output may stay high for more than one access cycle, due to a memory effect of the node ZA0. The consequence is that WL0 remains selected a certain time (depending on the defect size) when WL1 is selected.

The following sequence has been used to sensitize and detect this dynamic fault:

– *Sensitization*: Write d at WL0, Write $\bar{d}$ at WL1;
– *Detection*: Read WL0. d is expected.

This sequence, originally proposed in [20], will be always called Sachdev-like sequence in the rest of this paper.

A possible alternative (March-like sequence) has also been considered:

– *Sensitization and detection*: Write d for each WL, read d and write $\bar{d}$ for each WL.

The interest of the latter sequence is that it could be integrated in industry-standard March C- tests [15] by using a proper address generator, e.g. the LFSR reported in [18]. The March-like sequence sensitizes and detects the fault during a read operation. In other words there is a double faulty access to two cells with different stored values, during a read operation. Since conflicting values are driven on the bit lines and the final fault detection is uncertain. Detailed simulations have confirmed that the fault detection

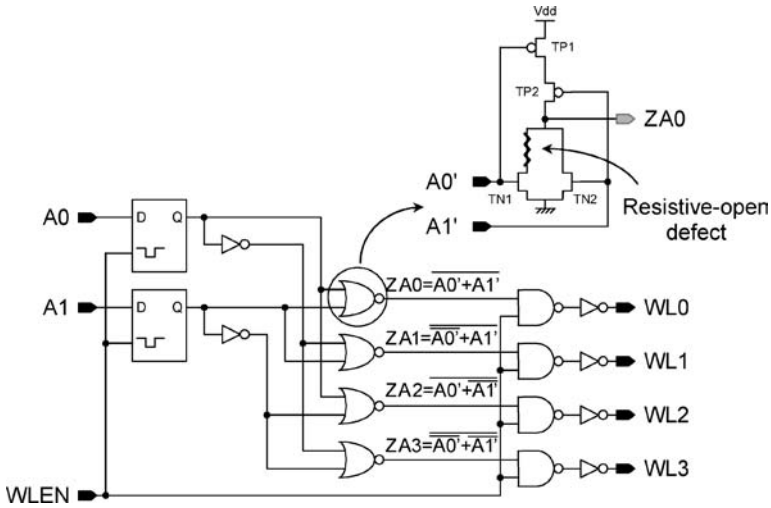

Fig. 2. Intra-gate resistive-open in the pull-down path of NOR-based address pre-decoder.

reliability is very low, while the Sachdev-like sequence is very effective. Therefore we have disregarded the March-like sequence found in bibliography and we have applied only the Sachdev-like sequence for our study.

3. Simulation Results

In the following, the most significant simulation results are presented, with particular emphasis on the detected dynamic fault models. Referring to the classification presented in [11], a fault is considered dynamic if the sequence of operations needed to sensitize it consists of more than one operation. Additionally, in order to characterize precisely the conditions which maximize the fault detection probability, we have analyzed the dependence of the detected faults on the relevant memory timings, e.g. the clock cycle time.

In the presence of resistive-open defects, the detection of a particular fault depends on environmental conditions, such as supply voltage, operating temperature and the considered process corner.

3.1. Core-Cell Simulations

The simulations have been performed with all the different PVT conditions. In Table 1 we show only the most significant results according to the conditions which maximize the fault detection, i.e. the minimum detectable resistance value. The PVT conditions have only an impact on the minimal defect size that induces a faulty behavior but not on the fault model. This means that in all the other cases not shown here, the fault models are still valid but there are related to larger defect size. All the fault models have been detected by 1w0r0 (i.e. '1' stored in the cell, a w0 operation immediately followed by a r0) or 0w1r1 sequences.

Table 1. Summary of worst-case PVT corners for the defects of Fig. 1 and corresponding minimum detected resistance and fault model.

Dfi	Process corner	Voltage (V)	Temp (°C)	Min res (kΩ)	Fault model
1	Fast	1.6	−40	∼25	TF
2	Fast	1.6	–	∼8	RDF/DRDF
3	Fast	1.6	125	∼3	RDF/DRDF
4	Fast	1.6	125	∼130	Dynamic RDF
5	Fast	1.6	−40	100/140	IRF/TF
6	Fast	1.6	125	∼2 MΩ	TF

In this table the first column (Dfi) indicates the defect location in the core-cell. The following four columns correspond to the electrical parameters which maximize the fault detection. The last column gives the corresponding fault models that have the following definitions:

- *Transition Fault (TF)*: A cell is said to have a TF if it fails to undergo a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written.
- *Read Destructive Fault (RDF)* [2]: A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output.
- dynamic Read Destructive Fault (dRDF) [11, 13]: A cell is said to have an dRDF if a write operation immediately followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output.
- *Deceptive Read Destructive Fault (DRDF)* [2]: A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell.
- *Incorrect Read Fault (IRF)*: A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell.

A general result is that fault detection is usually better at high voltage with a fast process, while it can greatly vary with the operating temperature. When a fast process is adopted, high supply voltage makes the memory surprisingly less stable than a lower supply voltage. This unexpected phenomenon is a consequence of the decrease of stability of the core cell due to the fast process that maximizes the leakage and the threshold voltage. For high supply voltage, the commutations become quicker as the voltage difference gets higher. In this condition the cell is more sensitive to any perturbation. Moreover leakage is enforced at high temperature while voltage threshold is minimal at low temperature. The presence of effects of second or third order does not make it easy to determine exactly which of them is predominant.

Defects in the Cell Pull-Down. A resistive defect in the pull-down path of one of the core-cell inverters (Df3 in Fig. 1) may cause a destructive read operation [2]. The read value can be wrong or correct, thus a second

read access is necessary to detect the fault (*deceptive destructive read*).

The impact of the defect on memory robustness has been taken into account since the fault detection is more or less reliable depending on the voltage difference between BL and BLB during the read access (referred to as ΔBL). As a reference for this technology, we consider a "good" absolute value of ΔBL to be higher than 80 mV. When ΔBL is lower than 80 mV a wrong value can be read during the access because of transistor mismatches in the sense amplifier or for low-drive core cell. Nevertheless, since these effects are not taken into account in standard "perfect" Spice simulations, the simulated read value will always be the correct one. Hence it is extremely important to characterize the impact of the defect also in terms of variations of ΔBL compared to its reference value.

The simulation results, in presence of Df3, are shown in Fig. 3 for a typical process at room temperature and 1.5 V supply voltage. Still referring to the notation presented in [11], the operation sequence considered here is: 0w1r1 ('0' previously stored, operation of w1 and r1). However this read disturb fault can be considered static, since the single-operation sequence 1r1 has shown the same sensitization effect. Likewise, additional read accesses did not improve the fault detection.

It is important to note that, even though a destructive read (a.k.a. read disturb) takes place for resistance values higher than $\sim$7 kΩ, the reduction in ΔBL affects the memory robustness starting from a value of $\sim$4.5 kΩ. Besides, in the entire RDF region corresponding to a read disturb fault, the fault detection is considered uncertain, because ΔBL is consistently lower than the 80 mV "safe" value. Thus a second read access is always necessary to ensure proper fault detection, regardless of the simulation outcome. A deceptive read disturb is also identified in simulation for a resistance value of 7.5 kΩ.

Defects in the Cell Pull-Up. A resistive defect in the pull-up path of one of the core-cell inverters, as Df4 in Fig. 1, is a classic hard-to-detect fault [11]. When a defect is on Mtp2 source, a *dynamic Read Destructive Fault* occurs when a zero is stored in the cell. A '0' stored correspond to a '0' on node S and a '1' (VDD) on node SB, see Fig. 1.

The first step of the read operation is the precharge at VDD of BL and BLB. Then the cell is connected to the bit lines, the word line signal actives transistors Mtn3 and Mtn4, which are switched on. BLB and node SB are at same potential, while BL and node S have a different potential. As BL has a high capacitance, its discharge is long. So, we can consider that BL and BLB values remain at VDD at the beginning of the read operation. Moreover, the current in Mtn3 is high due to the voltage difference between BL and S (see Fig. 4). The S node is thus charged a little ($0 + \delta$V). As the value at the inverter input has slightly increased, the value at its output (SB) decreases because Mtp2 cannot compensate this leak of charge due to the resistive defect. Consequently, SB voltage decreases a little (VDD $-$ δ V) causing the degradation of the logic '0' on S. If SB value becomes close to VDD/2, there is a swap of the value stored in the cell. Note that, in normal condition, when there is not a resistive defect in the pull-up path, the current in the Mtp2 transistor is sufficient to maintain the SB node close to VDD.

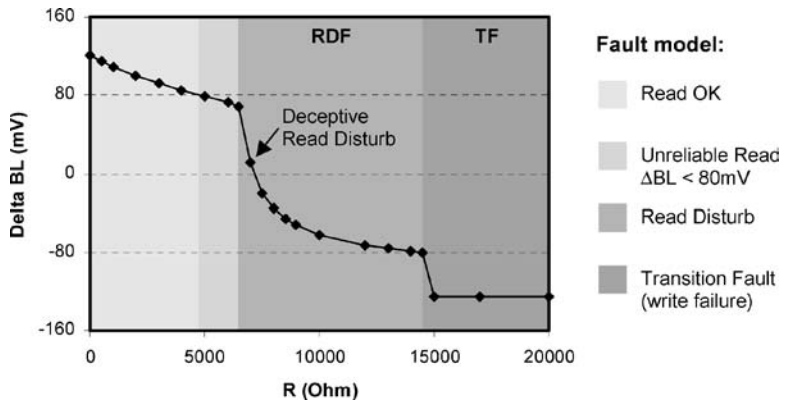

Fig. 3. Variation of ΔBL during read as a function of injected resistance value (Df3).

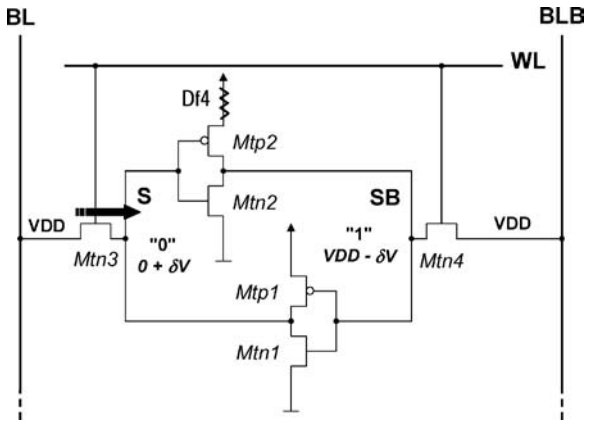

Fig. 4. Effect of Df4 during a read '0' operation.

When in the faulty cell is stored '1' and a '0' is written just before a read operation, the cell loses its content more easily. Actually, after the w0 operation, SB does not have enough time to reach VDD and it begins to discharge when it is not at an actual '1' logic. If the defect is sensitized by a write operation followed by a read access, the corresponding fault model is a *dynamic Read Destructive Fault*. If the cell flips after several reads, it is a *dynamic Multiple-Read Destructive Fault*. Before the destruction of the cell content, the SB level is slightly degraded after each read (see Figs. 5 and 6).

Thus, depending on the resistance value, the fault is detected by a different sequence. In Fig. 5, a 10 MΩ resistance is sensitized by a Write-Read sequence, while a 3 MΩ resistance needs a Write-Read-Read operation series. A resistance value if 1 MΩ is never detected at this clock frequency.

Therefore the detection of this defect can be improved by a series of read operations performed at high speed. The simulation waveforms in the typical process corner, at 125°C temperature and 1.6 V supply are shown in Fig. 6. Here a 1.5 MΩ resistive defect produces a read disturb fault after the fifth consecutive read access performed *at-speed* (cycle time = 3 ns). The sensitization sequence for this fault is $1w0(r0)^5$, i.e. a w0 followed by five r0. This fault can thus be regarded as a *dynamic Multiple Read Destructive Fault*, and it is an extension of the *dynamic Read Destructive Fault* already reported for e-DRAMs [4]. Note that the memory data output is still correct during the fifth read, so that an additional read operation is necessary to observe the fault (*deceptive Multiple Read Destructive Fault*).

In general, the dependence of dRDF has been studied in relation to the cycle time and the defect size. The results are presented in the graph of Fig. 7 where each point corresponds to a determined couple (cycle time, defect size) and is placed in a certain area corresponding to a sensitization sequence like $1w0(r0)^N$, where $N = 1$ to 5.

The graph in Fig. 7 clearly shows that the minimum detected resistance value largely depends on the length of the clock cycle. The range for the resistance value is about between some hundreds Ω up to 10 MΩ, so

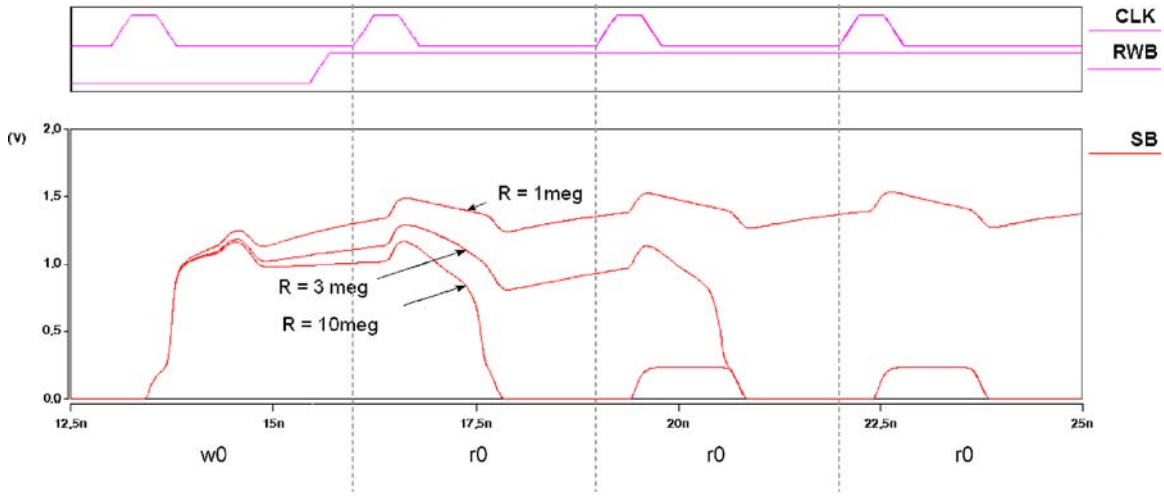

Fig. 5. A destructive read occurring after consecutives "at-speed" read access (typ proc, $T = 125°C$, $V = 1.6$ V, $T_{cyc} = 3$ ns).

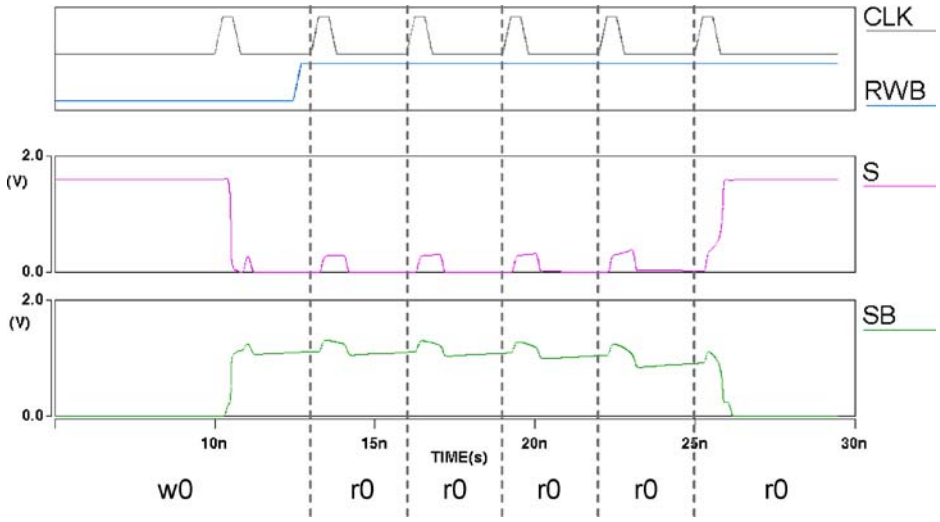

Fig. 6. A destructive read occurring after the 5th consecutive "at-speed" read access (typ proc, $T = 125°C$, $V = 1.6$ V, $T_{cyc} = 3$ ns, $R = 1.5$ MΩ).

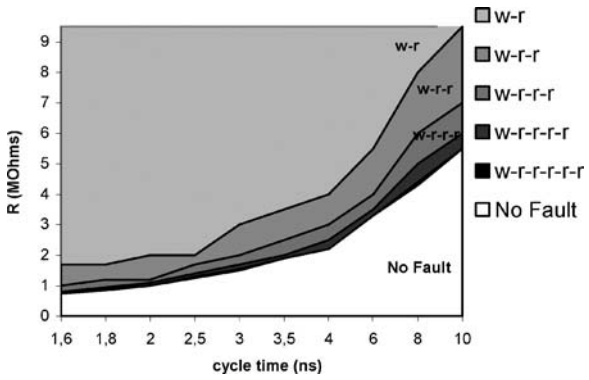

Fig. 7. Defect detection as a function of cycle-time for different sensitization sequences (typ proc, $T = 125°C$, $V = 1.6$ V).

one order of magnitude occurs in the processed window for the resistance variation. Besides, even at the highest simulated speed (i.e. 1.6 ns, which is the minimum clock cycle for the memory under study), it can be observed that the fault detection can still be improved by a factor of ∼2X by applying a series of 4–5 consecutive reads. It is also interesting to note that this fault can equivalently be represented as a degradation of the memory minimum cycle time.

Finally, the "dynamic" nature of the fault is confirmed by the fact that a fully static read test (i.e. a 0r0 sensitization sequence) is able to detect only faults produced by high resistance values, larger than 140 MΩ.

3.2. Address Decoder Simulations

The outcome of a simulation of a 50 kΩ resistive defect injected in the pull-down path of one of the NOR gates of the word line pre-decoder is shown in Fig. 8. During the first cycle, WL0 is addressed and the corresponding NOR-gate output (ZA0 in the graph and in the scheme of Fig. 2) is '1' logic. This first access produces a w1 at WL0. During the second cycle, WL1 is accessed (ZA1 is activated, '1' logic), but, due to the presence of the defect, ZA0 remains still high. Consequently both WL0 and WL1 are selected and the '1', that is written in the cell addressed by WL1, overwrites the '0' that was previously stocked at WL0. Hence the final access at WL0 will read a '1' instead of the expected '0'.

In presence of stuck-open faults in the address decoder (a.k.a. SOAFs or ADOFs) are always detected by applying a proper address switching sequence, the detection of resistive-opens depends on the resistance value and the access speed. In particular the presence of a resistive-open is equivalent to a degradation of the address setup time for a particular address sequence. This effect is confirmed by the graph of Fig. 9, where the detected resistance value is given as a function of the address setup time. Interestingly enough, the fault detection does not depend on the clock cycle time since the fault is sensitized in the memory cycle immediately following the address change. However, if the addresses are generated by registers, which are clocked on a certain clock edge, an increase in the clock speed

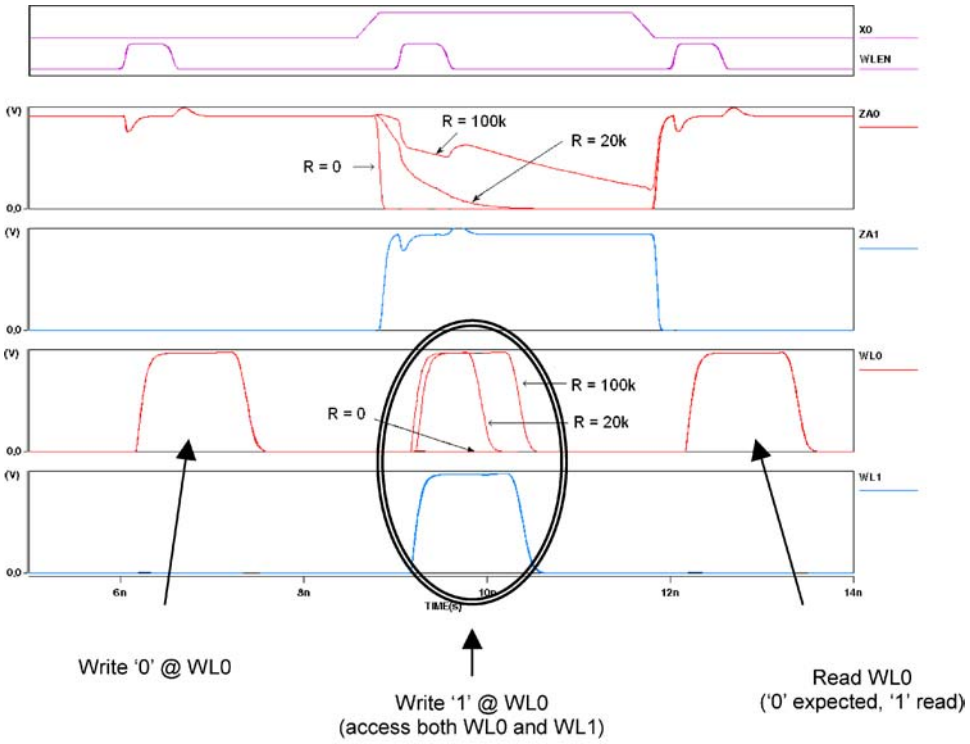

Fig. 8. A resistive-open fault in the X address decoder sensitized by a Sachdev-like sequence ($T_{cyc} = 3$ ns, $T_{Asetup} = 0.3$ ns, $R_{defect} = 50\,k\Omega$).

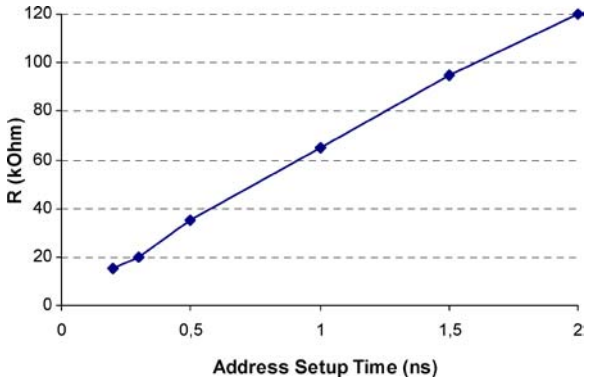

Fig. 9. Minimum detected resistance vs. address setup time (typ proc, $T = 27°C$, $V = 1.5$ V).

would also decrease the address setup time, thus improving the fault detection.

4. Implications for Memory Test

The results obtained during the simulations performed for this study have shown the importance of resistive-open defects in SRAM memories. In particular, among the numerous fault models related to the injected defects it is interesting to put the attention on those that involve a dynamic behavior because of their hardness of detection. In the following sub-sections we introduce some elements of our consequent works on this subject and the efficient test solutions developed for ADOFs and dRDF detection.

4.1. Address Decoder Open Fault

Several test solutions can be used for ADOFs and resistive-ADOFs detection but March tests remain the most attractive solution due to their linear complexity and effectiveness for detection of a large number of other faults. However, March tests are constructed essentially for the detection of static faults such as stuck-at and transition faults. ADOFs and resistive-ADOFs are not targeted by such test algorithms due to their dynamic nature and thus require either new algorithms or some modifications in existing algorithms.

As mentioned in Section 2, ADOF detection requires a specific address sequence in order to sensitize all the faults. This is done by using an address sequence

including all the pattern pairs with an Hamming distance of 1. The Sachdev-like sequence includes this property. The basic idea proposed in [7] consists in developing new March elements having the same properties than the operations (read and write) used in the Sachdev-like sequence as well as the specific address sequence. These new March elements are able to detect all ADOFs and resistive-ADOFs without sensitization and observation problems.

An extension of this study was presented in [6] where we propose to embed in the March C- the properties of these new March elements. The reformulation of the March C-, called March iC-, is essentially based on introducing a particular address sequence and a particular read/write data sequence making it able to detect ADOFs and resistive-ADOFs. We also show that these modifications do not change the complexity and, in particular, the ability of March C- to detect the faults initially covered by this algorithm (SAFs, TFs, coupling faults, AFs).

4.2. Dynamic Faults in the Core-Cell

Among the known dynamic faults that may affect SRAM memories, we also concentrate on those that concern the core-cell. One of these faults is the dynamic Read Destructive Fault (dRDF). It has the following behavior: a write operation immediately followed by a read operation causes the flip of the logic value stored in the cell. A possible defect that may involve a dRDF is the defect 4 in Fig. 1.

Recently, a test solution, referred as March RAW (Read After Write) [13], has been proposed to detect all single-cell dynamic faults in core-cells. Its complexity is 13N including the initialization. This algorithm detects dRDFs by March elements that perform a write operation followed by a read operation, e.g. 1w0r0. As shown before (Section 3.1) this test can be improved by applying $1w0r0^M$ sequences where $r0^M$ denotes a sequence of M successive r0 operations, e.g. $1w0r0^4$ = 1w0r0r0r0r0. In this case, the multiple read operations after the w0 allow a more efficient fault detection. However, if a large number of read operations is needed to sensitize the fault, the test complexity increases dramatically.

In [8] we have proposed a more efficient alternative to March RAW. For this purpose, we have improved the standard March C- algorithm (10N) in order to make it able to detect also dynamic faults in the core-cell. Our modified March C- detects dRDFs by using a particular address sequence. This modification is allowed by the first of the six Degrees of Freedom (DOF) [17] of March tests, and does not change the capability of March C- to detect the former target faults.

The multiple read operations can be achieved by our modified March C- by an indirect way. During a read or write operation the pre-charge circuit is turned off in the selected column; the others columns have the pre-charge left on. Consequently, all the cells on the same word line of the selected cell fight against the pre-charge circuit. In [8] we have shown that this event, that we called "Read Equivalent Stress" (RES), can be used to sensitize dRDF as actual read operations. The occurrence of a maximal number and distribution of RESs for all the cells is warranted by a simple address ordering, word line after word line.

5. Conclusions

The present study has been focused on the extraction of defect-based fault models. The primary targets have been the study of the consequences of resistive-open defect injection because this kind of defects seems to be responsible of most of delay faults and "hard-to-detect" faults in memories. Among all the identified fault models we have focused the attention on those that have a dynamic behavior. In particular a detailed analysis has been done for ADOFs and dRDF, respectively in the address decoder and in the core cell.

In order to operate a correct characterization we have identified specific test sequences for ADOFs and dRDF sensitizations. All the simulations have been performed for different values of temperature, supply voltage and process corner. Moreover, we have considered the variations of other parameters as the value of the resistance of the injected resistive-open defects and the clock cycle of the circuit. This way we have identified those conditions that maximize the fault sensitization.

The here presented investigations have been the bases for our further studies in which we have proposed efficient algorithmic solutions for the considered dynamic faults.

Acknowledgments

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A SPICE-Like 2T-FLOTOX Core-Cell Model for Defect Injection and Faulty Behavior Prediction in eFlash

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Abstract The embedded Flash technology can be subject to complex defects creating functional faults. In this paper, we describe the different steps in the electrical modeling of 2T-FLOTOX core-cells for a good understanding of failure mechanisms. At first, we present a first order electrical model of 2T-FLOTOX core-cells which is characterized and compared with silicon data measurements based on the ATMEL 0.15 µm eFlash technology. Next, we propose a study of resistive defect injections in eFlash memories to show the interest of the proposed simulation model. At the end of the paper, a table summarizes the functional fault models for different resistive defect configurations and experimental set-ups. According to these first results and with additional analysis on actual defects presented in [3] we are then able to enhance existing test solutions for eFlash testing.

Keywords Embedded Flash · 2T-FLOTOX core-cell · Electrical model · Resistive defects · Fault modeling

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1 Introduction

Memory density will continue to grow over the next years according to Moore's Law. This is confirmed by the SIA Roadmap which forecasts a memory density approaching 94% of System-on-Chip (SoC) silicon area in the next ten years [16]. Moreover, memory will continue to be used as a process development vehicle for new digital technologies. Therefore, memories are becoming the main contributor of the overall SoC yield loss. Consequently, efficient test solutions and repair schemes for memories are needed.

Different types of memory can be embedded in a SoC as SRAM, DRAM, EEPROM and Flash. The increased use of portable electronic devices such as mobile phones and digital camera produces a high demand for Flash memories. Flash memory is a non-volatile memory that allows programming and erasing memory data electronically [1, 12]. The main-stream operation is based on the floating-gate concept on which charges can be stored and removed. Its low-power consumption and high integration density make it popular for portable devices.

However, the high integration density of eFlash memories and their particular manufacturing process steps make them more and more prone to inter or intra core-cell defects. Moreover, the non-volatile nature of eFlash requires a high electric field to inject charges in the floating-gate during the programming mode. In some cases, the presence of such high electric field may disturb the core-cell state [6, 10].

In this domain, only few papers can be found in the literature. Generally, all reported studies deal with 1T Flash core-cells (stacked gate/ETOX) [5, 10, 11] or 11/2T Flash core-cells (split gate/local SONOS) [5, 10, 11]. In [3], we have considered the standard 2T-FLOTOX core-cell structure which is often used to build embedded Flash memories. We have performed a qualitative analysis of actual defects that may occur in the core-cell and in the memory array. These defects are opens and bridges (pure or resistive), capacitive coupling but also defects linked to the sense transistor such as bad tunnel window. All these defects have been reported from silicon measurements on the ATMEL 0.15 µm eFlash technology.

From this set of defects, we have to perform electrical simulations in order to analyze the possible resulting faulty behaviors of the 2T-FLOTOX core-cell. These electrical simulations have to reflect the read, write and erase operations. The read operation consists of current sensing. During this operation, the sense amplifier measures the current through the core-cell. Depending on the core-cell state, the sense amplifier gives a logic '0' or '1' on its output. Such a simulation can be easily done with a SPICE-like description with appropriate Vt according to the core-cell state and appropriate voltage levels on the different nodes of the memory array. On the other hand, the faulty behavior of the memory has also to be evaluated during erase and write operations. These two operations change the core-cell state (from a logic '0' to a logic '1' and vice-versa), *i.e.* charges are injected or removed to the floating gate device. In this case, the memory behavior is much more difficult to simulate as many physical phenomena have to be considered such as the Fowler-Nordheim tunneling effect.

In this paper, we propose a SPICE-like electrical simulation model of the 2T-FLOTOX core-cell that allows write and erase operations in addition to read operations. This model is a first order model of the 2T-FLOTOX core-cell. Comparisons with silicon data show the accuracy of the proposed model. In the last section of the paper, this new model is used to analyze the functional behavior of possible defects that may occur in an eFlash memory. Further possible uses of this model are eFlash characterization and process optimization.

The rest of the paper is organized as follows. Section 2 describes the eFlash and gives the basic operations of a 2T-FLOTOX core-cell. Section 3 details the electrical simulation model of the 2T-FLOTOX core-cell. Section 4 presents a resistive defect injection in an eFlash array designed with the proposed simulation model. Finally, Section 5 concludes the paper.

2 eFlash Description

The functional scheme of an eFlash memory is presented in Fig. 1. As all other memories the eFlash is composed of a core-cell array (CORE), data latches (DLATCH), bit-line and word-line decoders and sense amplifiers. In addition, eFlash memories need two particular building blocks to perform dedicated functions: a charge pump device for the High Voltage Generation (HVG) allowing the write and erase operations and a Sense Reference Voltage used during the read operation.

Two types of core-cell array can be used to design an eFlash memory; NOR and NAND-based structures [12, 14]. Here, we present only the NOR-based structure which is the most often used in high-speed applications. In a NOR-based eFlash, core-cells are placed in parallel as shown in Fig. 2. A word-line (WL_i) is shared by all core-cells in the row. All core-cells of one row are addressed together to form a page.

The eFlash core-cell is based on the floating-gate (FG) concept. There are two typical mechanisms to transfer electric charges from and into the FG: hot carrier injection (HCI) [12, 14] and the Fowler-Nordheim (FN) tunneling effect [12, 14]. The FN tunneling effect is used for charge

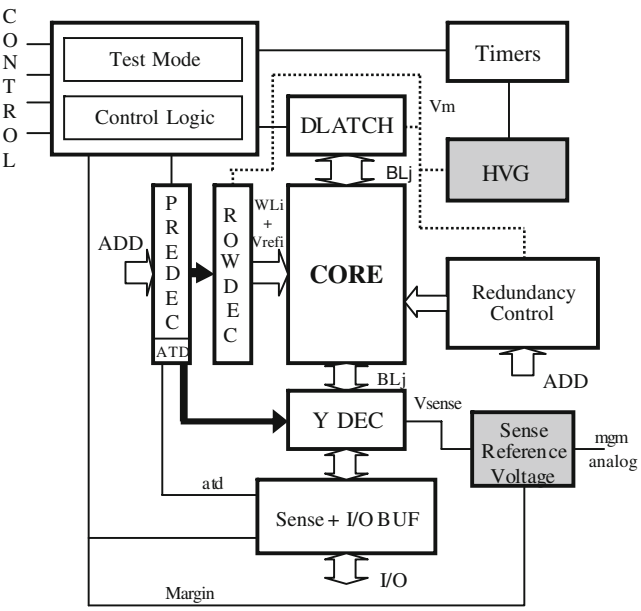

Fig. 1 Functional scheme of eFlash memories

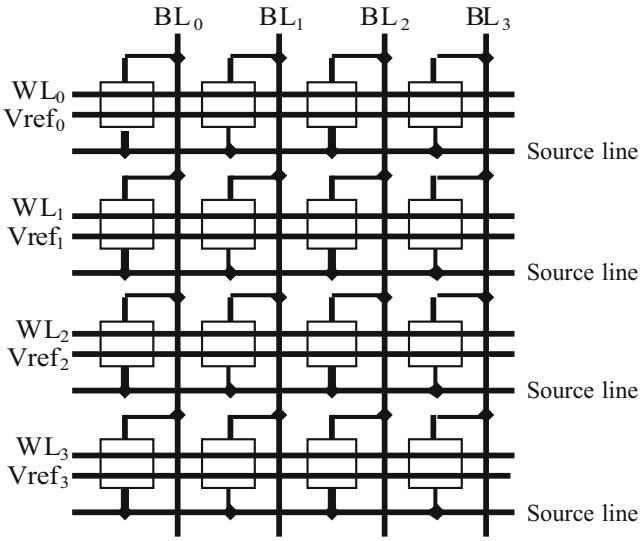

Fig. 2 NOR eFlash structure

injection or removal in 2T-FLOTOX core-cells. For this study, we use the 2T-FLOTOX core-cell structure presented in Fig. 3 [7, 12, 14]. The memory core-cell is composed of a select transistor and a sense transistor. The select transistor allows the selection of the targeted core-cell. It also avoids disturbances from the high voltage on the bit-line when the core-cell is not selected. The sense transistor contains the floating-gate (FG) and the sense gate.

Three different operations can be performed on an eFlash: Erase, Write and Read. In the following, we consider cell(*i*,*j*) as the target core-cell. The different voltage levels required for the erase, write and read operations are reported in Table 1. The Erase operation consists in injecting charges in the FG with a specific high voltage combination. To inject charges in the FG, the high voltage must be applied on the Vref node of the sense transistor while its drain must be maintained at ground. During the Erase operation, the core-cell is 'on' and allows the node BL_j to be pulled-down at the Vss potential. At this point, it is important to notice that the erase operation is performed simultaneously on all core-cells of the same page and not core-cell by core-cell. At the end of the erase

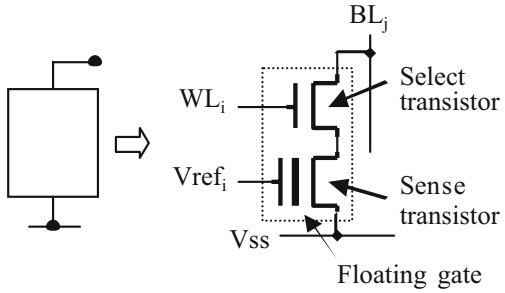

Fig. 3 2T-FLOTOX core-cell

Table 1 Voltage levels for erase, write and read operations

	Erase	Write	Read
BLj	0 v	Vpp	1 v
BLx	0 v	HZ	1 v
WLi	15 v	15 v	3.3 v
WLy	0 v	0 v	0 v
Vss	0 v	1.2 v	0 v
Vrefi	Vpp	0 v	0.7 v
Vrefy	HZ	HZ	HZ

with $x \neq j$ and $y \neq I$, Vpp≈12.5 v

operation, charges in the FG have changed the Vt of the sense transistor to a high Vt (VTH in Fig. 4). From a functional point of view VTH corresponds to logic '1'.

The Write operation consists in removing charges from the FG by putting the Vref node at ground while maintaining BLj at a high voltage (see Table 1). With this operation, charges of the FG are removed and so the sense transistor has a low Vt (VTL in Fig. 4) which corresponds to logic '0'. We call Vt window (VTW) the difference between VTH and VTL.

As for all other kinds of memory, the read operation is performed by a sense amplifier but working in a current measurement mode. The Vref node is set around 0.7 v during the read operation (see Table 1). If the sense transistor has a low Vt (VTL), it delivers a current (between 10 µA to 30 µA) and the sense amplifier provides a logic '0' on its output. On the other hand, with the same Vref value, if the sense transistor has a high Vt (VTH) there is no current through the bit-line and the sense amplifier gives a logic '1'.

3 SPICE-like 2T-FLOTOX Core-Cell Model

In our previous work [3], a qualitative analysis has been proposed on actual defects that may occur in an eFlash memory array built with 2T-FLOTOX core cells. The faulty behaviors associated to this study have been easily modeled without the use of electrical simulations.

Conversely, electrical evaluations have to be performed in order to validate the possible faulty behaviors of the eFlash in presence of complex defects such as resistive shorts. Electrical simulation models are needed to perform such evaluations during the read operation but also during the write and erase operations. The read operation is easy to simulate as it consists in a current measurement through the core-cell. This operation can be simulated with a SPICE-like description including different Vt values (VTL and VTH) of the floating gate transistor and appropriate voltage levels on core-cell nodes. On the other hand, erase and write operations have to be performed in presence of

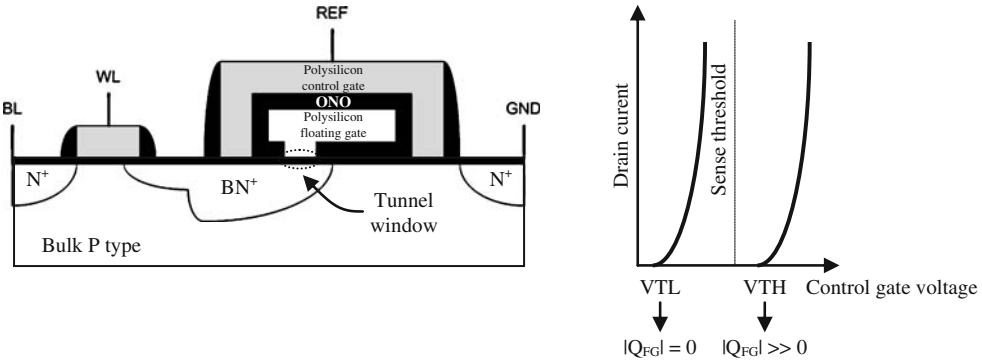

Fig. 4 Vt modulation with charge quantity

defects. In this case, the electrical simulation model has to take into account the Fowler-Nordheim tunneling effect which is more difficult to represent.

In [10, 11], a SPICE electrical model based on 1T Flash core-cell is presented to evaluate the program disturb fault in Flash memories. This model implements the two possible mechanisms (Channel Hot Electron Injection and Fowler-Nordheim tunneling effect) to write and erase a FG-transistor. In [8, 15], the authors proposed a SPICE electrical model based on 2T-FLOTOX core-cell. However, all these models are limited to a static description of write and erase operations represented by a fixed current and voltage sources. Therefore, with such models, it is impossible to simulate successive operations (write and/or erase) performed on a core-cell. Another study has proposed a dynamic solution to simulate the 2T-FLOTOX core-cell behavior based on a MOS Model 9 [13]. This model achieves good performances but requires complex set-up parameters. In this section, the development of a SPICE-like 2T-FLOTOX core-cell model writable and erasable by Fowler-Nordheim tunneling effect is proposed. Our proposed simulation model will have a dynamic and autonomous electrical behavior depending on voltages applied on its nodes. In the following, the proposed electrical model is described and then, comparisons with silicon data to validate this model are provided.

3.1 Description of the Simulation Model

To develop such a model, we consider the 2T-FLOTOX core-cell presented in Fig. 3. From that scheme, the development of the model consists in representing the select transistor and the sense transistor.

The *Select transistor* is modeled by a particular device available in the 0.15 µm ATMEL technology with high voltage properties. This particular transistor is called *NWMV*.

Concerning the *Sense transistor*, the description is more complex due to particular coupling effects and to the Fowler-Nordheim tunneling effect phenomenon.

To model the coupling effects, we consider the double-gate device presented in the cross-section of Fig. 4. One gate is the floating gate and the other gate is connected to the Vref node. Due to the ONO (Oxide Nitride Oxide) dielectric between the two gates, a part of the voltage applied on the Vref node also occurs on the floating gate. We call this phenomenon the *gate coupling effect*. This effect is characterized by the ratio of the ONO capacitance over the total capacitance of the sense transistor. This ratio is referred to here as *Ag*. To have a good understanding of this coupling effect, the Fig. 5 represents the different capacitances of the sense transistor. The different nodes of the sense transistor are also represented, *i.e.* the control gate (Vrefi), the floating gate, the drain, the bulk and the source nodes.

Due to the gate coupling effect, the high voltage applied to the control gate during the erase operation is important enough to create a high electric-field between the floating gate and the drain node. In presence of this electric-field, the Fowler-Nordheim tunneling effect can occur. The other capacitances (C_S and C_B) do not contribute significantly to the floating gate voltage due to their low values. The drain coupling effect (C_D) is due to the oxide tunnel window drawn above the drain diffusion where the oxide thickness is very small (see Fig. 4). It is referred to here as *Ad*.

We have seen the importance of capacitive effects in order to model the sense transistor. Now, we describe the charges injection or removing mechanisms in the floating gate. Remember that the erase or write operations of a 2T-

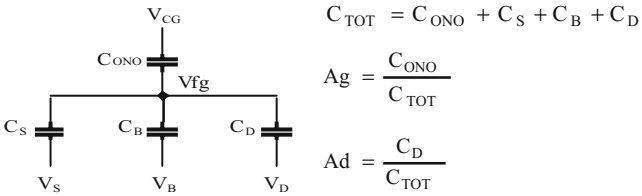

Fig. 5 Coupling effects in the sense transistor

FLOTOX core-cell use the Fowler-Nordheim tunneling effect to modulate the charge quantity in the floating gate and thus the threshold voltage value of the sense transistor. We can easily represent the floating gate by a capacitive charge quantity varying with the Fowler-Nordheim tunneling effect. Following the law $Q = C * U$ (which is the law defining the electrical charge quantity 'Q' contained in a capacitor 'C' under a potential 'U'), the voltage of this capacitance is proportional to the charges injected or removed. From a physical point of view, the equivalent capacitance value (C_{TOT}) represents the total capacitance of the sense transistor.

We have seen in the previous section that the charge quantity stored in the floating gate impacts the Vt value of the sense transistor. When the core-cell is erased, we have a high Vt (VTH) and when the core-cell is written, we have a low Vt (VTL). Thus, to build the model, we need a transistor whose Vt value changes according to the quantity of charges stored in C_{TOT}. This principle can be easily implemented in an electrical SPICE-like model.

Now, we describe the physical phenomenon of Fowler-Nordheim charge transfer in the floating gate. The Fowler-Nordheim tunneling effect is represented by the following equation [9]:

$$I_{FN} = A \times \alpha \times E_{ox}^2 \times \exp\left(\frac{-\beta}{E_{ox}}\right) \quad (1)$$

with:

A Tunnel window area
α Fowler Nordheim constant
β Fowler Nordheim constant
E_{ox} Oxide electric field

The tunneling effect is equivalent to a current source controlled by an electric-field (E_{ox}). This electric-field is due to the voltage between the drain diffusion and the floating gate at the tunnel window interface. In a SPICE-like simulator, we can describe such current source if we know all the parameters of Eq. 1. From the ATMEL silicon measurements on the 0.15 µm technology, we have extracted all these parameters; A, α, β and the oxide thickness of the tunnel window used to calculate E_{ox}.

With all these elements a first order SPICE-like model has been implemented and its block scheme is presented in Fig. 6.

For the select transistor, we use a NWMV transistor. The blocks *Ag* and *Ad* represent the coupling factors due to the different capacitances. The capacitance C_{TOT} is used to store the charges provided by the block *FN* representing the Fowler-Nordheim tunneling effect. This block is implemented as a current source in SPICE. We sum these three effects (block *Sum*) to control the gate of a high voltage transistor NWMV representing the sense

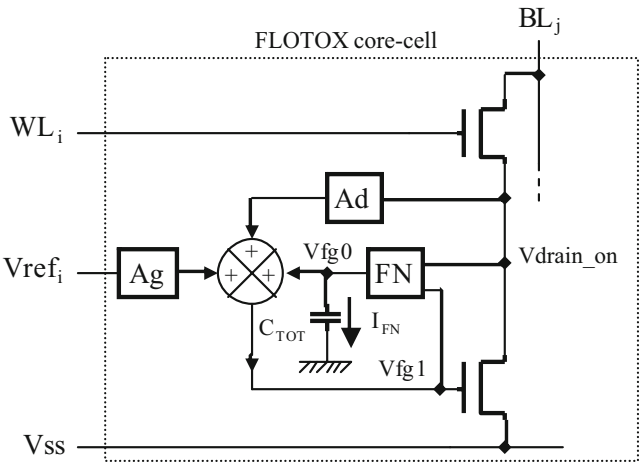

Fig. 6 2T-FLOTOX electrical simulation model

transistor. The voltage *Vfg1* represents the equivalent floating gate voltage of a 2T-FLOTOX core-cell under Fowler-Nordheim and coupling effects. As seen previously, the Vt value of an erased or written core-cell depends on the charge quantity stored in its floating-gate. This charge quantity is represented by the Vfg1 potential in the proposed model. During an erase operation, as charges are injected to the floating-gate, Vfg1 becomes negative. Conversely, the Vfg1 potential becomes positive during a write operation as charges are removed from the floating-gate. From a read operation point of view, when Vfg1 is negative, we need a high voltage on $Vref_i$ to create a population inversion in the NWMV device and thus a current through the bit-line. The resulting Vt value is high (VTH) that corresponds to an erased core-cell. When Vfg1 is positive, even a small voltage on $Vref_i$ node allows the NWMV device conduction, thus corresponding to a low Vt (VTL). The core-cell is written. Note that the model is represented as a linear feedback system because the electric field depends not only on the drain voltage but also on the floating gate voltage which varies with the C_{TOT} charge quantity.

3.2 Experimental Validation of the Model

To validate our proposed 2T-FLOTOX core-cell model, we have done simulations for erase, write and read operations. These results are presented in Fig. 7. In this figure, the five waveforms represent WL_i, $Vref_i$, BL_j, Vfg1 and the current through the bit line (I_{BLj}) respectively.

The first 2 ms of the simulation corresponds to an erase operation. This operation consists in applying a high voltage to WL_i (≈14 v) and $Vref_i$ (≈12.5 v) nodes, and in assigning Vss and BL_j nodes at ground. At the beginning of the erase operation, due to the coupling effects (Ag and Ad), the floating gate voltage (Vfg1)

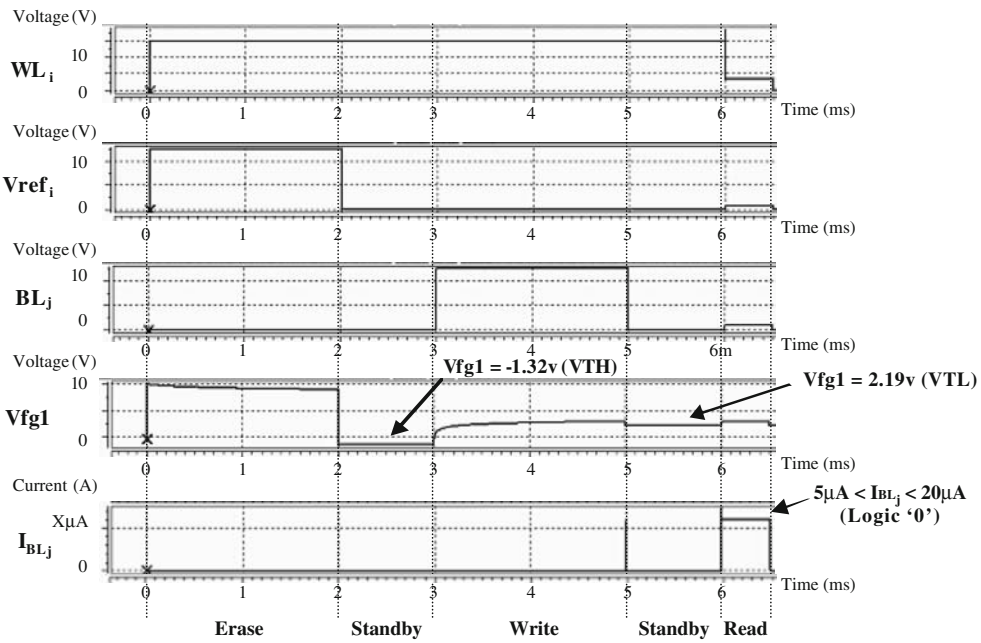

Fig. 7 Electrical simulations of Erase, Write and Read operations

follows the $Vref_i$ node ($Vfg1 \approx Ag * Vref_i$). Afterwards, the Fowler-Nordheim tunneling effect begins and induces a charge injection in the floating gate. In the model, charges are stored in C_{TOT} that leads to a negative voltage level at Vfg0 node. Thus, the resulting level of Vfg1 decreases until the end of the erase operation. The erase operation is followed by a standby phase of 1 ms duration. During this phase, we measure the Vfg1 level, about −1.32 v, which is an image of the Vt value (VTH) of an erased 2T-FLOTOX core-cell.

In the next phase (from 3 ms to 5 ms) which is a write operation, nodes WL_i and BL_j are set to a high voltage (≈14 v and ≈12.5 v respectively) while nodes Vss and $Vref_i$ are set to ground. At the beginning of this write operation, the coupling effects (Ag and Ad) and the voltage levels on the core-cell nodes make the floating gate level close to its previous level. Then, the Fowler-Nordheim tunneling effect starts to remove charges stored in the floating gate. According to the model, charges are removed from C_{TOT}. The Vfg1 level increases as a capacitance loading. The following phase, as previously, is a standby phase. The Vfg1 level measured in this phase is about 2.19 v which is an image of the VTL of a written 2T-FLOTOX core-cell.

Finally, the last operation (from 6 ms to 6.5 ms) corresponds to a read operation. The different nodes of the core-cell are set as follows: ≈3.3 v for WL_i, ≈1 v for BL_j, ≈0.7 v for $Vref_i$ and ground for Vss. As the core-cell has been written (VTL), it contains a logic '0'. In this case, during the read operation the sense amplifier measures a current through the bit line. We also simulate an erase operation followed by a read (not represented on the figure). This time, the core-cell is erased (VTH which represents a logic '1'). The simulation has confirmed that no current passes through the bit line.

After these basic simulations of the 2T-FLOTOX core-cell model, we now present some comparisons with silicon data obtained on the 0.15 μm ATMEL technology. We analyze the VTH and VTL values after the erase and write operations for different programming times and voltage levels. Table 2 gives a representative set of these comparisons between ATMEL Silicon data and the proposed model. In this table, the two first columns give the programming time (Tp) and voltage conditions (Vpp). The following columns present the Vt window (VTW=VTH−VTL) obtained after an erase and a write operation for both our model (SPICE-like Model) and ATMEL measurements (Silicon Data). The last column of the table gives the difference between the model and silicon data. VTH and VTL values obtained with the model and measured on an ATMEL eFlash are not reported on this table for confidentiality reasons.

These comparisons show that for a Vpp value close to the nominal condition (12.5 v), the SPICE-like model and silicon data are always quite similar (2% or less) irrespective of the considered programming time (from 1 ms to 5 ms). To comment these results, it is important to notice that the establishment of the model has required the extraction of the Fowler-Nordheim constants from silicon data measurements. These constants have been calculated from erase and write operations in nominal conditions; a programming time of 2 ms and a high voltage Vpp of 12.5 v. So, the matching between the model and silicon data was quite predictable for a nominal value of Vpp. Even if this proposed model is a first order model, the resulting

Table 2 Characterization of 2T-FLOTOX model

Timing and voltage conditions		Threshold voltage Vt (v)		$\frac{VTWm-VTWd}{VTWd}$ (%)
		SPICE-like model	*Silicon data*	
Tp	Vpp	VTWm	VTWd	
1 ms	12.5 v	3.67	3.64	0.82
1 ms	12 v	2.69	2.77	−2.89
1 ms	11.5 v	1.84	1.90	−3.16
1 ms	11 v	1.15	1.04	10.58
2 ms	12.5 v	4.28	4.19	2.15
2 ms	12 v	3.26	3.32	−1.81
2 ms	11.5 v	2.32	2.45	−5.31
2 ms	11 v	1.52	1.58	−3.8
5 ms	12.5 v	4.98	4.88	2.05
5 ms	12 v	3.93	4.00	−1.75
5 ms	11.5 v	2.93	3.13	−6.39
5 ms	11 v	2.04	2.26	−9.73

simulation represent, with good accuracy, the electrical behavior of 2T-FLOTOX core-cell.

3.3 Further Improvements of the Model

The objective of our model was reached for nominal conditions as there is a good matching with silicon data measurements. However, we can extend our characterization study of the proposed model to other conditions. These conditions could be those of new Flash memory utilization or those induced by the presence of a particular defect. Consequently we have performed additional simulations with a Vpp not in nominal conditions (see Table 2). For these extremes conditions, the decrease of the Vpp voltage involves a bad matching of the proposed model with silicon measurements. This is true especially when we measure VTH and VTL (not reported here for confidentiality reasons) obtained with the model and silicon data. As for the nominal conditions characterization, these results were predictable. In fact, we have performed the Fowler-Nordheim constants calculation in nominal conditions and silicon measurements show that their values can depend on the electrical conditions applied on the 2T-FLOTOX core-cell. For example, the β parameter of Eq. 1, which depends on the SiO_2 energy barrier at the tunnel window interface, varies with the initial electric-field E_{OX} intensity and so, with the Vpp value. These discrepancies of the model do not appear when we only consider the Vt window (VTWm and VTWd) as presented in the last column of Table 2 where we obtain a maximum error of 10.6%. We can explain this phenomenon by an offset problem for which the value is correlated to the extremes Vpp and Tp conditions.

Our future work will therefore focus on the setting up of a new model matching more precisely the silicon measurements irrespective of the experimental conditions. Due to the high voltage, the 2T-FLOTOX environment is aggressive and thus requires the use of particular devices (NWMV) to design the model. We will propose a future model where these NWMV devices will be characterized for a larger range of operations. However, it is important to emphasize that the model proposed in this paper is pertinent enough to describe the electrical behavior of a 2T-FLOTOX core-cell under defect injection or for failure analysis.

4 Resistive Defect Injection in a 2t-Flotox Core-Cell Array

In [3] the qualitative analysis of possible defects occurring in the 2T-FLOTOX core-cell and in the eFlash array has been performed. All these resistive defects have been reported from a 0.15 µm eFlash technology.

From this first analysis, we have seen that resistive defects in the core-cell array involve complex behaviors during erase, write and read operations. Now, with the help of the proposed 2T-FLOTOX model, resistive defects have been injected and their corresponding behaviors have been analyzed. The objective in this section is to demonstrate the interest of our electrical model for defect analysis and faulty behavior prediction useful to give comprehensive fault models. In fact, the proposed model is used to simulate the erase, write and read operation in presence of defects. These simulations allow the evaluation of electrical levels on important nodes of the core-cell. These levels allow predicting the resulting faulty behavior of the core-cell and the range of defects that involves this faulty behavior.

In the following, we first present the resistive defect injection and the simulation environment used. Then, each defect with electrical data has been analyzed in detail and a functional fault model is proposed for each faulty behavior.

4.1 Resistive Defect Injection in the Eflash Array

From a layout point of view, resistive defects may occur on the same layer (poly/poly, *i.e.* resistive defect between WL and Vref) or between two layers (metal/poly, *i.e.* resistive defect between WL and BL). Note that, resistive defects between Vref and BL are not possible. This resistive defect analysis is performed on the 3*3 NOR-based eFlash memory array presented in Fig. 8.

In order to analyze the eFlash behavior in presence of resistive defects, we have injected defects as follows (see Fig. 8):

- **Df1:** resistive short between WL_i and BL_j. This defect concerns cell(*i*,*j*).
- **Df2:**resistive short between WL_i and BL_{j+1}. This defect concerns cell(*i*,*j*+1) sharing the same word-line as cell(*i*,*j*) but not on the same bit-line.
- **Df3:** resistive short between WL_{i-1} and BL_j. This defect concerns a cell(*i*−1,*j*) sharing the same bit-line as cell(*i*,*j*) but not on the same word-line.
- **Df4:** resistive short between WLi and Vrefi. This defect concerns all core-cells sharing the same word line and the same control line.
- **Df5:** resistive short between WLi and WLi+1. As for Df4, this defect concerns all core-cells sharing the same word line.

On the basis of [3], we have sensitized the different weakness points that have to be investigated more precisely.

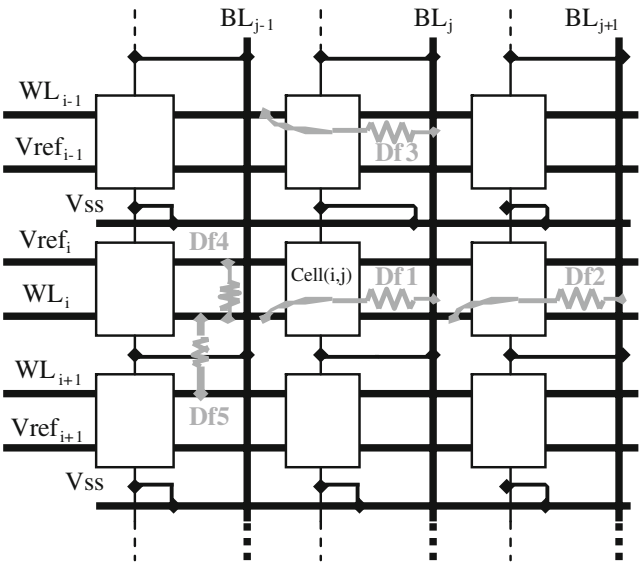

Fig. 8 Resistive short defects in a 3*3 NOR-based eFlash memory

In the following subsection, we present a complete electrical analysis of these defects. All these simulations have been allowed by the proposed model because, as mentioned in Section 3, it is able to reproduce the 2T-FLOTOX behavior during erase, write and read operations. Compared to our previous work in this domain [3], now we are able to give electrical levels of the core-cell nodes and thus, provide a quantitative analysis of defect injection. With all these electrical values, we can easily define the limit of a faulty or fault-free 2T-FLOTOX core-cell in presence of a defect and provide a complete functional fault modeling to enhance existing eFlash test methods.

4.2 Simulation Environment

First, a simulation environment is configured close to the silicon reality. A 3*3 eFlash core-cell array based on our 2T-FLOTOX core-cell model is described. Moreover, in this description two blocks are added; a logic decoder and a high voltage generator. The logic decoder drives the high voltage on the WLi, Vrefi and BLj nodes according to the operation performed on the selected core-cell. Details on this circuit are not given here as it is composed of standard decoder circuits using pass-gates with high voltage properties.

In eFlash memories, a charge pump based on the Dickson principle [2] is embedded for high voltage generation. In order to simplify the simulation environment, the equivalent scheme of the charge pump (Fig. 9) is used.

A charge pump allows providing a high voltage level from a standard low voltage supply by a capacitive energy transfer [2]. There is a linear relation between the size of the charge pump (*N*), the low voltage supply (Vdd) and its output voltage (*V*out):

$$V_{\text{out}} = (N+1) \times \text{Vdd} \tag{2}$$

In this relation we can add a statement introducing that the charge pump device has a drop voltage when its load becomes too important:

$$V_{\text{out}}* = (N+1) \times \text{Vdd} - \left(I_{\text{load}} \times R_{\text{eq}}\right) \tag{3}$$

Note that the equivalent resistance of the charge pump (Req) depends on the size of its building elements and on its working frequency [2]. In our simulation environment, an equivalent charge pump circuit embedded in a 2Mbits eFlash memory is used. The equivalent resistance of this charge pump is 42 kΩ and the output clamped voltage is about 15 V. For the defect injection simulation, especially for resistive shorts, the previous statements on the electrical charge pump characteristics must be considered.

With the complete simulation environment, including the core-cell array, the logic decoder and the charge pump, the considered defects can be injected and thus the prediction of their impact on different node voltages is possible. This

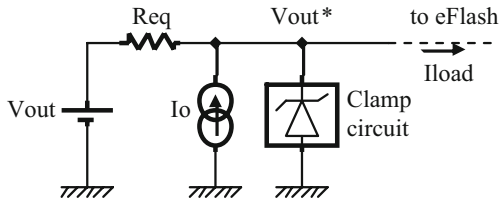

Fig. 9 Charge pump first order equivalent circuit

was done for different defect values but also for the following sequence of operations:

- **Op.1**: Erasing WLi and Writing cell(*i*,*j*).
- **Op.2**: Reading cell(*i*,*j*), cell(*i*,*j*+1) and cell(*i*−1,*j*).
- **Op.3**: Erasing WLi.
- **Op.4**: Reading cell(*i*,*j*), cell(*i*,*j*+1) and cell(*i*−1,*j*).

Note that only cell(*i*,*j*) is written in Op.1 and the other core-cells of the array are considered as erased (VTH → the core-cells contain a logic '1'). Moreover, during Op.1 an erase of the entire word line WLi is performed before a write on cell(*i*,*j*). In the functional work of a 2T-FLOTOX core-cell, a write operation is always preceded by an erase operation. Only the first erase operation is performed from a pseudo-virgin state where the core-cell has its threshold voltage between VTH and VTL. Concerning the read operation, the neighborhood core-cells of cell(*i*,*j*) sharing the same word line are also read to analyze the possible coupling effect induced by each resistive defect. Moreover, simulations have been performed with the following parameters:

- Process: fast.
- Supply voltage: 1.8 V for logic parts.
- Temperature: 25°C.
- Programming time (erase and write operations): 2 ms.

In the following, the impact of each resistive defect is detailed during the four operations (Op.1 to Op.4). Simulations have been performed on a 3*3 eFlash array built with our proposed 2T-FLOTOX core-cell model for which the following electrical values have been extracted:

- Vm corresponding to the charge pump output voltage.
- WLi, Vrefi, and BLj corresponding to the inputs of cell(*i*,*j*).
- Vt value (VTH or VTL) calculated from the floating gate voltage Vfg.
- I_{BL} value corresponding to the read current of a core-cell measured by the sense amplifier.

4.3 Resistive-Short Between Metal and Poly-Silicon Layers

In this sub-section, the resistive-open defects corresponding to the configurations Df1, Df2 and Df3 described previously are analyzed (see Fig. 8).

4.3.1 Df1 Analysis

The impact of defect Df1 (resistive short between WLi and BLj) on the behavior of cell(*i*,*j*) and its neighbors cell(*i*,*j*+1) and cell(*i*−1,*j*) is analyzed. Electrical measurements provided by the model are reported in Table 3.

Op.1: Df1 Impact During a Write Operation In presence of Df1 during a write operation, the voltage of BLj node increases. This effect is due to nominal conditions for which the WLi voltage is always higher than the BLj voltage. For small defect size, Df1 = 10 Ω for example, the BLj voltage becomes equivalent to the WLi level. Concerning the VTL value of cell(*i*,*j*), we see in Table 3 that whatever the size of Df1, it remains stable around −1.1 v.

Cell(*i*,*j*+1), sharing the same word line as cell(*i*,*j*), has its VTH value that begins to be impacted for Df1 less than 100 kΩ, from 2.66 v to 1.47 v. Remember that during Op1 we first erase all core-cells of WLi. During this operation, the high voltage potential (Vpp) undergoes a drop for low value of Df1. Consequently, the erase operation is not well performed on cell(*i*,*j*+1).

The VTH of the cell(*i*−1,*j*) remains unchanged whatever the size of Df1.

Op.2: Df1 Impact During a Read Operation For Op.1, we have seen that the Vt value of the defective written core-cell (VTL) keeps its expected value. During the read operation, the current that passes through the core-cell must correspond to this VTL value, *i.e.* the core-cell must provide a current between 5 µA to 30 µA. However, the current induced by the defect may mask the current provided by cell(*i*,*j*) as illustrated in Fig. 10. Depending on Df1 size, the current on the bit line becomes negative when the current through Df1 becomes higher than the current through the core-cell. Consequently, the sense amplifier interprets this negative current flow on the bit line as a logic '1' instead of a logic '0'. As shown in Table 3, a faulty behavior of the read operation on cell(*i*,*j*) begins to occur for a defect size less than 100 kΩ.

During Op.2, the current read through the cell(*i*,*j*+1) corresponds to a logic '1' whatever Df1 size as the defect has no influence on the bit line j+1.

On the other hand, during the read operation of cell (*i*−1,*j*), the current that passes through the defect makes the sense amplifier providing a logic '0' instead of a logic '1' for Df1 size lower than 1 MΩ.

Op.3: Df1 Impact During an Erase Operation During the erase operation, Df1 involves two main impacts on cell(*i*,*j*); the first one on the BLj node and the second one on the high voltage generation Vm. Without defect during the

Table 3 Electrical simulation results for Df1 injection

Node levels during Opi		Df1 value (Ω)							
		10	100	1 k	10 k	100 k	1 M	10 M	∞
Write Op.1	Vm(V)	15.2	15.2	15.2	15.2	15.2	15.2	15.2	15.2
	WLi(V)	14.4	14.4	14.4	14.5	14.6	14.6	14.6	14.6
	Vrefi(V)	0.351	0.351	0.351	0.351	0.351	0.351	0.351	0.351
	BLj(V)	14.4	14.4	14.4	14.2	12.8	12.5	12.5	12.5
	Vfg1(V)	1.76	1.76	1.76	1.77	1.8	1.86	1.86	1.86
	VTL(V) of cell(i,j)	−1.04	−1.04	−1.04	−1.05	−1.09	−1.16	−1.16	−1.16
	VTH(V) of cell(i,j+1)	1.47	1.47	1.47	1.47	2.11	2.66	2.66	2.66
	VTH(V) of cell(i−1,j)	2.66	2.66	2.66	2.66	2.66	2.66	2.66	2.66
Read Op.2	WLi(V)	2.04	2.07	2.29	2.96	3.26	3.3	3.3	3.3
	Vrefi(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
	BLj(V)	2.03	2.01	1.8	1.23	0.991	0.958	0.955	1
	Iblj(A)	−5.9E−4	−5.75E−4	−4.66E−4	−1.42E−4	5.56E−6	2.6E−5	2.8E−5	2.8E−5
	Ibl of cell(i,j+1)	7.29E−8	7.29E−8	7.29E−8	7.29E−8	0	0	0	0
	Ibl of cell(i−1,j)	2.98E−4	2.9E−4	2.32E−4	7.6E−5	9.97E−6	9.97E−7	0	0
Erase Op.3	Vm(V)	10.7	10.7	10.7	10.9	14.6	15.2	15.2	15.2
	WLi(V)	9.44	9.44	9.24	9.64	13.5	14.5	14.6	14.7
	Vrefi(V)	8.78	8.79	8.82	8.95	12.2	12.8	12.8	12.8
	BLj(V)	9.44	9.42	9.24	7.31	1.45	0.147	0	0
	Vfg1(V)	1.76	1.76	1.76	1.76	0.033	−1.17	−1.27	−1.28
	VTH(V) of cell(i,j)	−1.04	−1.04	−1.04	−1.04	1.06	2.53	2.65	2.66
	VTH(V) of cell(i,j+1)	1.47	1.47	1.47	1.47	2.11	2.66	2.66	2.66
	VTH(V) of cell(i−1,j)	2.66	2.66	2.66	2.66	2.66	2.66	2.66	2.66
READ Op.4	WLi(V)	2.04	2.07	2.3	2.96	3.26	3.3	3.3	3.3
	Vrefi(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
	BLj(V)	2.03	2.01	1.81	1.23	1.03	1	1	1
	Iblj(A)	−5.89E−4	−5.75E−4	−4.66E−4	−1.42E−4	−2.02E−5	−2.29E−6	−2.3E−7	0
	Ibl of cell(i,j+1)	7.29E−8	7.29E−8	7.29E−8	7.29E−8	0	0	0	0
	Ibl of cell(i−1,j)	2.98E−4	2.9E−4	2.32E−4	7.6E−5	9.97E−6	9.97E−7	0	0

erase operation the two transistors of the core-cell are on. As Vss node is set to ground, BLj is pulled-down to this level. Now, in presence of Df1, and depending on its size, BLj is pulled-up to the WLi level. As the two core-cell transistors are 'on' (linear mode), a part of the BLj voltage is present on the drain node of the sense transistor. When the BLj level becomes equivalent to the WLi level, the select transistor becomes saturated and starts to deliver a current through the core-cell. This current passes through the core-cell but also through the defect. The charge pump delivers this defective current. When it reaches a certain value, a drop on the high voltage generation is observed. In Table 3, we observe the increase of the BLj node and the drop on the high voltage generation, *i.e.* on the Vm node. For a defect size of about 10 kΩ the clamp of the Vm level is observed. With the increase of BLj level, the drain level of the FG-transistor increases too. This involves a reduction of the electric field E_{ox} used in the current tunnel equation. Consequently, the Fowler-Nordheim tunneling effect is not efficient enough to inject charges in the floating gate. Due to the reduction in the electric field, the Vt value of cell(*i*,*j*), obtained at the end of the erase operation, remains close to its previous state (VTL). The core-cell does not reach the expected VTH (about +2.66 V for a fault free core-cell). For example, with Df1 = 10 kΩ, the electrical model gives a VTH of about −1.04 V.

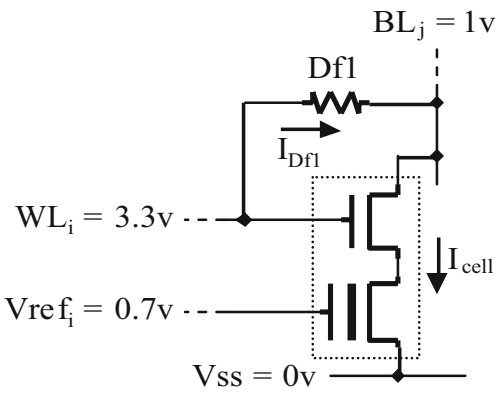

Fig. 10 Df1 impact during a read operation on cell(*i*,*j*)

The Vt values of cell(i,j+1) and cell(i−1,j) remain unchanged, *i.e.* the ones obtained with Op.1.

Op.4: Df1 Impact During a Read Operation According to Df1 values, the expected VTH can never be reached by cell (i,j) and thus keeps its previous state, *i.e.* a low Vt. As in read mode the control gate voltage is 0.7 v, a positive current must be observed through the core-cell. Due to the presence of Df1 and to the voltage conditions between WLi and BLj, we do not observe this current caused by the bad erasing of cell(i,j). But a negative current through Df1 is observed with a value depending on its size. According to Df1 size, this defective current may inhibit the current delivered by the core-cell. In Table 3, we observe that the current read through the bit line never exceeds the sense amplifier threshold. The sense amplifier always reads a logic '1' and that for any Df1 values.

Concerning cell(i,j+1) and cell(i−1,j), the same explanation as for Op.2 can be done.

Conclusion and Fault Modeling From a quantitative point of view, the presence of Df1 is always problematic whatever its size. In fact, a faulty behavior occurs for both small and high defect values. Based on the electrical simulation performed with the proposed model, different faulty behaviors can be associated to functional fault models.

For cell(i,j), as shown before, the write operation is correctly acted while, due to a drop on the high voltage generation, the erase operation is not performed. A read operation after a write will provide a logic '1' due to the current through the defect even if the core-cell has a low Vt. In the same way, a logic '1' is read after an erase operation even if the core-cell has a low Vt. Thus, Df1 behaves like a Stuck-At '1' Fault (SAF1) when it is lower than 100 kΩ.

The presence of Df1 has no impact on cell(i,j+1) behavior while it impacts cell(i−1,j). Cell(i−1,j) is erased (VTH) but any read operation will give a logic '0' as the sense amplifier measures the defective current that passes through the defect. Then, a Stuck-At '0' Fault (SAF0) occurs on cell(i−1,j) when Df1 is lower than 1 MΩ.

4.3.2 Df2 Analysis

In this subsection, the impact of defect Df2 (resistive short between WLi and BLj+1) on the behavior of cell(i,j) and its neighbors cell(i,j+1) and cell(i−1,j) is analyzed. Electrical measurements provided by the model are reported in Table 4.

Op.1: Df2 Impact During a Write Operation The presence of Df2 in the eFlash array during a write operation does not impact the behavior of cell(i,j). The threshold voltage of cell(i,j) remains almost unchanged with the decrease of Df2 size: VTL varies from −1.16 v for Df2=10 MΩ to −0.98 v for Df2=10 Ω.

On the other hand, the Vt of cell(i,j+1) is affected during the write of cell(i,j) with a minimum value of −1.43 v for Df2=100 kΩ.

Finally, cell(i−1,j) is not impacted by the defect and thus its Vt remains unchanged.

Op.2: Df2 Impact During a Read Operation We have seen in the previous operation analysis that the Vt value (VTL) of cell(i,j) keeps roughly its expected value. During the read operation, the current that passes through the core-cell corresponds to this VTL and its value is around 20 µA. However, we can observe that the word line potential WLi goes down with the decrease of Df2. Consequently, the select transistor of the 2T-FLOTOX becomes less conductor inducing a small decrease of the read current provided by cell(i,j). From a logic point view, cell(i,j) after a write operation and in presence of Df2 gives a logic '0' whatever the defect size.

The impact of Df2 on the read operation of cell(i,j+1) is more complex. As seen previously, the write performed on cell(i,j) has impacted the Vt of cell(i,j+1). This corresponds to a flip from VTH to VTL. Thus, the read operation of cell (i,j+1) should provide a logic '0'. Data reported in Table 4 show that the core-cell provides a current that corresponds to a logic '0' for a defect size of about 100 kΩ. For lower defect sizes, the current that passes through the defect masks the current of the core-cell and then a logic '1' is read. This phenomenon is represented in Fig. 11 where waveforms of Vt and IBL of cell(i,j+1) are drawn. From these waveforms, we show that a logic '0' is read when 100 kΩ < Df2 < 400 kΩ.

During the read operation performed on cell(i−1,j), no current is provided by this core-cell through the bit line and thus a logic '1' is always read.

Op.3: Df2 Impact During an Erase Operation As for Df1 injection, the high voltage generation falls down with the decrease of Df2 during the erase operation. In Table 4, the voltage drop of the Vm node for a defect less than 10 kΩ is observed. This voltage drop on Vm induces a reduction of the electric field Eox used in the current tunnel equation. Consequently, the Fowler-Nordheim tunneling effect is not effective to inject charges in the floating gate. Due to this inefficient electric field, the Vt value of cell(i,j) obtained at the end of the erase operation (VTH) remains close to its previous state. The core-cell does not reach the expected VTH (about +2.66 V for a fault free core-cell). For example, with Df2=10 kΩ, the electrical model gives a VTH of about −1.04 V.

Table 4 Electrical simulation results for Df2 injection

Node levels during Opi		Df2 value (Ω)							
		10	100	1 k	10 k	100 k	1 M	10 M	∞
Write Op.1	Vm(V)	15.1	15.1	15.1	15.2	15.2	15.2	15.2	15.2
	WLi(V)	14.4	14.4	14.4	14.5	14.6	14.6	14.6	14.6
	Vrefi(V)	0.351	0.351	0.351	0.351	0.351	0.351	0.351	0.351
	BLj(V)	12.3	12.3	12.3	12.3	12.4	12.4	12.4	12.5
	Vfg1(V)	1.71	1.71	1.72	1.72	1.78	1.86	1.86	1.86
	VTL(V) of cell(i,j)	−0.98	−0.98	−0.992	−0.992	−1.07	−1.16	−1.16	−1.16
	VTH(V) of cell(i,j+1)	−1.38	−1.38	−1.38	−1.38	−1.43	1.38	1.81	2.66
	VTH(V) of cell(i−1,j)	2.66	2.66	2.66	2.66	2.66	2.66	2.66	2.66
Read Op.2	WLi(V)	2.04	2.07	2.29	2.96	3.26	3.3	3.3	3.3
	Vrefi(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
	BLj(V)	0.969	0.969	0.966	0.96	0.957	0.955	0.955	1
	Iblj(A)	1.8E−5	1.9E−5	2.1E−5	2.5E−5	2.67E−5	2.8E−5	2.8E−5	2.8E−5
	Ibl of cell(i,j+1)	−6E−4	−5.8E−4	−4.8E−4	−1.44E−4	7.2E−6	0	0	0
	Ibl of cell(i−1,j)	0	0	0	0	0	0	0	0
Erase Op.3	Vm(V)	10.7	10.7	10.7	10.9	14.6	15.2	15.2	15.2
	WLi(V)	9.52	9.52	9.56	9.64	13.5	14.5	14.7	14.7
	Vrefi(V)	8.86	8.86	8.89	9.02	12.2	12.8	12.8	12.8
	BLj(V)	0.18	0.18	0.18	0.18	0	0	00	0
	Vfg1(V)	1.59	1.59	1.58	1.55	−0.715	−1.25	−1.28	−1.28
	VTH(V) of cell(i,j)	−1.04	−1.04	−1.04	−1.04	1.06	2.53	2.65	2.66
	VTH(V) of cell(i,j+1)	−1.02	−1.02	−1.02	−1.02	1.02	2.64	2.98	2.98
	VTH(V) of cell(i−1,j)	2.66	2.66	2.66	2.66	2.66	2.66	2.66	2.66
Read Op.4	WLi(V)	2.04	2.07	2.3	2.96	3.26	3.3	3.3	3.3
	Vrefi(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
	BLj(V)	0.969	0.969	0.966	0.96	0.957	0.955	0.955	1
	Iblj(A)	1.83E−5	1.86E−5	2.03E−5	2.34E−5	0	0	0	0
	Ibl of cell(i,j+1)	−5.8E−4	−5.7E−4	−4.6E−4	−1.4E−4	−2E−5	−3E−6	0	0
	Ibl of cell (i−1,j)	0	0	0	0	0	0	0	0

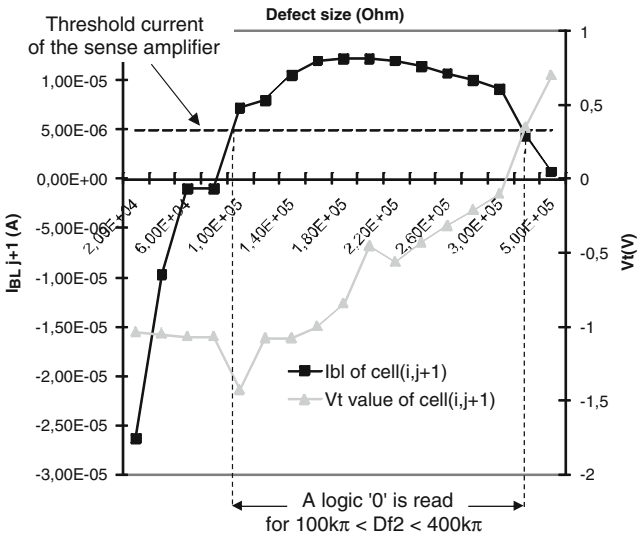

Fig. 11 Vt and I_{BL} of cell(i,j+1) function of Df2 size after a write operation on cell(i,j)

Finally, the Vt values of cell(i,j+1) and cell(i−1,j) remain close to the ones obtained after Op.1.

Op.4: Df2 Impact During a Read Operation We have seen that the expected VTH can never be reached by cell(i,j) for values of Df2 lower than 100 kΩ and thus the core-cell keeps its previous state. Then, when a voltage close to 0.7 v is applied on the control gate of cell(i,j), a current close to 20 μA, corresponding to the low threshold voltage of the core-cell, is observed. This phenomenon occurs when Df2 is less than 100 kΩ and corresponds to a Vt of about −1.04 v on cell(i,j). However, note that Df2 also induces a drop of the WLi net voltage limiting the current delivered by the core-cell but not enough efficient to inhibit it. When Df2 is less than 10 kΩ, a logic '0' is read instead of an expected logic '1' on cell(i,j).

Concerning cell(i,j+1) and cell(i−1,j), the presence of Df2 does not induce a faulty behavior and a logic '1' is always read on these core-cells even if cell(i,j+1) has a low Vt. In that case, the current that passes through the defect masks the current of the core-cell.

Conclusion and Fault Modeling As for Df1, a functional fault modeling can be performed with the help of electrical data provided by our 2T-FLOTOX core-cell model. The presence of Df2 does not disturb the write operation on cell (i,j). The following read gives a logic '0' that corresponds to a low Vt. However, due to a drop on the high voltage generation, Df2 prevents the erase operation, so that the core-cell remains with a low Vt. The read operation on the erased core-cell will provide a logic '0' instead of a logic '1'. This faulty behavior corresponds to a Stuck-At '0' Fault (SAF0) for Df2 lower than 100 kΩ.

As mentioned above, the behavior of cell(i,j+1) is impacted by the presence of Df2 especially when a write operation in performed on cell(i,j). In that case and for 100 kΩ < Df2 < 400 kΩ, the Vt of cell(i,j+1) changes from VTH to VTL. From a functional point of view, a write on a core-cell (aggressor) involves the switch of another core-cell (victim) to a logic '0'. This faulty behavior can be easily modeled by a State Coupling Fault; CFst(0,0).

Finally, cell(i−1,j) is not impacted by Df2.

4.3.3 Df3 Analysis

In this subsection, the impact of defect Df3 (resistive short between WLi-1 and BLj) on the behavior of cell(i,j) and its neighbors cell(i,j+1) and cell(i−1,j) is analyzed. Electrical measurements provided by our model are reported in Table 5.

Op.1: Df3 Impact During a Write Operation The presence of Df3 during a write operation induces a high drop voltage on the Vm generation due to the potential between WLi-1 and BLj. The unselected word line WLi-1 is pulled down to the ground whereas the bit line voltage BLj is close to the Vm potential. The current through the defect is important and the charge pump device cannot deliver such amount of current. That involves the Vt of the cell(i,j) does not reach its expected value VTL and remains quasi unchanged at VTH. In Table 5, we see that this phenomenon occurs for Df3 less than 100 kΩ. For example, when Df3 = 10 kΩ, the Vt value of cell(i,j) is about +2.66 v as the one obtained after an erase operation.

We can also observe in Table 5 that cell(i,j+1) and cell (i−1,j) are not impacted by the presence of Df3. These core-cells keep their Vt values (VTH).

Op.2: Df3 Impact During a Read Operation After a write operation (Op.1), we have seen that for defect Df3 less than 100 kΩ the Vt value of the cell(i,j) remains in an erased state and thus the core-cell is not able to provide any current during the read operation. However, due to the presence of this defect, a defective current between WLi-1 and BLj appears and masks the bad writing effect induced by Df3. From a logical point of view, a logic '0' is read even if the core-cell has a high Vt. The bad writing of cell (i,j) is masked.

Concerning cell(i,j+1) and cell(i−1,j), the expected logic '1' is read.

Op.3: Df3 Impact During an Erase Operation During the erase operation, no problem occurs on the three core-cells. Only a small increase of VTH can be observed on cell(i,j) for Df3 size less than 100 kΩ.

Op.4: Df3 Impact During a Read Operation As explained above for Op.2, a defective current due to Df3 can be measured through the bit line BLj and even if the cell(i,j) state is erased with a VTH value close to +2.66 v. The sense amplifier interprets this current (defective current through the defect) as a logic '0' on the cell(i,j).

Df3 has no impact during Op.4 on cell(i,j+1) and cell (i−1,j) as a logic '1' is read.

Conclusion and Fault Modeling As previously, a functional fault modeling based on electrical data provided by our model has to be performed. The presence of Df3 only impacts the behavior of cell(i,j). This defect prevents the write operation on cell(i,j) but, even if the core-cell has a high Vt after the write operation, the sense amplifier provides a logic '0' during the read. In the same way, the erase operation is performed correctly, but the read after the erase operation gives a logic '0'. Thus, when Df3 is lower than 1 MΩ, it behaves like a Stuck-At '0' Fault (SAF0).

4.4 Resistive Short Between Two Poly-Silicon Layers

In this sub-section, the resistive defects corresponding to Df4 and Df5 (short between two poly-silicon layers) are described (see Fig. 8). Note that these two defects require only a faulty behavior analysis of core-cells belonging to the word line WLi as and not on core-cells belonging to the word line WLi+1. Consequently, we will only consider cell (i,j) and cell(i,j+1) is the following analysis.

4.4.1 Df4 Analysis

In this part, the impact of defect Df4 (resistive short between WLi and Vrefi) on the behavior of cell(i,j) and its neighbor cell(i,j+1) is analyzed. Electrical measurements provided by our model are reported in Table 6.

Op.1: Df4 Impact During a Write Operation The presence of Df4 during a write operation induces an increase of

Table 5 Electrical simulation results for Df3 injection

Node levels during Opi		Df3 value (Ω)							
		10	100	1 k	10 k	100 k	1 M	10 M	∞
Write Op.1	Vm(V)	2.18	2.22	2.62	6	14.4	15.2	15.2	15.2
	WLi(V)	2.15	2.19	2.58	5.85	13.9	14.7	14.7	14.7
	Vrefi(V)	0.292	0.293	0.296	0.316	0.349	0.351	0.351	0.351
	BLj(V)	0.49	0.521	0.843	3.74	11.4	12.4	12.5	12.5
	Vfg1(V)	−1.31	−1.31	−1.31	−1.31	0.917	1.8	1.86	1.86
	VTL(V) of cell(i,j)	2.66	2.66	2.66	2.66	−1.39E−2	−1.09	−1.16	−1.16
	VTH(V) of cell(i,j+1)	2.66	2.66	2.66	2.66	2.66	2.66	2.66	2.66
	VTH(V) of cell(i−1,j)	2.66	2.66	2.66	2.66	2.66	2.66	2.66	2.66
Read Op.2	WLi(V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
	Vrefi(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
	BLj(V)	0.51	0.522	0.62	0.877	0.959	0.954	0.954	1
	Iblj(A)	2.9E−4	2.9E−4	2.3E−4	7.6E−5	2.6E−5	2.8E−5	2.8E−5	2.8E−5
	Ibl of cell(i,j+1)	0	0	0	0	0	0	0	0
	Ibl of cell (i−1,j)	−6E−4	−5.8E−4	−4.8E−4	−1.6E−4	−2.2E−5	−2.2E−6	−2.3E−7	0
Erase Op.3	Vm(V)	15.2	15.2	15.2	15.2	15.2	15.2	15.2	15.2
	WLi(V)	14.7	14.7	14.7	14.7	14.7	14.7	14.7	14.7
	Vrefi(V)	12.8	12.8	12.8	12.8	12.8	12.8	12.8	12.8
	BLj(V)	0	0	0	0	0	0	0	0
	Vfg1(V)	−1.55	−1.55	−1.55	−1.55	−1.28	−1.28	−1.28	−1.28
	VTH(V) of cell(i,j)	3	3	3	3	2.66	2.66	2.66	2.66
	VTH(V) of cell(i,j+1)	2.66	2.66	2.66	2.66	2.66	2.66	2.66	2.66
	VTH(V) of cell(i−1,j)	2.66	2.66	2.66	2.66	2.66	2.66	2.66	2.66
Read Op.4	WLi(V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
	Vrefi(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
	BLj(V)	0.51	0.522	0.62	0.877	0.959	0.954	0.954	1
	Iblj(A)	3E−4	2.9E−4	2.3E−4	7.65E−5	9.7E−6	1E−8	1E−7	0
	Ibl of cell(i,j+1)	0	0	0	0	0	0	0	0
	Ibl of cell(i−1,j)	−6E−4	−5.8E−4	−4.8E−4	−1.6E−4	−2.2E−5	−2.2E−6	−2.3E−7	0

Vrefi. In fact, due to this resistive short, Vrefi is loaded by the potential applied on WLi. This effect begins earlier with a defect size close to 1 MΩ. Due to the increase of Vrefi, the write operation is not performed and cell(i,j) remains erased with a high Vt. Moreover this defect also induces a small increase of VTH on all core-cells belonging to WLi. Table 6 shows that Vt values of cell(i,j) and cell(i,j+1) reach about +4.84 v.

Op.2: Df4 Impact During a Read Operation Due to the presence of Df4 we have seen that the write operation is inhibited even for high defect values. Thus, during the read operation, a logic '1' is observed instead of an expected logic '0'.

Op.3: Df4 Impact During an Erase Operation During the erase operation, no problem occurs on core-cells sharing WLi. Only a small increase of VTH can be observed on all core-cells belonging to WLi for Df4 size less than 1 MΩ.

Op.4: Df4 Impact During a Read Operation During this operation, the presence of Df4 does not disturb the read-out content. The expected logic '1' is read in all core-cells sharing WLi.

Conclusion and Fault Modeling To conclude the Df4 study and to analyze this defect from a functional point of view, the presence of Df4 can be interpreted as a Stuck-At '1' Fault (SAF1). This fault model occurs when Df4 has a size lower than 10 MΩ.

4.4.2 Df5 Analysis

In this part, the impact of defect Df5 (resistive short between WLi and WLi+1) on the behavior of cell(i,j) and its neighbor cell(i,j+1)) is analyzed. Electrical measurements provided by our model are reported in Table 7.

Op.1: Df5 Impact During a Write Operation The presence of Df5 during a write operation induces a drop on the high

Table 6 Electrical simulation results for Df4 injection

Node levels during Opi		Df4 value (Ω)							
		10	100	1 k	10 k	100 k	1 M	10 M	∞
Write Op.1	Vm(V)	2.18	2.22	2.62	6	14.4	15.2	15.2	15.2
	WLi(V)	14.7	14.7	14.7	14.7	14.7	14.7	14.7	14.7
	Vrefi(V)	14.7	14.7	14.7	14.7	14.7	14.7	14.6	0.351
	BLj(V)	12.5	12.5	12.5	12.5	12.5	12.5	12.5	12.5
	Vfg1(V)	−3.07	−3.07	−3.07	−3.07	−3.07	−3.07	−1.1	1.86
	VTL(V) of cell(i,j)	4.84	4.84	4.84	4.84	4.84	4.84	−1.16	−1.16
	VTH(V) of cell(i,j+1)	4.84	4.84	4.84	4.84	4.84	4.84	4.03	2.66
Read Op.2	WLi(V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
	Vrefi(V)	3.29	3.29	3.29	3.29	3.29	2.67	0.756	0.7
	BLj(V)	1	1	1	1	1	1	1	1
	Iblj(A)	0	0	0	0	0	0	0	2.8E−5
	Ibl of cell(i,j+1)	0	0	0	0	0	0	0	0
Erase Op.3	Vm(V)	15.2	15.2	15.2	15.2	15.2	15.2	15.2	15.2
	WLi(V)	14.7	14.7	14.7	14.7	14.7	14.7	14.7	14.7
	Vrefi(V)	14.7	14.7	14.7	14.7	14.7	14.6	12.8	12.8
	BLj(V)	0	0	0	0	0	0	0	0
	Vfg1(V)	−3.32	−3.32	−3.32	−3.32	−3.32	−3.26	−3.05	−1.28
	VTH(V) of cell(i,j)	4.82	4.82	4.82	4.82	4.82	4.82	4.82	2.66
	VTH(V) of cell(i,j+1)	4.84	4.84	4.84	4.84	4.84	4.84	4.84	2.66
Read Op.4	WLi(V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
	Vrefi(V)	3.29	3.29	3.29	3.29	3.29	2.67	0.756	0.7
	BLj(V)	1	1	1	1	1	1	1	1
	Iblj(A)	0	0	0	0	0	0	0	0
	Ibl of cell(i,j+1)	0	0	0	0	0	0	0	0

voltage generation due to the potential between WLi and WLi+1. In fact, the word line WLi+1 is unselected and its potential is pull down to the ground (a strong 0 v) whereas the selected word line WLi is pull up to the Vm potential. The current passing through the defect cannot be delivered by the charge pump device. Note that before this write operation, an erase has been performed and the same problem has been observed. The high voltage drop related to Df5 involves an impact on the Vt of the cell(*i*,*j*). The Vt does not reach its expected value VTL and remains quasi unchanged to the virgin value. In Table 7, we see that this phenomenon occurs for Df5 size less than 100 kΩ.

We can also observe in Table 7 that cell(*i*,*j*+1) is impacted by the presence of Df5 because the erase operation due to the defective current passing through Df5 is not correctly acted. To generalize, core-cells belonging to WLi have their Vt window (VTW) considerably reduced due to the weak erase and write operations induced by Df5.

Op.2: Df5 Impact During a Read Operation After a write operation (Op.1), for Df5 less than 100 kΩ, the Vt value of the cell(*i*,*j*) remains close to its virgin state and the core-cell is not able to provide any current during the read operation. Thus, a logic '1' is read instead of an expected logic '0' for a Df5 size less than 100 kΩ. This also true for the other core-cells belonging to WLi in which a logic '1' is always read but note that for these core-cells this is the expected value.

Op.3: Df5 Impact During an Erase Operation During the erase operation, the same problem as for Op.1 occurs (a drop on the high voltage generation) and impacts the Vt values of the core-cells sharing WLi. All the Vt values of these core-cells are close to their virgin values due to the inhibition of the erase operation induced by the presence of Df5. This problem appears when Df5 begins to be less than 100 kΩ.

Op.4: Df5 Impact During a Read Operation As explained above for the previous operations, Df5 inhibits write and erase and thus the core-cell remain virgin. The limit of this faulty behavior is when Df5 is less than 100 kΩ. Due to this problem, a logic '1' is always read on these core-cells whatever the operation performed on them.

Conclusion and Fault Modeling Modeling the faulty behavior induced by Df5 is very easy. When Df5 is less

Table 7 Electrical simulation results for Df5 injection

Node levels during Opi		Df5 value (Ω)							
		10	100	1 k	10 k	100 k	1 M	10 M	∞
Write Op.1	Vm(V)	2.18	2.22	2.62	6	14.4	15.2	15.2	15.2
	WLi(V)	2.15	2.19	2.58	5.85	13.9	14.7	14.7	14.7
	Vrefi(V)	0.292	0.293	0.296	0.316	0.349	0.351	0.351	0.351
	BLj(V)	0	0	0.2	3.55	11.6	12.4	12.5	12.5
	Vfg1(V)	0.31	0.31	0.31	0.31	0.51	1.8	1.86	1.86
	VTL(V) of cell(i,j)	0.73	0.73	0.73	0.73	0.49	−1.09	−1.16	−1.16
	VTH(V) of cell(i,j+1)	0.79	0.79	0.79	0.79	2.66	2.66	2.66	2.66
Read Op.2	WLi(V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
	Vrefi(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
	BLj(V)	0.954	0.954	0.954	0.954	0.954	0.954	0.954	1
	Iblj(A)	0	0	0	0	6E−6	2.8E−5	2.8E−5	2.8E−5
	Ibl of cell(i,j+1)	0	0	0	0	0	0	0	0
Erase Op.3	Vm(V)	2.18	2.22	2.62	6	14.4	15.2	15.2	15.2
	WLi(V)	2.15	2.19	2.58	5.85	13.9	14.7	14.7	14.7
	Vrefi(V)	0	0	0.5	3.8	11.8	12.8	12.8	12.8
	BLj(V)	0	0	0	0	0	0	0	0
	Vfg1(V)	0.31	0.31	0.31	0.31	−0.09	−0.95	−1.28	−1.28
	VTH(V) of cell(i,j)	0.73	0.73	0.73	0.73	1.2	2.26	2.66	2.66
	VTH(V) of cell(i,j+1)	0.79	0.79	0.79	0.79	2.66	2.66	2.66	2.66
Read Op.4	WLi(V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
	Vrefi(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
	BLj(V)	0.954	0.954	0.954	0.954	0.954	0.954	0.954	1
	Iblj(A)	0	0	0	0	0	0	0	0
	Ibl of cell(i,j+1)	0	0	0	0	0	0	0	0

than 100 kΩ, a Stuck-At '1' Fault (SAF1) is observed whereas for defects above this limit the core-cells are fault free.

4.5 Fault Modeling Summary

In the previous investigations, all resistive defects that may induce a faulty behavior of the eFlash core-cell have been analyzed. From these different failure mechanisms, a functional fault modeling has been performed. Table 8 summarizes the different fault models associated to each defect and targeted core-cells. In this table, we also report the defect size thresholds at which these faulty behaviors occur. The obtained functional fault models correspond to the memory testing literature; SAF0, SAF1 and more complex faults such as coupling fault CFst(0,0).

Compared to previous studies published on eFlash memory testing, the main contribution of this paper lies in the fact that the proposed simulation model now allows to perform a functional fault modeling for any actual defect in an eFlash. Fault modeling is done from electrical simulations, using all the operations that an eFlash can perform, *i.e.* read, erase and write operations. The next step in this work will consist in verifying if a test sequence generally used for eFlash testing detects all the fault models resulting from the defect analysis. The test sequence will be modified if it is not able to detect some fault models.

Table 8 Fault modeling summary

Defect	Cell(*i*,*j*)		Cell(*i*,*j*+1)		Cell (*i*−1,*j*)	
	Defect size	Fault model	Defect size	Fault model	Defect size	Fault model
Df1	<100 kΩ	SAF1	–	–	<1 MΩ	SAF0
Df2	<10 kΩ	SAF0	100 kΩ < … < 400 kΩ	CFst(0,0)	–	–
Df3	<100 kΩ	SAF0	–	–	–	–
Df4	<10 MΩ	SAF1	–	–	–	–
Df5	<100 kΩ	SAF1	–	–	–	–

5 Conclusion

In this paper we have explored the possibilities to create a simulation model of the 2T-FLOTOX core-cell. We have detailed the different steps required to create this model and its basic scheme. From measurements on the 0.15 µm ATMEL technology, we have validated this first order 2T-FLOTOX core-cell model.

With the help of the proposed model resistive defect injections have been performed and the resulting faulty behaviors have been modeled from knowledge of the CMOS memory test literature.

In a future work, further investigations on any other kind of defects [3, 4] will be done with the help of our SPICE model. For each defect, we will analyze the faulty behavior to finally give a comprehensive set of fault models. Finally, with a complete eFlash electrical defect analysis, we will be able to validate and enhance the existing eFlash test solution.

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A Complete Resistive-Open Defect Analysis for Thermally Assisted Switching MRAMs

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***Abstract*— Magnetic random access memory (MRAM) is an emerging technology with potential to become the universal on-chip memory. Among existing MRAM technologies, thermally assisted switching (TAS)-MRAM technology offers several advantages compared with other technologies: selectivity, single magnetic field, and high-integration density. In this paper, we analyze the impact of resistive-open defects on TAS-MRAM behavior. Electrical simulations were performed on a hypothetical 16 word TAS-MRAM architecture enabling any combination of read and write operations. Results show that read and write sequences may be affected by resistive-open defects that may induce single and double-cell faulty behaviors. As a next step, we will exploit the analyses results to guide the test phase by providing effective test algorithms targeting faults related to actual defects affecting TAS-MRAM architectures.**

***Index Terms*— Fault modeling, nonvolatile memories (NVM), resistive-open defects, spintronics, thermally assisted switching (TAS)-MRAM, test.**

I. Introduction

CONSUMER applications like digital audio players and tablet PCs require more and more integration of nonvolatile embedded memories. Memories occupy most of the silicon area in today's system-on-chip according to the International Technology Roadmap for Semiconductors (ITRS) [1]. Though widely used, nonvolatile flash memories still have several drawbacks, such as high-supply voltage requirement and susceptibility to reliability issues due to high-electric field for programming operations. On the other side, magnetic random access memory (MRAM) is an emerging technology with high-data processing speed, low-power consumption and high-integration density compared with flash memories. In addition, these memories are nonvolatile with fair processing speed and reasonable power consumption when compared with static RAMs (SRAMs). Additionally, MRAMs are entirely compatible with complementary metal oxide semiconductor (CMOS) fabrication process [2]. MRAM probably is the closest to an ideal universal memory since it is nonvolatile and fast, and can be cycled indefinitely. Thus, MRAM may be used as nonvolatile memory (NVM) as well as SRAM and DRAM according to the ITRS [1].

In MRAM, data is stored in a magnetic tunnel junction (MTJ), which is generally composed of two ferromagnetic (FM) layers separated by an insulating layer. Normally, one layer is pinned and acts as a reference layer and the other one is free and can be switched between, at least, two stable states during a write operation.

MRAMs have the potential to mitigate almost all flash related issues. However, they are prone to defects as any other kind of memory. Only few papers on MRAM testing can be found in the literature, and target mainly field induced magnetic switching (FIMS)-MRAMs technologies. In [3]–[5], authors present the write disturbance fault model, a fault that affects data stored in toggle MRAM cells due to the amount of magnetic field applied during write operations on neighboring cells. In [6], two new faults related to the magnetic junction behavior were identified: multivictim fault, in which a cluster of cells can easily change their magnetization state due to process variations; and kink fault, in which the hysteresis loop shrinks because of its relation with cell shape, thus changing MTJ resistivity.

A thorough investigation and deep analysis must be done for testing MRAMs memories. In [7], a first analysis of resistive-open defects in thermally assisted switching (TAS)-MRAM memory architecture is presented. This preliminary study has revealed the importance of electrical analyses of defects that may impact the functionality of TAS-MRAMs.

In this paper, we present a complete study while considering seven resistive-open defect locations. We first develop a TAS-MRAM architecture able to perform any read/write sequences. The injected resistive-open defects are classified into three categories: 1) defects that directly impact MTJ's heat current; 2) defects that indirectly impact the MTJ's heat current; and 3) defects that impact field-line current. The impact of each defect category is analyzed.

Related fault models are well-known fault models in memory test [8] such as stuck-at fault, transition fault (TF), and write destructive (WD) for single cell faults and state coupling fault (SCF) for double cell faults. This fault model association will be helpful for the development of effective test algorithms dedicated to TAS-MRAMs.

The rest of this paper is organized as follows. Section II provides fundamentals on MRAM technologies. The proposed

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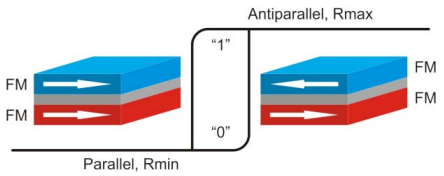

Fig. 1. MTJ in parallel and antiparallel states.

TAS-MRAM architecture is described in Section III. Resistive-open defect analyses are provided in Section IV. Finally, Section V concludes this paper.

II. MRAM Technologies

MRAMs are spintronic devices that store data in MTJs. A basic MTJ device is usually composed of two FM layers separated by an insulating layer, as shown in Fig. 1. One of the FM layers is pinned and acts as a reference layer. The other one is free and can be switched between, at least, two stable states. These states are parallel or antiparallel with respect to the reference layer. When the MTJ is in the parallel state, it offers the minimum resistance ($R_{\min}$) while the maximum resistance ($R_{\max}$) is obtained when antiparallel. The difference between $R_{\min}$ and $R_{\max}$, quantified by the tunnel magneto resistance (TMR), is high enough to be sensed during a read operation.

A read operation consists in determining the MTJs magnetization state and can be performed by voltage or current sensing across the MTJ stack. A CMOS sense amplifier is used to retrieve the stored bit information. High-TMR allows simple and stable sense amplifiers, improving reading accuracy [9].

Magnetization dynamics describes how the magnetization goes from one point of equilibrium to another one. This evolution of the magnetization in terms of time and space under a local effective field can be described by the Landau–Lifshitz–Gilbert equation

$$\frac{\partial \vec{m}}{\partial t} = -\frac{\gamma}{1+\alpha^2}\vec{m} \times \overrightarrow{H_{\text{eff}}} - \frac{\gamma\,\alpha}{1+\alpha^2}\vec{m} \times \left(\vec{m} \times \overrightarrow{H_{\text{eff}}}\right) \quad (1)$$

where $\vec{m}$ is the unit vector along the magnetization of the free layer, γ is the gyromagnetic ratio, α is the Gilbert damping constant, and H_{eff} is the effective magnetic field.

A write operation can be performed using magnetic fields or spin polarized current and depends on MRAM technologies: FIMS, toggle switching, TAS, and current induced magnetic switching (CIMS).

FIMS-MRAM generation relies on the Stoner–Wohlfarth theory of coherent rotation in single domain particles [10]. In this approach, the energy required to reverse the magnetization is minimized by applying simultaneously two perpendicular magnetic fields. The MTJ is fully selected when two magnetic fields are applied to it. Finding a set of magnetic fields which can be used to program all cells becomes difficult due to the very narrow write margin in this technology [11]. A small deviation of MTJs characteristics has a huge influence in the switching field distribution in large bit arrays. Another issue is the thermal activation of half-selected MTJs, which increases addressing errors.

A new approach called toggle switching was proposed in [12] to overcome the selectivity issue of FIMS technology. The FM layers were replaced by synthetic layers. This methodology relies on the unique behavior of the synthetic antiferromagnet free layer. In toggle memories a prior read is mandatory as it is only possible to toggle the state. This drawback is compensated by the advantage of using single current polarity to create the magnetic fields.

TAS is an alternative switching method for MRAMs. In the scheme proposed in [13] and industrialized by Crocus Technology, the MTJ is modified by inserting an anti-FM (AFM) layer that pins the storage layer while below its blocking temperature (T_B) that can be calculated by

$$T_B = \frac{KV}{k_B \ln\left(\frac{\tau_m}{\tau_0}\right)} \quad (2)$$

$$\tau_N = \tau_0 e^{\left(\frac{KV}{k_B T}\right)} \quad (3)$$

where k_B is the Boltzmann constant, τ_m is the measurement time of the magnetization, τ_0 is the attempt time, and τ_N (3) is the Néel relaxation time. The temperature for which $\tau_m = \tau_N$ is called blocking temperature T_B.

In AFM materials, the magnetic moments of atoms are aligned in a regular pattern neighboring spins pointing in opposite directions. This organization vanishes above T_B and the material becomes paramagnetic and the storage layer is freed and can be reversed under the application of a magnetic field provided by a single field-line. The magnetic field is maintained beyond the heating voltage pulse to ensure the correct pinning of the storage layer.

TAS approach offers several advantages. The selectivity problem is reduced since only heated MTJs are able to switch and all other MTJs remain in their stable state as they are below their blocking temperature. Although TAS needs an additional heating current, this current is much smaller than the current used to generate the second magnetic field in FIMS-MRAMs. The integration density is improved due to thermal stability and the need of only one field-line.

CIMS is the most recent and promising MRAM technology. The writing is accomplished by injecting a spin-polarized high-current density through MTJ without the assistance of any external magnetic field [14]. This approach relies on the spin transfer torque (STT) effect. However, there are some problems to solve in this recent technology. Lowering the write current density while maintaining data stability and improving the read signal are the main concerns of spin induced reversal mechanism. This raises considerable challenges since the MRAM cells must be able to withstand high-current densities without exceeding the MTJs breakdown voltage. Some circuit design techniques for reducing the write current density have already been proposed in [15].

III. TAS-MRAM Architecture

Fig. 2 shows the TAS-MRAM architecture that we have developed for our paper. The organization is done in a square matrix that has 2^{MR} rows and 2^{NC} columns, for a total storage capacity of $2^{\text{MR+NC}}$ bit per page, where MR and NC are the

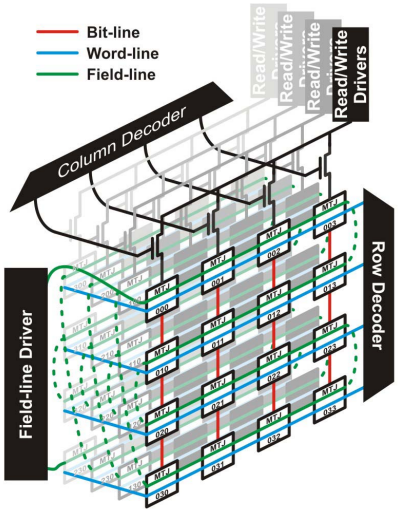

Fig. 2. TAS-MRAM architecture.

number of bits used to specify the row and column address, respectively. In this paper, MR and NC are equal to two and the number of pages is four. Hence, the storage capacity is 64 bits (16 words of 4 bits). Each cell in the array is connected to one of the row-lines, called word-lines, and connected to one of the column-lines, called bit-lines. A particular set of MTJs can be accessed for a read or write operation by selecting its word-line and bit-line. There is only one field-line that connects all MTJs serially row by row passing through all pages in this architecture.

During a read operation, the read driver applies a small voltage that generates negligible heat to both the selected MTJ and a reference MTJ. The reference MTJ is halfway between the high- and low-resistance values. The resistance difference is then sensed to determine the stored data in the selected MTJ.

The write operation is performed as follows.

1) Initially, the write driver applies a voltage to heat the selected MTJ above its blocking temperature (∼150 °C).
2) Next, the field-line driver applies a current to generate the data zero magnetic field. While the MTJ is cooled down below MTJs blocking temperature, the magnetic field is maintained.
3) Then, the field-line driver inverses the current direction and the MTJ is heated again to perform the write 1 operation, if needed. When the MTJ reaches room temperature, the writing procedure is accomplished.

This approach allows writing logic 0 and logic 1 in one cycle to different MTJs sharing the same field-line. Note that, a Write 1 operation (denoted *W1*) consists of applying both field-line current polarities (magnetic field for data 0 and then magnetic field for data 1), while a Write 0 operation (denoted *W0*) consists of applying only one field-line current polarity (magnetic field for data 0 only). These writing procedures are inspired by the flash programming procedures where a write operation (write 1) is always preceded by an erase operation (write 0).

TABLE I
$MTJ_{1,1,1}$ CHARACTERISTICS UNDER READ/WRITE OPERATIONS

Operation	$MTJ_{1,1,1}$ parameters					S (mV)
	V (mV)	I (uA)	R (kΩ)	T (°C)	M	
R0	111.49	74.89	1.48	31.16	1	165.67
R1	202.35	72.11	2.80	34.26	-1	254.49
W0	745.32	606.59	1.22	193.18	1	n.a.
W1	745.32 863.09	606.59 542.63	1.22 1.59	193.18 183.75	-1	n.a.

Electrical simulations were performed using the TAS-MTJ model developed by Spintec [13]. This model is based on the physical equations of the MTJ and is calibrated with respect to the targeted TAS-MRAM technology. In addition, this model is compiled in C language and is compatible with the Spectre simulator of the standard Cadence design suite [16].

Table I summarizes simulated fault-free characteristics of $MTJ_{1,1,1}$ ($MTJ_{i,j,k}$ with $i \Rightarrow$ page number, $j \Rightarrow$ row number, and $k \Rightarrow$ column number) in the second page, second column, and second line of the TAS-MRAM architecture shown in Fig. 2. The first column in the table gives the four possible operations *R0*, *R1*, *W0*, and *W1*. The next five columns provide all the MTJs parameters.

1) V: voltage level at the MTJ interface.
2) I: current passing through the MTJ during read or write operations.
3) R: resistance of the MTJ.
4) T: temperature of the MTJ during operations.
5) M: magnetization state that is related to the angle between the two FM layers. The parallel magnetization state is represented ideally by $1 \Rightarrow$ logic 0 and the antiparallel magnetization state by $-1 \Rightarrow$ logic 1.

Finally, the last column gives the sensing voltage (S) during read operation only. The two resistive states of the MTJ are well centered in 1.48 kΩ for $R_{\min}$ and 2.80 kΩ for $R_{\max}$ during read operation. In normal operation, the sensing voltage (S) is around 165 mV for $R_{\min}$ and 254 mV for $R_{\max}$ which should be sensed by a robust sense amplifier due to narrow 89 mV excursion. This excursion is related to read driver strength which can be increased to facilitate the design of the sense amplifier worsening power consumption.

The sense amplifier reference has its resistivity well centered in between $R_{\min}$ and $R_{\max}$. All sensing voltages above 232.29 mV are considered data 1, below 187.88 mV are considered data 0 and in between these two values are not reliable due to possible dissymmetry of the sense amplifier.

During write operations, the current that passes through the MTJ is high enough to heat its temperature above the blocking temperature, i.e., 193 °C for *W0* and 193/183 °C for *W1*. While cooling time depends on material properties only, heating time can be engineered modifying the heating current. One write cycle is enough to heat up and cool down selected MTJs locally. The minimum distances between cells consider of neighboring cells heating.

During read and write operations, the MTJs resistivity is different, even if the magnetization state is the same. This is

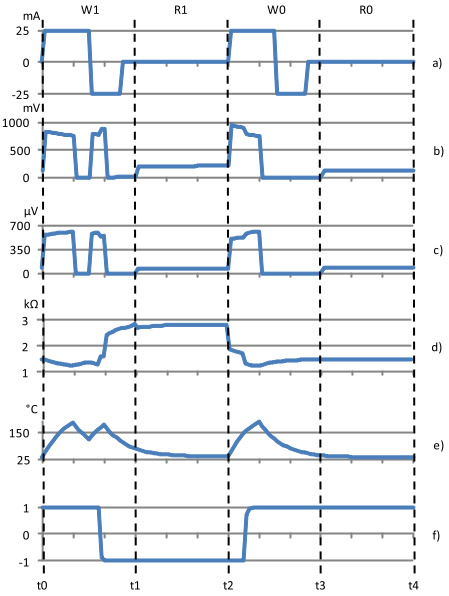

Fig. 3. MTJ parameters for a *W1_R1_W0_R0* operation sequence.

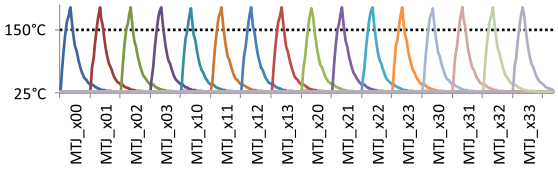

Fig. 4. 16-bit *W0* fault-free temperature profiles.

due to the voltage applied to the MTJ as well as its operating temperature.

In Fig. 3, we present how the following MTJ's parameters change over time for a *W1_R1_W*0*_R*0 sequence.

a) Applied field-line current.
b) Voltage at MTJ's interface.
c) Current passing through MTJ.
d) MTJ's resistivity.
e) MTJ's core temperature.
f) MTJ's magnetization state.

The writing approach previously described can be observed from *t0* to *t1* where a *W1* operation is performed and from *t2* to *t3* where a *W0* operation is performed. *R1* and *R0* operations are performed from *t1* to *t2* and from *t3* to *t4*, respectively. Note that magnetization state is able to switch when MTJ's temperature is above T_B and enough field-line current is applied.

Figs. 4 and 5 show temperature profiles for *W0* and *W1* operations performed on a 16-bit fault-free TAS-MRAM memory page, respectively. Note that MTJs are written row by row from $\text{MTJ}_{x,0,0}$ to $\text{MTJ}_{x,3,3}$. We observe that temperature rises twice during each write cycle in *W1* operations and rises only once per cycle in *W0* operations. In these cases all write operations are correctly performed.

IV. Resistive-Open Defect Analysis

Resistive-open defects have become one of the most significant issues in deep submicron CMOS technologies. This kind

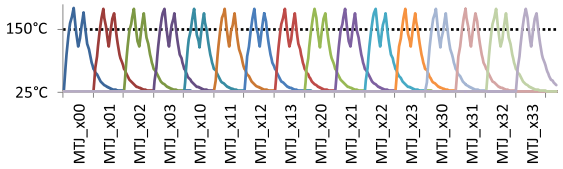

Fig. 5. 16-bit *W1* fault-free temperature profiles.

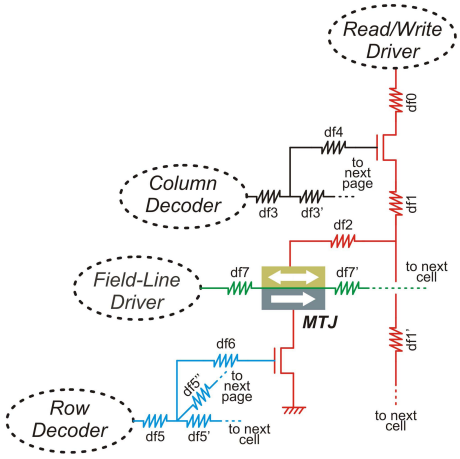

Fig. 6. Resistive-open defects injection.

of defects can represent mainly ill-formed wires and contacts [17]. The resistive-open defect injection in TAS-MRAM architecture is depicted in Fig. 6 and considers both magnetic and CMOS fabrication processes. Resistive-open defects are inserted on interconnects of the memory array as follows.

1) Defects that directly impact MTJ's heat current:
   a) df0: global defect placed before the reading sense amplifier affecting bit-line heat path.
   b) df1: global defect placed after the reading sense amplifier affecting the bit-line heat path.
   c) df1′: distributed defect along the bit-line heat path.
   d) df2: local defect placed after the reading sense amplifier affecting a single MTJ heat path.
2) Defects that indirectly impact the MTJ's heat current:
   a) df3: global defect affecting the (column) bit-line selection transistor of all pages.
   b) df3′: distributed defect along the pages affecting up to three pages.
   c) df4: local defect affecting a single (on a single page) bit-line selection transistor.
   d) df5: global defect affecting the (row) word-line of all pages.
   e) df5′: distributed defect in the same page affecting up to three selection transistors.
   f) df5″: distributed defect along the pages affecting up to three pages.
   g) df6: local defect affecting a single MTJ selection transistor on a single page.
3) Defects that impact field-line current:
   a) df7: global defect affecting the field-line path.

TAS-MRAM operation is affected by these resistive-open defects in several ways. In the following, we show a complete

TABLE II
MTJ$_1$, 1, 1 CHARACTERISTICS UNDER DEFECTS THAT DIRECTLY IMPACT THE HEAT CURRENT

Defect size			*0W1*	*1W1*	*1W0*	*0W0*
	Field-line	mA	±25			
	Initial Magnetization		1	-1	-1	1
390Ω	**Current**	µA	542.54 539.76	543.80 485.65	543.80 -	542.54 -
	Voltage	mV	693.35 699.44	691.07 817.64	691.07 -	693.35 -
	Temperature	°C	166.16 156.20	172.50 159.66	172.50 -	166.16 -
	Final Magnetization		-1	-1	+1	+1
400Ω	**Current**	µA	541.03 538.31	541.72 484.25	541.72 -	541.03 -
	Voltage	mV	692.04 698.04	689.93 816.56	689.93 -	692.04 -
	Temperature	°C	165.51 **155.59**	171.96 158.80	171.96 -	165.51 -
	Final Magnetization		+1	-1	+1	+1
600Ω	**Current**	µA	512.35 510.16	462.49 459.56	462.49 -	512.35 -
	Voltage	mV	666.33 671.56	785.18 792.10	785.18 -	666.33 -
	Temperature	°C	153.38 144.25	161.54 151.20	161.54 -	153.38 -
	Final Magnetization		+1	-1	+1	+1
610Ω	**Current**	µA	510.99 508.84	461.15 457.31	461.15 -	510.99 -
	Voltage	mV	665.07 670.25	784.33 793.04	784.33 -	665.07 -
	Temperature	°C	152.81 143.72	161.01 **149.94**	161.01 **-**	152.81 -
	Final Magnetization		+1	+1	+1	+1
640Ω	**Current**	µA	506.95 504.84	457.45 454.76	457.45 -	506.95 -
	Voltage	mV	661.30 666.41	781.19 787.66	781.19 -	661.30 -
	Temperature	°C	151.12 142.14	159.42 149.22	159.42	151.12 -
	Final Magnetization		+1	+1	+1	+1
650Ω	**Current**	µA	505.62 503.53	456.20 453.59	456.20 -	505.62 -
	Voltage	mV	660.05 665.12	780.16 786.49	780.16 -	660.05 -
	Temperature	°C	150.56 141.62	158.90 148.81	**158.90** -	150.56 -
	Final Magnetization		+1	-1	-1	+1

analysis of how these seven resistive-open defects impact the TAS-MRAM behavior. In addition to ill-formed wires and contacts these defects can represent misbehavior of memory components such as drivers, decoders, and sense amplifiers.

A. Defects That Directly Impact MTJ's Heat Current

The current that passes through the MTJ is responsible for heating the device above its blocking temperature during write operations. This current is also important to retrieve the MTJ's logic state during read operations. Table II summarizes field-line currents applied and MTJ$_{1,1,1'}$s simulated characteristics (same as Table I) under six resistive-open defect sizes. Simulations were performed using the following write sequences.

1) *0W1: W1* operation performed on MTJ$_{1,1,1}$ that initially contains logic 0. This sequence corresponds to a rising transition.

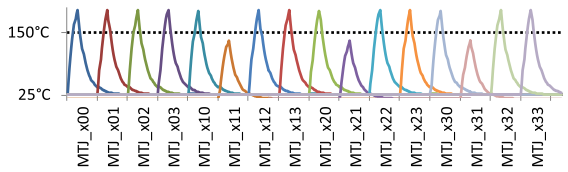

Fig. 7. 16-bit *W0* temperature profiles under df1′ = 1 kΩ.

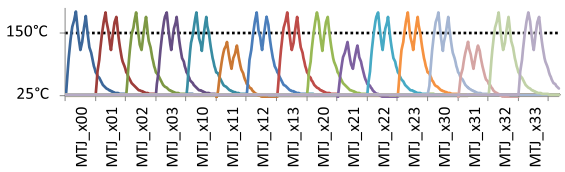

Fig. 8. 16-bit *W1* temperature profiles under df1′ = 1 kΩ.

2) *1W1: W1* operation performed on $MTJ_{1,1,1}$ that initially contains logic 1. This sequence allows verifying the *W1* operation since it applies both field-line current polarities.
3) *1W0: W0* operation performed on $MTJ_{1,1,1}$ that initially contains logic 1. This sequence corresponds to a falling transition.
4) *0W0: W0* operation performed on $MTJ_{1,1,1}$ that initially contains logic 0. There is no transition in this sequence.

The observed switching of the magnetization state is equivalent for df0, df1, and df2 during write sequences. For resistive-open defects up to 390 Ω all write operations were correctly performed.

For a resistive-open defect of 400 Ω, the *0W1* sequence is corrupted. In that case, the current passing through the magnetic junction is enough to heat $MTJ_{1,1,1}$ above its blocking temperature (150 °C) but the amount of time that MTJ remains above this temperature while data 1 magnetic field is applied, is not long enough to switch the magnetization state. MTJ has this behavior for defects up to 600 Ω.

As described earlier, *0W1* operations no longer work. In addition, *1W1* operations become destructive for defects ranging from 610 to 640 Ω, as MTJ is heated above blocking temperature only when data 0 magnetic field is applied. Hence, $MTJ_{1,1,1}$ undergoes a nondesired *W0* operation.

Finally, for resistive-open defects greater than 650 Ω, *W0* and *W1* operations were not correctly performed. The current passing through the magnetic junction was not enough to heat the selected MTJ above its blocking temperature (150 °C). Therefore, $MTJ_{1,1,1}$ keeps its initial magnetization state during all write operations. Since df0 and df1 are global defects, they affect all MTJs that share the same bit-line branch. In Figs. 7 and 8, we show temperature profiles for *W0* and *W1* operations performed in one memory page under df1′ = 1kΩ. The resistive-open defect df1′ was placed on the second bit-line after the first MTJ in the column, thus affecting only three MTJs in the defective bit-line. We can see that $MTJ_{x,1,1}$, $MTJ_{x,2,1}$, and $MTJ_{x,3,1}$ were affected.

1) df0 Detailed Analysis: To fully characterize the impact of df0, we injected this resistive-open defect in the second bit-line of the TAS-MRAM architecture. In addition, we have performed simulations using read and read after write sequences.

Fig. 9 shows sense voltage (S) with respect to the size of df0 for *R1* and *R0* operations. The resistive-open defect df0 has a positive impact on *R0* operations as the sensing voltage decreases with defect size. In this case, all read operations return logic 0. Conversely, *R1* operations are not reliable if df0 has a resistance value in the range of 4 up to 11 kΩ

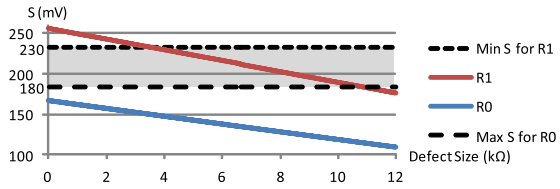

Fig. 9. *R1* and *R0* operations under df0.

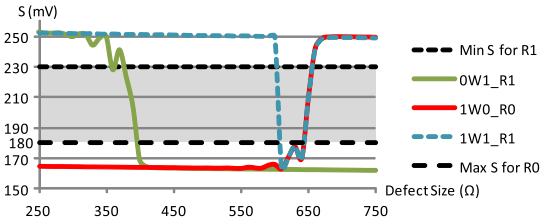

Fig. 10. Write followed by read sequences under df0.

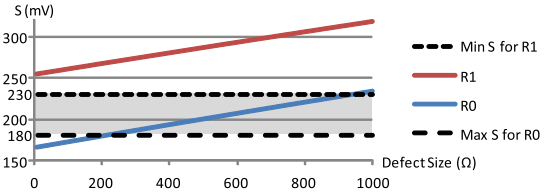

Fig. 11. *R1* and *R0* operations under df1/df2.

as the sensing voltage is in between the required levels and the output logic may be corrupted. Above 11 kΩ, the sense amplifier always returns logic 0.

The dashed area represents the minimum value of S (Min S) for a *R1* and the maximum value of S (Max S) for a *R0*, respectively. If the sensing voltage (S) is in the dashed area, the output logic data from the sense amplifier is not reliable.

Fig. 10 shows sense voltage (S) for read preceded by write operations in presence of df0. Note that all abnormal behaviors shown in Table II can be observed when performing *0W1_R1*, *1W0_R0*, and *1W1_R1* sequences.

2) df1 and df2 Detailed Analysis: These kinds of defects can represent the ill-formed contacts between magnetic layers and metallization in addition to standard ill-formed wires and contacts. To fully characterize the impact of df1 and df2 on the TAS-MRAM architecture, we have performed read operations and read after write sequences.

Fig. 11 shows the sense voltage (S) with respect to the size of df1 and df2 resistive-open defects for *R1* and *R0* operations. These defects have a positive impact on *R1* operations as the sensing voltage increases with the defect size. *R0* operations are not reliable if the defect has a resistance value in the range

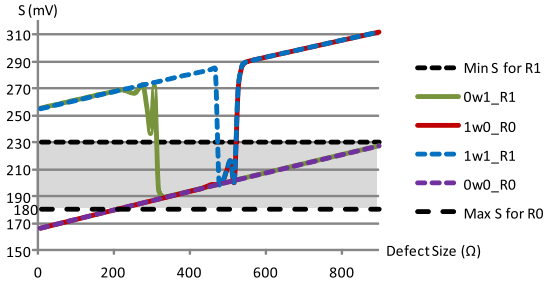

Fig. 12. Write followed by read sequences under df1/df2.

of 200–900 Ω (the sensing voltage is in between the required levels and the output logic may be corrupted). Above 900 Ω, the sense amplifier always returns logic 1.

Fig. 12 shows the sense voltage (S) for read preceded by write operations in presence of df1 and df2. Note that, for *0W1_R1* and *1W1_R1* sequences, even if the write operation preceding the read operation is not well performed, a correct logic value is returned by the sense amplifier during the read operation. Furthermore, a wrong logic value can be observed while reading even if the write operation preceding the read operation is correctly performed as seen in *1W0_R0* sequence. Finally, when a write operation that does not affect the magnetization state is performed, it is possible to observe an undesired behavior as seen in *0W0_R0* sequence.

The observed switching of the magnetization state is equivalent for df0, df1, and df2 during write operations. However, for df1 and df2, some of abnormal behaviors might not be observable as the sensing voltage (S) is in between the required levels.

B. Defects That Indirectly Impact MTJ's Heat Current

This class of defects can represent the undesired behavior on row and column decoders. Resistive-open defects df3, df4, df5, and df6 may add an extra delay while selecting or deselecting a bit-line/word-line depending on the defect size and equivalent gate capacitance of the transistor that selects the line.

In Fig. 13, we have plotted temperature profiles of a 16-bit TAS-MRAM memory page under df3 (1 MΩ) placed in the second bit-line when performing *W1* operations in the entire memory page. Similar temperature profiles are obtained for all pages of the considered MRAM array.

Since a *W1* operation is made of two write operations (write 0 followed by a write 1), two temperature peaks are observed. The *W1* operation is correctly performed on all MTJs of the first bit-line (blue curves). The *W1* on the bit-line affected by df3 (red curves) does not work because the defect slows down the bit-line selection, thus the amount of current in the heat path is decreased (single-cell faulty behavior). The following *W1* operation on the next bit-line (orange curves) is also affected even if the defect is not on this bit-line. In this case, since the deselection of the previous bit-line is delayed, the heat current is distributed among two bit-lines, and a double-cell faulty behavior may occur. Finally, there is no fault on the last *W1* operation performed on each word-line (green curves).

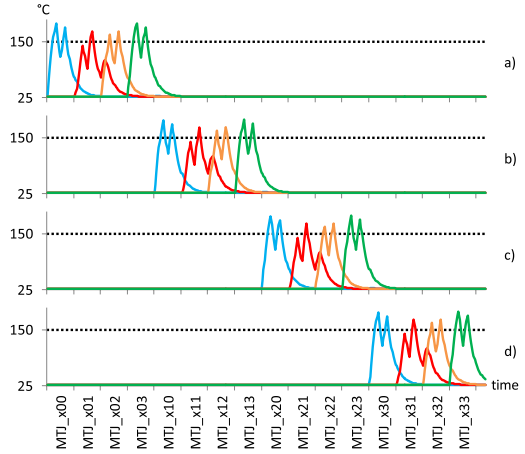

Fig. 13. 16-bit *W1* temperature profile under df3 (1 MΩ).

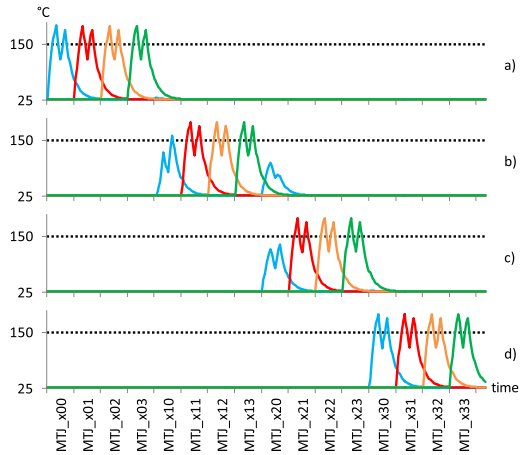

Fig. 14. 16-bit *W1* temperature profile under df5 (500 kΩ).

In Fig. 14, we have plotted temperature profiles under df5 (500 kΩ) placed in the second word-line when performing *W1* operations in one memory page. All *W1* operations on the first word-line work correctly [Fig. 14(a)].

The impact of the defect is visible when performing *W1* on the second word-line [Fig. 14(b)]. The first *W1* operation performed on the second word-line is not correctly performed since df5 has delayed MTJ's selection which did not reach its blocking temperature. The remaining *W1* operations in the same word-line are correctly performed since the word-line selection is now completed. The double-cell faulty behavior appears when changing the word-line, i.e., second to third, and current is shared between two MTJs for a while [blue curves of Fig. 14(b) and (c)]. Finally, all *W1* operations on the last word-line work correctly [Fig. 14(d)].

The remaining defects that impact indirectly the heat current, local (df5 and df6) and distributed (df3′, df5′, and df5″), have the same single-cell and double-cell faulty behaviors, with a difference in defect size range and affected MTJs.

1) df3 Detailed Analysis: Single-cell faulty behavior may happen when selecting MTJs located in defective bit-lines and double-cell faulty behavior may occur when an operation is

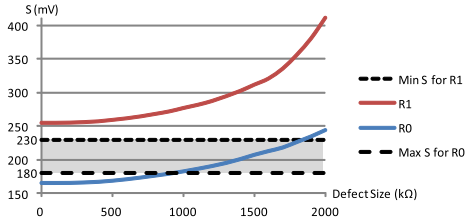

Fig. 15. *R1* and *R0* operations under df3.

TABLE III
$MTJ_{1,1,1}$ CHARACTERISTICS UNDER df3 FOR SINGLE-CELL WRITE OPERATIONS

Op.	Defect size (kΩ)	$MTJ_{1,1,1}$ parameters				
		V (mV)	I (uA)	R (kΩ)	T (°C)	M
0W1	140	715.61 871.31	531.17 555.29	1.34 1.56	125.76 167.42	-1
	150	707.75 787.04	522.87 597.65	1.35 1.31	121.89 165.79	+1
1W1	90	856.73 885.23	508.28 556.55	1.68 1.59	**149.98** 179.39	-1
	270	717.42 867.36	368.57 516.47	1.94 1.67	90.41 **150.09**	-1
1W0	30	752.56 -	599.36 -	1.25 -	181.90 -	+1
	80	860.28 -	515.32 -	1.66 -	155.29 -	-1

performed on MTJs located in nondefective bit-lines while defective bit-line remains partially selected.

To fully characterize the impact of df3, we have injected df3 in the second bit-line of the TAS-MRAM architecture. In addition, we have performed simulations using combinations of read and write operations in which the first operation is performed on $MTJ_{1,1,1}$ and second on $MTJ_{1,1,3}$ or $MTJ_{1,3,3}$. In the following subsections, we first analyze single-cell faulty behavior and then double-cell faulty behavior.

a) Single-cell analysis: Fig. 15 shows the sensing voltage (S) with respect to the size of df3 resistive-open defect for *R1* and *R0* operations. *R1* operations on $MTJ_{1,1,1}$ are affected positively by df3 as the sensing voltage increases with the defect size. In this case, all read operations return logic 1. Conversely, *R0* operations are not reliable if df3 has a resistance value in the range of 1 up to 1.9 MΩ. Above 1.9 MΩ the sense amplifier always returns logic 1 even if the $MTJ_{1,1,1}$ contains logic 0.

Table III summarizes simulated characteristics of $MTJ_{1,1,1}$ under single-cell write operations in presence of df3. The first column shows the write operation and the second one, lists the simulated defect sizes. The next five columns provide all MTJ's parameters.

As shown in Table III, both transition sequences (*1W0* and *0W1*) are affected by df3. The *1W0* operation shows an abnormal behavior for a defect size higher than 80 kΩ while the *0W1* sequence stops working when df3 is higher than 150 kΩ.

There is no impact of df3 on *1W1* operations as the one observed on df0, df1, and df2. In this case, $MTJ_{1,1,1}$ is heated above its blocking temperature only while applying data 1 magnetic field for defect sizes ranging from 90 to 270 kΩ. Above 270 kΩ, $MTJ_{1,1,1}$ keeps its initial magnetic state.

Finally, there is no impact of df3 on the *0W0* operations as $MTJ_{1,1,1}$ exhibits the correct magnetization state after the operation no matter the defect size.

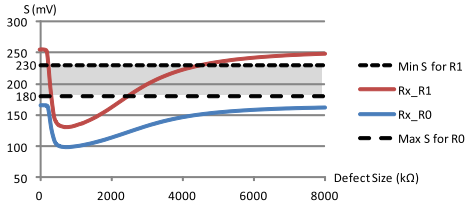

Fig. 16. Read after read double-cell sequences under df3.

TABLE IV
$MTJ_{1,1,1}$ CHARACTERISTICS UNDER df3 FOR *xWy_0W1* SEQUENCE

Sequence	Defect size (kΩ)	$MTJ_{1,1,1}$ parameters				
		V (mV)	I (uA)	R (kΩ)	T (°C)	M
xWy_0W1	100	750.99 862.87	580.77 539.32	1.29 1.60	157.78 170.25	-1
	200	678.63 744.08	510.39 572.94	1.33 1.30	136.37 **154.38**	+1
	2700	696.57 706.10	542.18 544.83	1.28 1.30	162.33 **156.06**	+1
	2800	697.58 706.88	543.40 545.76	1.28 1.30	162.91 156.51	-1

b) Double-cell sequence analysis: Fig. 16 shows sensing voltage (S) of $MTJ_{1,1,3}$ under df3 for read after read sequences in which the first operation is performed on $MTJ_{1,1,1}$, and the second one is performed on $MTJ_{1,1,3}$. The first operation exhibits the previously described single-cell faulty behavior. For read after read sequences, the presence of df3 decreases the sensing voltage (S) on $MTJ_{1,1,3}$. This happens because the reading path of $MTJ_{1,1,1}$ is still open and read current is shared between two MTJs.

The impact of df3 on the second operation of sequences *Rx_R0* is positive. No abnormal behavior is observed and *R0* operation always returns logic 0. However, the second operation of sequences *Rx_R1* are affected by df3 depending on the defect size. The *R1* operation returns logic 0 when df3 is in the range of 400 kΩ up to 2 MΩ and is not reliable from 200 to 400 kΩ and 2 to 4 MΩ as the sensing voltage (S) is in between the required.

Note that df3 presents the same faulty behavior for read after read sequences in which the first operation is performed on $MTJ_{1,1,1}$ and the second one is performed on $MTJ_{1,3,3}$. In this case, current is shared between $MTJ_{1,3,1}$ and $MTJ_{1,3,3}$ as they are on the same bit-line.

Table IV summarizes simulated characteristics of $MTJ_{1,1,3}$ under *xWy_0W1* sequence in presence of df3 in which the first operation is performed on $MTJ_{1,1,1}$, and second on $MTJ_{1,1,3}$. $MTJ_{1,1,3}$ is barely heated above its blocking temperature for a df3 of 200 kΩ and 2.7 MΩ keeping its initial magnetization state. In this defect size range, $MTJ_{1,1,3}$ is never heated above

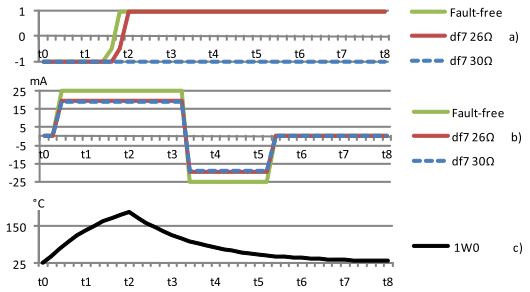

Fig. 17. MTJ parameters for *1W0* without defect and under df7.

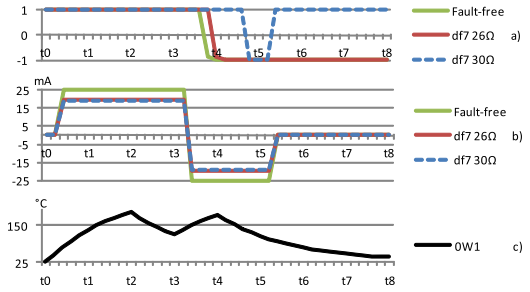

Fig. 18. MTJ parameters for *0W1* without defect and under df7.

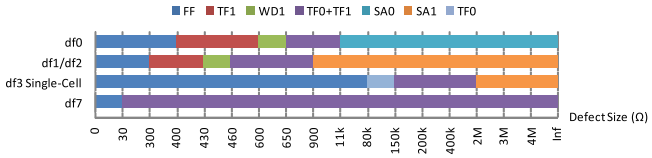

Fig. 19. Fault modeling of resistive-open defects with respect to defect size.

its blocking temperature. Note that, both transition operations performed on $MTJ_{1,1,3}$ (*1W0* and *0W1*) have the same behavior but with opposite magnetization states. In addition, the remaining write after write sequences are not affected by df3.

C. Defects That Impact Field-Line Current

We already studied defects affecting heat current in the considered TAS-MRAM architecture. This section shows what happens when defects are injected in the field-line. Note that the field-line driver should provide ∼25 mA considering all field-line parasitics. Figs. 17 and 18 show how MTJs parameters—magnetization state switching, applied field-line current, and MTJ's temperature profile—change over time without defect (green curve) and under df7 (red and blue curves) for *1W0* and *0W1* operations, respectively.

The amount of magnetic field applied to the MTJ is reduced in the presence of df7. For this reason, both operations are delayed when the defect size is below 30 Ω. For defects greater than 30 Ω both write operations are not performed correctly. Read operations and heat current are not affected by this class of defects.

Field-line resistivity depends on several factors as its cross section and length. Changing field-line characteristics only shifts defect regions while keeping same faulty behaviors.

D. Fault Modeling

Based on electrical simulations, we associate a set of fault models to the observed faulty behaviors. Fig. 19 presents the single-cell fault modeling with respect to the defect size. Single-cell TAS-MRAM functional fault modles (FFMs) according to the literature on SRAMs [8].

1) SA1 ⇒*R0* operations that return logic 1.
2) SA0 ⇒*R1* operations that return logic 0.
3) TF1 ⇒*0W1* transition operation followed by read operation that returns logic 1.
4) TF0 ⇒*1W0* transition operation followed by read operation that returns logic 0.
5) WD1 ⇒*1W1* operation followed by read operation that returns logic 0.

In addition, double-cell TAS-MRAM FFMs for all failing transition sequences in double-cell context are SCFs (all types of SCFs).

Note that, the defect size range is strictly related to technology node, memory architecture and MTJ fabrication process parameters. Even if these parameters change, the expected behaviors are equivalent.

V. Conclusion

In this paper, we analyzed resistive-open defects that may impact the functionality of TAS-MRAMs. Electrical simulations are performed in the presence of seven resistive-open defects and their impact on read and write sequences are evaluated. In addition, we demonstrated that single-cell and double-cell FFMs can model the resulting faulty behaviors.

This paper provides insights into several kinds of MRAM resistive-open defects and their behaviors. As future works, we plan to use these analysis results to guide the test phase by providing effective test algorithm targeting faults related to actual defects that may affect TAS-MRAMs and extend resistive-open defect analysis to more recent MRAM technologies such as STT-MRAMs.

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Is triple modular redundancy suitable for yield improvement?

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Abstract: With the technology entering the nanodimension, manufacturing processes are less and less reliable, thus drastically impacting the yield. A possible solution to alleviate this problem in the future could consist in using fault-tolerant architectures to tolerate manufacturing defects. In this paper, we consider the classical triple modular redundancy (TMR) as fault-tolerant architecture for yield improvement purposes. Firstly, we compute a set of conditions to be satisfied in order to make use of TMR architectures interesting for yield improvement. Then, we prove that these conditions depend on the testability of the TMR architecture. Thus, we investigate test requirements for TMR architectures and we propose a solution for generating test patterns for this type of architecture. Finally, we propose a new way of implementing the TMR architecture in order to achieve more benefits for yield improvement purpose. This is done by partitioning the logic part and then adding voters between sub-modules. Experimental results are provided on ISCAS'85 and ITC'99 benchmark circuits to demonstrate the efficiency of the proposed approach in terms of yield improvement.

1 Introduction

Deep submicron technologies allow hundreds of millions of transistors to be integrated on the same chip. However, the yield of such large chips decreases because of gross imperfections caused by manufacturing defects or process deviations. Even with a well-controlled manufacturing process, it becomes more and more difficult to guarantee a chip without any defect. Consequently, the design and test of an electronic system benefiting from technological advances will be even more challenging in the coming years [2].

To increase the yield for future very large scale integration (VLSI) systems, fault-tolerant architectures have been proposed as a potential solution [3]. Fault-tolerant architectures are commonly used to tolerate on-line faults, that is, faults that appear during the normal functioning of the system irrespective of their transient or permanent nature [4]. In the near future, fault-tolerant architectures could also be used to tolerate permanent defects because of an imperfect manufacturing process.

Fault-tolerant architectures use redundancies. Redundancy is the property of having more resources than needed to perform a given function, which are therefore used to tolerate defects. Fault tolerance architectures are generally classified depending on the type of redundant resources. Basically four types of redundancy are considered: hardware, software, information and temporal [5].

This paper is an extended version of a previously published paper. In [1] we have proposed a preliminary study on using TMR architectures for yield improvement. This paper has provided a theoretical analysis of TMR architectures where voters are omitted, an automatic test pattern generator (ATPG) procedure to evaluate the interest of manufacturing TMR architectures and finally an improvement of the TMR fault tolerance by circuit partitioning. Main contributions of this paper with respect to [1] are as follows:
→ A complete analysis of the TMR architecture including voters in terms of additional area overhead. Moreover, voters are considered to be possibly defective.
→ A formulation of the updated conditions making TMR suitable for yield improvement.
→ A new comparative study between TMR architectures having voters that can be defective (with the same defect density than the logic part) and TMR architectures having voters considered as fault free (i.e. voters manufactured with robust design techniques).

Hardware redundancy consists in modifying the design by adding additional hardware. For example, instead of having a single processor, three processors are embedded to perform the same operation. The failure of one processor is tolerated thanks to a voter that chooses the majority outputs. This is the basic principle of a triple modular redundancy (TMR) architecture [5]. In software redundancy, error detection and recovery are based on replicating application processes on a single or multiple computers [6]. In information redundancy, additional data are used. For example, the use of error-correcting codes requires extra bits that need to be added to the original data bits [5]. Depending on the dimension of extra data and the used code, an error can be either detected or corrected. This kind of redundancy is particularly used in signal transmission technologies. Nevertheless, the use of error-correcting codes in logic cores has non-negligible impact on the design and requires a high area overhead. Temporal redundancy consists in forcing the system (or a sub-system) to repeat a given operation and then compare the results with those of the previous operation. Such a redundancy is able to tolerate transient or intermittent errors but not permanent errors thus making this solution not suitable for our study [7].

In this paper, we consider hardware redundancy for achieving yield ramp-up benefits. As a case study, we consider the well-known TMR fault-tolerant architecture in order to tolerate manufacturing defects while increasing the yield [1]. We first determine the set of conditions to be satisfied in order to successfully resort to TMR to ramp-up the yield. Then, we propose a test pattern generation solution for TMR architectures in order to evaluate the condition that makes such architectures suitable to yield improvement. The first set of results show that the combinational depth of circuits has a strong impact on the effectiveness of the TMR architecture. We therefore propose to improve the tolerance of TMR architectures by reducing the combinational depth of its internal modules. This is done by partitioning each module and adding voters between partitions. For this purpose we use a hypergraph representation of TMR modules and a tool to partition the graph as presented in Section 4.1. Results show that this improvement of the TMR architecture is very fruitful to improve its tolerance capability at the price of a low silicon area overhead (less than 5% for the biggest benchmark circuits).

The remainder of the paper is organised as follows. In Section 2, we present the TMR architecture and we analyse its capability to tolerate manufacturing defects. Section 3 details the test strategy targeting the TMR architecture and presents a first set of experimental results on ISCAS'85 and ITC'99 benchmark circuits. Section 4 presents the improvement of the TMR architecture to make it able to tolerate more defects. Finally, concluding remarks and future works are given in Section 5.

2 Yield analysis of TMR architectures

2.1 TMR principle

A number of hardware fault-tolerant architectures have been proposed in the literature [8]. Generally, the degree of fault tolerance is defined as the maximum number of faults that can be tolerated in the system [9]. The classical hardware redundancy architecture is the NMR (N Modular Redundancy). An NMR structure is a fault-tolerant architecture based on N modules performing the same function. The outputs of these modules are compared by using a majority voter. In general, this architecture can tolerate at least $(N-1)/2$ defects.

The case of $N=3$ is called TMR and has been widely studied and used in practical applications [5]. The inputs to three identical modules are tied together, thus receiving the same data, and their outputs feed a majority Voter (V) circuit as shown in Fig. 1. As a result, the TMR architecture significantly reduces the error probability at the primary outputs of the system. The erroneous value propagated by a defective module can be masked thanks to the presence of the two other fault-free modules. In TMR architectures, the voter is the weak point. If a fault appears in the voter, the TMR structure can be possibly faulty. To avoid this type of problem, the voter can be realised in software or with more robust design techniques [10].

2.2 TMR limitations

It is known that for nano-scale bulk-complementary metal oxide semiconductor (CMOS) VLSI circuits, systematic defects caused by micro-lithography-related printability issues significantly dominate the random defects caused primarily by contamination of foreign particles during fabrication process. In this context, improvement of fault tolerance or design robustness is primarily concerned with relative placement of polygons in a given mask layer so that the overall quality of the resist profile sees the improvement. If a given mask with printability problems is simply used three times to fabricate a TMR architecture, same systematic defects are likely to creep in all three copies of the same circuit causing a poor yield for the overall TMR architecture. Consequently, electronic systems

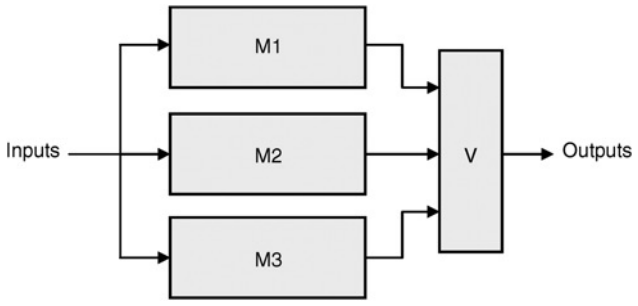

Figure 1 *TMR principle*

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using TMR architectures are built with three different circuits. Circuits can be obtained by modifying options and libraries of the synthesis tool and/or by changing options of the place and route tool. The objective is to obtain the same functionality for each circuit but with a different layout and thus a lower sensibility to systematic defects.

In this paper, we consider for simplicity that the three circuits have the same structure. As shown later in the paper, this assumption makes the ATPG procedure we have developed easier to implement. However, in order to deal with systematic defects, our study can be easily extended and is still valid if the TMR is built with three different structures of the same functional logic block.

2.3 How many defects can be tolerated?

Basically, a TMR architecture can tolerate at least one defect. Under certain conditions, however, more than one defect can be tolerated. To be not tolerated, two defects must be located in two different modules and propagate an error towards identical outputs on each module. Let P be the input pattern, Ω_i be the set of erroneous outputs in module i ($i = 1, 2, 3$) because of the first defect when P is applied and Ω_j be the set of erroneous outputs in module j ($j = 1, 2, 3$) because of the second defect when P is applied. Under these constraints, defect tolerance is formalised as follows:

- If $i = j$, defects are in the same module and, consequently, are tolerated.
- If $i \neq j$ and $\Omega_i \cap \Omega_j = \emptyset$, defects are tolerated.
- If $i \neq j$ and $\Omega_i \cap \Omega_j \neq \emptyset$, defects are not tolerated.

In Fig. 2, two examples are shown with the same pattern P feeding the three modules. The voter has been omitted. Each defect is modelled as a stuck-at fault (f_1 and f_2, respectively).

In the case of Fig. 2*a*, f_1 is propagated towards $O1$ in the first module and f_2 is propagated towards $O2$ in the second module. The majority voter receives two correct values and one wrong value. The outputs of the TMR are therefore correct and faults f_1 and f_2 are tolerated. In the case of Fig. 2*b*, f_1 is propagated towards $O1$ and $O2$ whereas f_2 is propagated towards $O2$. The voter receives one wrong value for $O1$ and two wrong values for $O2$. So, the value on the second output of the TMR is faulty. Faults f_1 and f_2 are not tolerated.

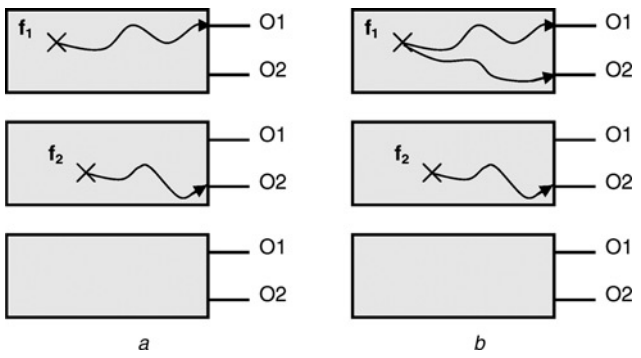


Figure 2 *Two stuck-at faults*
a Tolerated
b Not tolerated

Consequently, two stuck-at faults are tolerated when there is no pattern able to propagate errors coming from the two faults in different modules towards identical outputs in each module. In the case of more than two defects, multiple defects can be handled by considering all the possible defect couples between them.

2.4 Yield improvement with TMR architectures

In this sub-section, we investigate the value of producing the TMR version of a circuit, instead of its single version, in order to tolerate manufacturing defects and consequently improve the yield as presented in [11]. We therefore analyse the conditions that have to be fulfilled to achieve benefits in implementing such a TMR architecture instead of using a simple non-tolerant architecture.

Let A_C be the area of the logic circuit and A_V the area of voters. The resulting area overhead of the TMR implementation is

$$A_O = \frac{3A_C + A_V}{A_C} = 3 + \frac{A_V}{A_C} \quad (1)$$

Thus, if we triplicate a circuit to implement a TMR architecture on a given silicon area, we can have N TMR circuits having a yield equal to Y_{TMR} ($Y_{TMR} \times N$ circuits having a correct behaviour) or $A_O \times N$ circuits (without redundancy) having a yield equal to Y_C ($Y_C \times A_O \times N$ fault-free circuits). Then, for a given silicon area, a TMR architecture is worthwhile only if

$$\frac{Y_{TMR}}{A_O} > Y_C \quad (2)$$

As $Y_{TMR} \leq 1$, using a TMR architecture for yield improvement is interesting only if

$$Y_C \leq \frac{1}{A_O} \quad (3)$$

First of all, because of (3), it is important to notice that a TMR architecture is worthwhile only if $Y_C \leq 1/A_O$, that is, when a low manufacturing yield is expected because of the use of aggressive nanotechnologies.

Let us now compute Y_{TMR} and Y_C by using the Poisson distribution. It would not be completely accurate to use the

Poisson distribution for large circuits because of clustering effects on defects [12, 13]. But, for a first and rough evaluation this is reasonable. In our case, the Poisson distribution is a discrete probability distribution that defines the probability that a number of manufacturing defects occur in a fixed area if these defects occur with a known probability.

Let X be the number of manufacturing defects. Let λ be the average number of expected defects for a given silicon area. Then, $\lambda = n \times p$ with n being the number of logic gates (or transistors) and p the average defect rate of a gate (or a transistor). Let $P\{X = k\}$ be the probability that the circuit has k manufacturing defects. If n is high and p is low, the binomial distribution becomes the Poisson distribution:

$$P\{X = k\} = e^{-\lambda} \times \frac{\lambda^k}{k!} \tag{4}$$

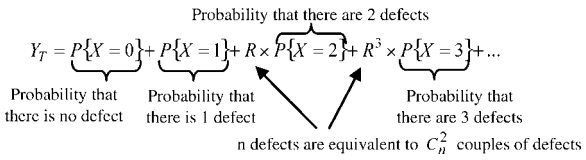
In the circuit without redundancy, the presence of a fault makes the entire circuit faulty. So, Y_C is the probability that there is no defect inside the circuit

$$Y_C = \underbrace{P\{X = 0\}}_{\text{Probability that there is no defect}} = e^{-\lambda_C} \times \frac{(\lambda_C)^0}{0!} = e^{-\lambda_C} \tag{5}$$

The computation of Y_{TMR} is more complex as it depends on (i) the ability of the triplication to tolerate manufacturing defects and (ii) the yield of the voter. Consequently, Y_{TMR} can be expressed as follows

$$Y_{TMR} = Y_T \times Y_V \tag{6}$$

where Y_T is the yield of the triplication without considering the voter and Y_V is the yield of the voter. Let us first compute Y_T as follows



$$Y_T = e^{-\lambda_T} \times \left(1 + \lambda_T + R\frac{(\lambda_T)^2}{2!} + R^3\frac{(\lambda_T)^3}{3!} + \cdots\right) \tag{7}$$

with R being the probability that two defects are tolerated. In fact, as shown in Section 2.2, two defects are tolerated if they propagate their effect towards the same module outputs. Otherwise, the effect of the defects can be view on voter outputs and are thus not tolerated. Consequently, this parameter reflects the tolerance of the resulting TMR architecture.

There are three times more gates (or transistors) into a TMR architecture than into a non-redundant circuit. So, by substituting λ_T by $3\lambda_C$ we obtain

$$Y_T = e^{-3\lambda_C} \times \left(1 + 3\lambda_C + \sum_{i=2}^{\infty} R^{C_i^2} \times \frac{(3\lambda_C)^i}{i!}\right) \tag{8}$$

On the other hand, Y_V is the probability that there is no defect inside the voter

$$Y_V = \underbrace{P\{X = 0\}}_{\text{Probability that there is no defect}} = e^{-\lambda_V} \times \frac{(\lambda_V)^0}{0!} = e^{-\lambda_V} \tag{9}$$

and, by substituting λ_V by $\lambda_C \times A_V/A_C$ we obtain

$$Y_V = e^{-\lambda_C(A_V/A_C)} \tag{10}$$

Consequently, Y_{TMR} becomes

$$Y_{TMR} = e^{-(3+A_V/A_C)\lambda_C} \times \left(1 + 3\lambda_C + \sum_{i=2}^{\infty} R^{C_i^2} \times \frac{(3\lambda_C)^i}{i!}\right) \tag{11}$$

and with $Y_C = e^{-\lambda_C} \Rightarrow \lambda_C = -\ln Y_C$ and $A_O = 3 + A_V/A_C$

$$Y_{TMR} = e^{A_O \ln Y_C} \times \left(1 - 3\ln Y_C + \sum_{i=2}^{\infty} R^{C_i^2} \times \frac{(-3\ln Y_C)^i}{i!}\right) \tag{12}$$

To summarise, implementing a TMR architecture for a given circuit can improve the yield if two conditions are satisfied. First, $Y_C \leq 1/A_O$; this condition is related to the area overhead needed to implement the TMR architecture. Second, $Y_{TMR} \geq A_O \times Y_C$ with Y_{TMR} depending on Y_C, A_O and R as shown in (12). To satisfy these conditions, we have to analyse the impact of A_O on the R parameter. Fig. 3 gives R_{min} as a function of A_O with R_{min} being the minimum value of R satisfying the previous conditions. For example, if the area overhead (A_O) is about 3.27, then the probability that two defects are tolerated (R) has to be

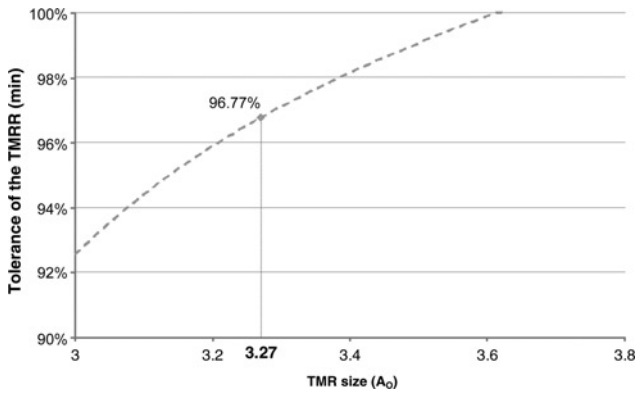


Figure 3 *Minimum value of the tolerance of the TMR architecture (R_{min}) related to the area overhead (A_O)*

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higher than 96.77% to successfully resort to a TMR architecture to ramp-up the yield.

From Fig. 3, two main conclusions can be drawn. First, the R probability increases with the area overhead. Second, when the area overhead becomes higher than 3.6, there is no interest in implementing a TMR architecture. In that case, even if the TMR architecture is fully tolerant ($R = 100\%$), Y_{TMR} remains always lower than $A_O \times Y_C$.

Consequently, a question is still open concerning the value of R: How can we determine the percentage of tolerated couple of defects for a given TMR architecture? As shown in the example of Fig. 2, tolerated defects lead to a fault-free value at the output of the TMR architecture. Consequently, the problem of determining the percentage of tolerated couple of defects (R) is equivalent to determining the percentage of untestable couple of defects. In the next section, we investigate test issues related to TMR architectures in order to determine this percentage.

3 Test of TMR architectures

3.1 Test specificities

Testing a TMR architecture depends on its final use. Classically, the goal is to tolerate potential on-line defects (permanent and/or transient). Every module has to be fault free at the end of the manufacturing process. Owing to the intrinsic impossibility to test single stuck-at fault, the architecture has to be modified during the test [4]. In this modified architecture, each module is individually tested. Redundancy is removed and each single stuck-at fault becomes testable.

In the proposed way of use, the goal is to increase the yield by tolerating permanent defects because of an imperfect manufacturing process. Thus, we have to verify if the presence of defects in the TMR architecture does not change its functioning. In this case, the test consists in testing globally the TMR architecture in order to determine what are the couples of defects which are tolerated or not (determination of the R probability). The architecture is therefore not modified for test purpose. Lastly, we remember that the TMR basically tolerates one single defect and optionally two or more defects as discussed previously. For example, if several defects are located in the same module, the TMR still works properly.

To summarise, in the first approach, the question to be answered during the test of the TMR is: 'Are there one or more manufacturing defects in each module?' In the second approach, the question becomes: 'Is the circuit still working despite the presence of one or more manufacturing defects?'

The fault model widely used in structural testing to detect a manufacturing defect is the single stuck-at fault model. Since the single stuck-at fault is by definition tolerated (untestable) in a TMR architecture (in its internal triplicated modules), a different fault model has to be considered. This fault model must be testable on primary outputs of the TMR architecture, and also be representative of actual manufacturing defects. We have seen in Fig. 2 that a couple of stuck-at faults can be observed (not tolerated) on primary outputs of the TMR and also can be testable. In the following, we refer to a couple of stuck-at fault as fault pair [3]. If there are two stuck-at faults simultaneously in a TMR architecture, these two faults are named a fault pair. If there are more than two stuck-at faults, these multiple stuck-at faults can be gathered in fault pairs (under the assumption that no masking effect occurs between faults). For example, three stuck-at faults (f_1, f_2, and f_3) are equivalent to three fault pairs $\{f_1, f_2\}$, $\{f_1, f_3\}$ and $\{f_2, f_3\}$. In general, n stuck-at faults are equivalent to C_n^2 fault pairs. To be testable and thus not tolerated, the two faults of a fault pair must affect two different modules and propagate towards common module outputs as shown in Fig. 2.

Let us now compute the size of the fault list considering the fault pair model. The whole number of stuck-at faults in the three modules is $3n$ with n being the number of single stuck-at faults in one module. As $\{f_1, f_2\} = \{f_2, f_1\}$, the total number of fault pairs is

$$Nb_{\text{fault pair}} = C_{3n}^2 = \frac{3n!}{(3n-2)! \times 2!} = \frac{9n^2 - 3n}{2} \quad (13)$$

3.2 ATPG procedure

In order to determine the percentage of untestable (tolerated) fault pairs, we have to generate test patterns able to detect all testable fault pairs. The remaining fault pairs are untestable. Since the number of fault pairs is quadratic to n, the use of a classical ATPG to detect the entire fault pair set will be unfeasible because of huge CPU time. Since the goal of this work was not to develop an ATPG for fault pairs, we have adapted an ATPG tool targeting single stuck-at faults to make it able to test fault pairs.

Considering that a fault pair is composed of two stuck-at faults $\{f_1, f_2\}$, the proposed approach consist in injecting a permanent fault in one module of the TMR architecture (f_1). This is simply done by modifying the 'netlist'. Then, an ATPG is run to test all stuck-at faults in the presence of the permanent one. This process is repeated until we have injected all stuck-at faults in one module.

The simplicity of this approach is obtained at the cost of higher simulation time since n full ATPG runs are needed. To reduce this drawback, we have first minimised the fault pair list as follows:

- When there is only one faulty module, the faulty outputs of this module are masked by the voter. Thus, all fault pairs that impact only one module are structurally

untestable. These fault pairs can be removed from the ATPG fault list.

- Symmetries of the TMR architectures are used to reduce the fault pair list. As each module inputs are tied together during the test, fault pairs are equivalent when their two stuck-at faults have the same location in two different modules. Therefore, equivalent fault pairs are removed from the ATPG fault list.

With the help of these reductions, it can be demonstrated that the size of the fault pair list becomes

$$\frac{n^2 + n}{2} \tag{14}$$

Secondly to further reduce the ATPG fault list, it is possible to determine by a simple preprocessing step fault pairs that are structurally untestable. Let us consider the fault pair $\{f_1, f_2\}$ and their output cones (list of outputs where the fault effect may be propagated) $\{\Phi_1, \Phi_2\}$. Owing to the presence of the voter, if $\Phi_1 \cap \Phi_2 = \emptyset$, the fault pair $\{f_1, f_2\}$ is structurally untestable and therefore, can be removed from the ATPG fault list. In practical cases, the number of structurally untestable fault pairs is quite large leading to a huge improvement of the overall ATPG performance. For example, the percentage of structurally untestable fault pairs is 82.86% for circuit c7552, 76.16% for circuit b05 and 88.01% for circuit b13.

3.3 Results

For the analysis, both ISCAS'85 and ITC'99 (combinational part only) benchmark circuits are used to implement TMR architectures by simply cloning each circuit three times. The results are reported in Table 1. The first column lists the circuit name. Second and third columns show the

Table 1 Tolerance of TMR architectures for ISCAS'85 and ITC'99 benchmarks

Circuit	# SAF	# FP	# ATPG FP	A_O	R_{min} (%)	Overall results		
						R (%)	FC (%)	# patterns
C432	392	691k	75.0k	3.10	94.41	41.00	33.30	912
C499	486	1.06M	95.0k	3.39	98.04	51.72	35.74	2450
C880	886	3.53M	133k	3.18	95.62	78.41	19.86	1896
c1908	1812	14.8M	1.30M	3.08	94.08	56.42	36.43	3852
c2670	2852	36.6M	1.87M	3.33	97.43	75.95	17.51	4987
c3540	3438	53.2M	4.91M	3.04	93.36	54.09	23.75	1756
c5315	4970	111M	3.44M	3.16	95.34	93.20	3.75	642
c6288	6250	176M	18.2M	3.03	93.17	38.02	54.79	4532
c7552	7438	249M	7.40M	3.09	94.25	84.92	11.71	8745
b01	127	72.4k	6.76k	3.38	97.94	79.35	20.65	31
b02	64	18.3k	1.57k	3.47	98.79	86.36	13.64	12
b03	382	656k	291k	3.57	99.65	87.93	12.06	114
b04	1477	9.81M	535k	3.32	97.33	84.32	12.70	3390
b05	2553	29.3M	1.17M	3.16	95.34	88.65	8.98	4699
b06	155	108k	7.73k	3.68	NA	87.51	12.49	16
b07	1120	5.64M	399k	3.38	97.94	81.91	16.00	1635
b08	439	867k	59.1k	3.38	97.94	89.09	10.78	132
b09	417	782k	57.3k	3.45	98.61	83.07	16.93	211
b10	468	985k	63.5k	3.31	97.22	89.39	10.60	149
b11	1308	7.70M	703k	3.19	95.76	74.50	21.16	1551
b12	2777	34.7M	857k	3.30	97.11	95.45	4.09	1274
b13	835	3.14M	59.6k	3.49	98.97	96.94	3.06	167

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number of stuck-at faults in one module (# SAF) and the number of equivalent fault pairs in the TMR structure (# FP), respectively. The number of stuck-at faults in one module of the TMR structure varies from 64 (b02) to 7438 (c7552). Consequently, the total number of fault pairs can be very high (over 249 million for c7552). The fourth column shows the number of fault pairs in the ATPG fault list (# ATPG FP). The fifth column (A_O) shows the area overhead required to implement the TMR architecture (i.e. circuit triplication and voters). The next column (R_{min}) gives the minimum value of R (percentage of untestable fault pairs) under which it is beneficial to use a TMR architecture. In that column, NA (not applicable) means that A_O is higher than 3.6 (see Fig. 3) making TMR architecture not suitable for yield ramp-up. The last columns provide the ATPG results: the tolerance of the TMR architecture (R), the fault coverage achieved with the ATPG tool (FC) and the test length (# patterns). The fault efficiency of the ATPG is not shown but can be easily computed as $R + FC$.

With the help of these APTG results, we are now able to determine whether implementing a TMR architecture will improve the yield. This is simply done by either comparing columns R_{min} and R in Table 1 or looking in Fig. 4, which represent graphically R as a function of A_O for each considered benchmark circuit. It appears that no circuit has the condition $R > R_{min}$ satisfied. Implementing a TMR architecture will improve the yield if crosses are above the dotted line, which gives R_{min} depending on A_O. From these results, it appears we have to find a solution to improve the tolerance of the TMR architecture.

4 Improvement of the TMR architecture

To improve the tolerance of the TMR architecture, we have to increase the percentage of untestable fault pairs. From the results presented in Table 1, we can notice that the R probability is higher for ITC'99 benchmark circuits than for ISCAS'85 benchmark circuits. The smaller combinational depth of ITC'99 circuits, as shown in Table 2, could explain this difference. Actually, it appears that the lower the combinational depth, the greater is the probability to have an empty intersection of logic cones, and hence a higher tolerance capability (R probability) of the TMR architecture. Then, in the following sub-section, we propose to modify the basic TMR architecture by partitioning its module in order to decrease their combinational depth.

4.1 Circuit partitioning

In order to reduce the combinational depth and thus increase the tolerance of the TMR architecture, each circuit is partitioned into two or three equivalent blocks. As shown in Fig. 5, majority voters are added on circuit edge cut. An important feature of partitioning the circuit is that the tolerance of fault pairs increases when the number of partitions increases as well. For example, in the case of double TMR (Fig. 5*b*), circuits (modules) are divided into two equivalent blocks. Each block operates independently and a manufacturing defect in the first block has no impact on the second block. In a basic TMR architecture, the percentage of untestable fault pairs is always greater than 33.33% as two stuck-at faults in the same module are untestable. In a double TMR architecture, if we consider that the first fault f_1 impacts M1′, then the fault pair $\{f_1, f_2\}$ can be detected (not tolerated) if and only if f_2 is in M2′ or M3′. Conversely, if f_2 is in M1′, M1″, M2″ or M3″, the fault pair is necessarily tolerated because of the presence of the voters. Therefore, the percentage of tolerated fault pairs in a double TMR architecture is always greater than 66.66%.

In the case of a triple TMR architecture (see Fig. 5*c*), circuits (modules) are divided into three equivalent blocks. If f_1 impacts M1′, the fault pair $\{f_1, f_2\}$ is necessarily

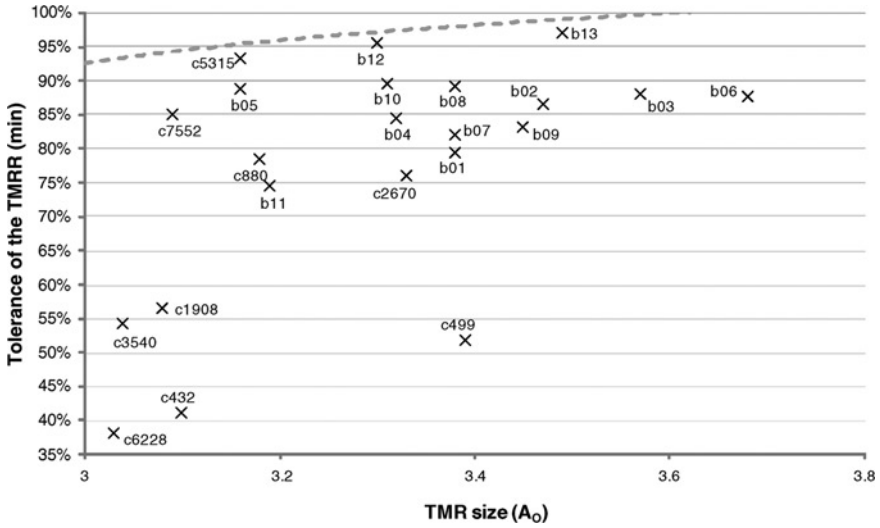

Figure 4 *Tolerance of TMR architectures (R) for ISCAS'85 and ITC'99 benchmarks*

Table 2 Combinational depth of ISCAS'85 and ITC'99 benchmark circuits

Circuits	Combinational depth
c432	17
c499	11
c880	24
c1908	40
c2670	32
c3540	47
c5315	49
c6288	124
c7552	43
b01	7
b02	7
b03	11
b04	26
b05	52
b06	8
b07	32
b08	18
b09	11
b10	12
b11	35
b12	15
b13	12

tolerated if f_2 impacts M1′, M1″, M2″, M3″, M1‴, M2‴ and M3‴. Consequently, the percentage of tolerated fault pairs is always higher than 77.77%. More formally, if circuits are partitioned into k blocks, then the percentage of tolerated fault pairs is always higher than

$$100 \times \frac{3k-2}{3k} \tag{15}$$

The circuit partitioning consists of three steps. First, we transform the circuit into a hypergraph. A hypergraph is a generalisation of a graph, where the set of edges is replaced by a set of hyperedges. A hyperedge extends the notion of an edge by allowing more than two vertices to be connected together. Formally, a hypergraph $H = (V, Eh)$ is defined as a set of vertices V and a set of hyperedges Eh, where each hyperedge is a subset of the vertex set V, and the size of an hyperedge is the cardinality of this subset. Hypergraphs can be used to naturally represent a gate-level VLSI circuit. The vertices of the hypergraph can be used to represent the gates of the circuit, and the hyperedges can be used to represent the lines connecting these gates. In a second step, we make the hypergraph partitioning. The proposed technique of circuit partitioning for TMR architecture improvement utilises sh-METIS, a multilevel hypergraph partitioning algorithm based upon the multilevel paradigm [14]. The quality of the partitioning produced by sh-METIS in terms of cut size (the size of the hyperedge cut is representative of the area overhead of the proposed solution), the computational time needed to partition large combinational circuits and the availability of sh-METIS in a free access on the web site of the University of Minnesota have motivated our choice for this academic tool. In a performance comparison of their multilevel partitioning algorithm with other state-of-the-art partitioning schemes, the authors of sh-METIS reported that their algorithm produces partitioning that are on the

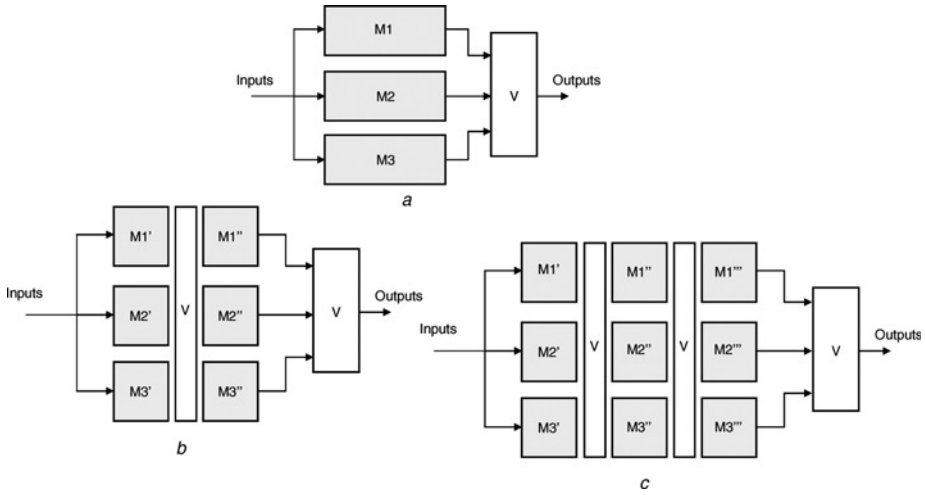

Figure 5 *Improvement of the TMR architecture*

a Basic
b Double
c Triple TMR architectures

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average 6–23% better (in terms of cut size) than existing algorithms, and often requires 4–10 times less time than that required by other schemes. The final step consists in adding voters in the place of hyper-cuts. The number of added voters is equal to number of hyper-cuts that is optimal using sh-METIS software.

With this technique, the tolerance of the TMR architecture increases with the increase of the number of partitions. The main drawback of this technique is the requirement of additional voters. Table 3 reports partitioning results.

The first column lists the circuit names. The second column gives the number of voters of a basic TMR architecture. This number is equal to the number of module outputs (each module output feeds one voter). The third column gives results (number of voters and area overhead computed using equivalent gates compared to a basic TMR architecture) of partitioning circuits into two equivalent blocks (*Double TMR*). For example, circuit c7552 requires 108 voters to implement a *Basic TMR*. The partitioning of this circuit needs 26 hyper-cuts. So, the total number of voters needed to implement a *Double TMR* becomes 134. That represents an area overhead of about 0.69% (remember that this percentage considers the area of voters and modules). In the same way, the fourth column of Table 3 shows results of partitioning circuits into three equivalent blocks (*Triple TMR*). From these results, we notice that the area overhead of this partitioning technique is low for large benchmark circuits; less than 2% for the larger ISCAS'85 and less than 5% for the largest ITC'99.

4.2 Experimental results

The ATPG procedure presented in Section 3.2 has been run on *Double* and *Triple TMR* architectures.

Table 3 Area overhead because of the TMR architecture partitioning

Circuit	Basic TMR # Voter	Double TMR		Triple TMR	
		# Voter	Area overhead (%)	# Voter	Area overhead (%)
c432	7	29	10.55	38	14.86
c499	32	49	6.14	59	9.75
c880	26	40	3.02	39	2.81
c1908	25	53	3.03	68	4.65
c2670	140	160	1.40	179	2.72
c3540	22	56	1.90	95	4.09
c5315	123	149	1.05	161	1.53
c6288	32	49	0.58	64	1.10
c7552	108	134	0.69	158	1.32
b01	7	17	16.08	19	19.29
b02	5	8	8.15	9	10.87
b03	34	43	4.25	47	6.14
b04	74	99	3.23	109	4.52
b05	60	73	1.08	91	2.57
b06	15	22	8.64	26	13.58
b07	57	80	4.58	84	5.38
b08	25	41	7.25	51	11.79
b09	29	40	4.96	44	6.77
b10	23	36	5.28	50	10.97
b11	37	76	6.14	94	8.97
b12	127	139	0.85	167	2.84
b13	63	66	0.67	70	1.56

Table 4 Comparisons of basic TMR with double and triple TMR architectures

Circuit	Basic TMR					Double TMR					Triple TMR				
	A_O	$Y_v < 1$		$Y_v = 1$		A_O	$Y_v < 1$		$Y_v = 1$		A_O	$Y_v < 1$		$Y_v = 1$	
		R_{min} (%)	R (%)	R_{min} (%)	R (%)		R_{min} (%)	R (%)	R_{min} (%)	R (%)		R_{min} (%)	R (%)	R_{min} (%)	R (%)
c432	3.10	94.41	41.00	92.79	41.00	3.43	98.42	87.03	93.38	87.03	3.57	99.65	95.56	93.59	95.56
c499	3.39	98.04	51.72	93.32	51.72	3.60	99.89	89.17	93.63	89.17	3.72	NA	95.11	93.79	95.11
c880	3.18	95.62	78.41	92.95	78.41	3.27	96.77	92.58	93.12	92.58	3.27	96.77	96.47	93.12	96.47
c1908	3.08	94.08	56.42	92.75	56.42	3.18	95.62	89.49	92.95	89.49	3.23	96.28	96.50	93.05	96.50
c2670	3.33	97.43	75.95	93.22	75.95	3.37	98.85	92.46	93.29	92.46	3.42	98.33	93.90	93.37	93.90
c3540	3.04	93.36	54.09	92.67	54.09	3.10	94.41	88.36	92.79	88.36	3.16	95.34	93.78	92.91	93.78
c5315	3.16	95.34	93.20	92.91	93.20	3.19	95.76	94.30	92.97	94.30	3.20	95.90	96.38	92.99	96.38
c6288	3.03	93.17	38.02	92.65	38.02	3.05	93.55	76.35	92.69	76.35	3.07	93.90	84.14	92.73	84.14
c7552	3.09	94.25	84.92	92.77	84.92	3.11	94.58	94.40	92.82	94.40	3.13	94.89	96.22	92.86	96.22
b01	3.38	97.94	79.35	93.30	79.35	3.92	NA	93.37	94.03	93.37	4.03	NA	95.36	94.15	95.36
b02	3.47	98.79	86.36	93.44	86.36	3.75	NA	91.09	93.83	91.09	3.85	NA	93.28	93.95	93.28
b03	3.57	99.65	87.93	93.59	87.93	3.73	NA	95.07	93.80	95.07	3.79	NA	96.75	93.88	96.75
b04	3.32	97.33	84.32	93.20	84.32	3.42	98.33	93.19	93.37	93.19	3.47	98.79	95.53	93.44	95.53
b05	3.16	95.34	88.65	92.91	88.65	3.19	95.76	89.09	92.97	89.09	3.24	96.41	93.30	93.06	93.30
b06	3.68	NA	87.51	93.74	87.51	4.00	NA	93.68	94.11	93.68	4.18	NA	96.26	94.30	96.26
b07	3.38	97.94	81.91	93.30	81.91	3.54	99.40	91.23	93.55	91.23	3.57	99.65	94.11	93.59	94.11
b08	3.38	97.94	89.09	93.30	89.09	3.63	NA	95.28	93.67	95.28	3.78	NA	96.75	93.86	96.75
b09	3.45	98.61	83.07	93.41	83.07	3.62	NA	95.15	93.66	95.15	3.69	NA	97.13	93.75	97.13
b10	3.31	97.22	89.39	93.19	89.39	3.48	98.88	94.92	93.46	94.92	3.67	NA	97.34	93.73	97.34
b11	3.19	95.76	74.50	92.97	74.50	3.38	97.94	87.75	93.30	87.75	3.47	98.79	93.91	93.44	93.91
b12	3.30	97.11	95.45	93.17	95.45	3.33	97.43	96.27	93.22	96.27	3.39	98.04	97.79	93.32	97.79
b13	3.49	98.97	96.94	93.47	96.94	3.51	99.14	97.36	93.50	97.36	3.54	99.40	97.83	93.55	97.83

Experimental results are reported in Table 4. The first column lists the circuit names. Next, Table 4 is divided into three main parts: *Basic TMR*, *Double TMR* and *Triple TMR*. In each part, the first sub-column gives the area overhead (A_O) needed to implement the TMR architecture. Next sub-columns provide R_{min} and R for two extreme scenarios:

Scenario_1: voters can be defective with the same defect density than the logic part ($Y_v < 1$) as previously considered in (12).

Scenario_2: voters are fault-free ($Y_v = 1$) as they are manufactured with robust design techniques. Consequently, (12) becomes

$$Y_{TMR} = e^{3\ln Y_C} \times \left(1 - 3\ln Y_C + \sum_{i=2}^{\infty} R^{C_i^2} \times \frac{(-3\ln Y_C)^i}{i!}\right) \quad (16)$$

Let us first comment the data corresponding to Scenario_1. In that scenario, the fault tolerance improvement achieved by implementing a double or a triple TMR is not enough to make TMR suitable for yield improvement. In fact, only three circuits (c1908, c5315 and c7552) successfully resort to TMR architectures when they are partitioned into three

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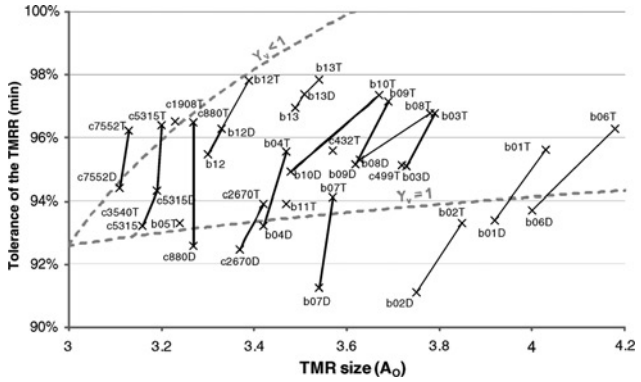

Figure 6 *Improvement of the TMR fault tolerance by circuit partitioning*

equivalent blocks (Triple TMR). On the other hand, if voters are fault-free (Scenario_2), implementing a TMR architecture for yield improvement purpose is suitable for almost all benchmark circuits (20 circuits among the 22 considered) always in the case of *Triple TMR*.

Data reported in Table 4 are also shown in Fig. 6. It gives $R_{\min}$ as a function of A_O for the two scenarios ($Y_v < 1$ and $Y_v = 1$). In this figure, each circuit is represented by a cross obtained from coordinates (A_O, R). Circuit names with a letter D (T) represent results achieved with a *Double* (*Triple*) *TMR* implementation. For a better legibility, only circuits having an R probability greater than 90% are reported. From Fig. 6, two main conclusions can be drawn. First, the figure demonstrates that partitioning the logic part increases the tolerance of the resulting TMR architecture (*Double* and *Triple TMR*). Second, this figure shows that most of circuits have a resulting tolerance in between grey dotted lines and only three of them have a resulting tolerance higher than the $R_{\min}$ limit corresponding to $Y_v < 1$ (i.e. voters can be defective with the same defect density than the logic part). These results clearly demonstrate that the logic part partitioning increases the tolerance of the resulting TMR architecture, but it must be completed with techniques making voters more robust (Y_v close to 100%). For example, voters can be realised in software or with more robust design techniques as presented in [10]. Then, TMR can successfully lead to yield improvement purpose.

5 Conclusion and future work

This paper analyses the use of TMR architectures for the purpose of yield improvement. We have computed the necessary conditions that make TMR architectures more attractive compared to non-tolerant circuits. These conditions are related to (i) the initial yield of the non-tolerant logic structure and (ii) the tolerance of the TMR implementation (the R probability). In order to evaluate the R probability on a set of benchmark circuits, we have developed an ATPG procedure. First results have demonstrated that the TMR architecture does not tolerate enough fault pairs. Consequently, we have proposed to partition the logic modules of the TMR architecture to improve the tolerance of the whole TMR. This has been done by using a hypergraph partitioning technique based on the use of sh-METIS; a software package for partitioning large hyper-graph with a minimal number of hyper-cuts. Results have shown that this improvement of the TMR architecture is very fruitful to improve its tolerance capability. Moreover, they have shown that TMR successfully results in yield improvement only if voters are designed in way to have a yield close to 100%.

Future work will first consist in improving the circuit partitioning. Next, we will focus on other fault-tolerant structures that could be able to tolerate a higher number of manufacturing defects or to have a smaller silicon area. Hardware redundancies have been exploited in this paper by using TMR structures. Information redundancies or a mix between hardware and information redundancies could also be interesting for our future work.

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