Systèmes intégrés adaptatifs ultra basse consommation pour l'Internet des Objets

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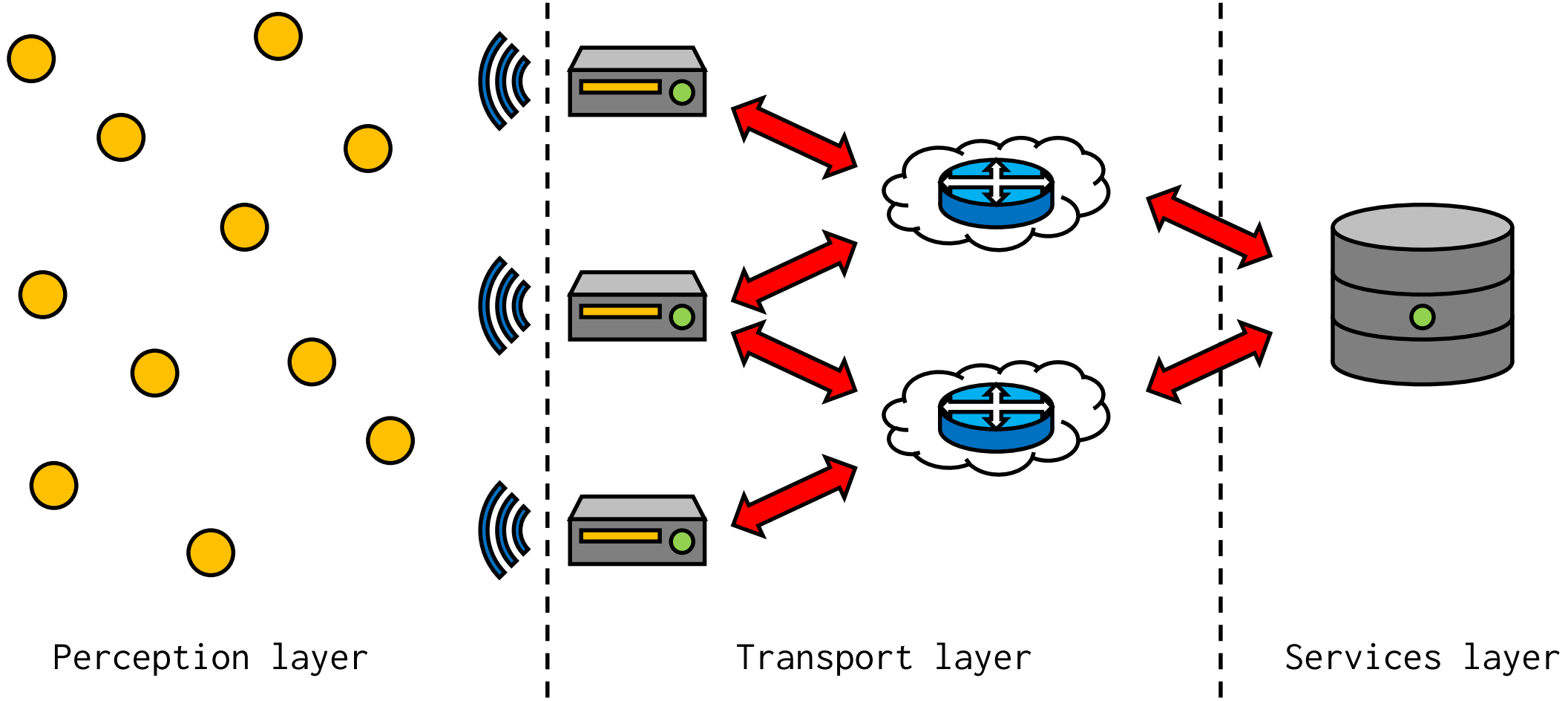
Sous la direction de Pascal Benoit

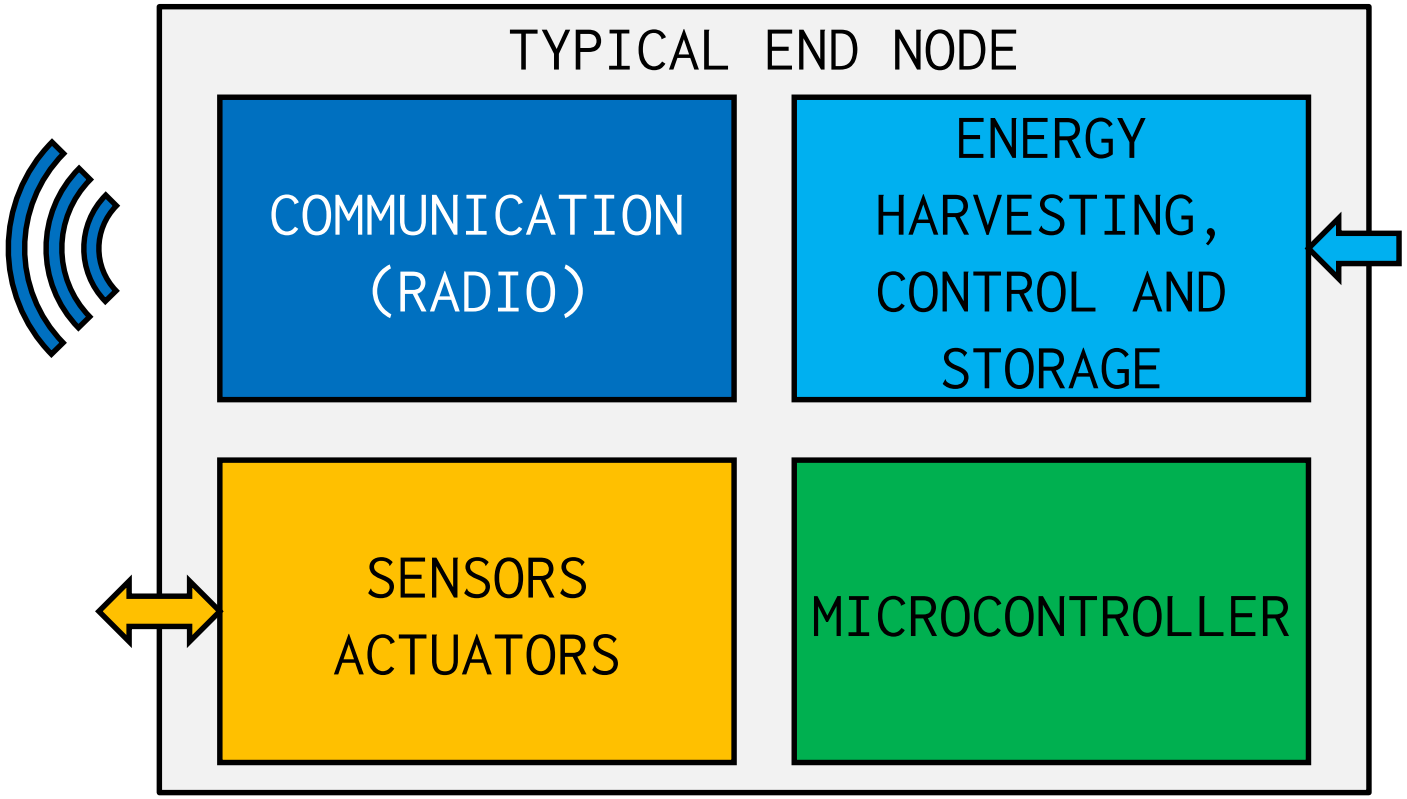
Co-encadré par Lionel Torres

Le 16 juillet 2020

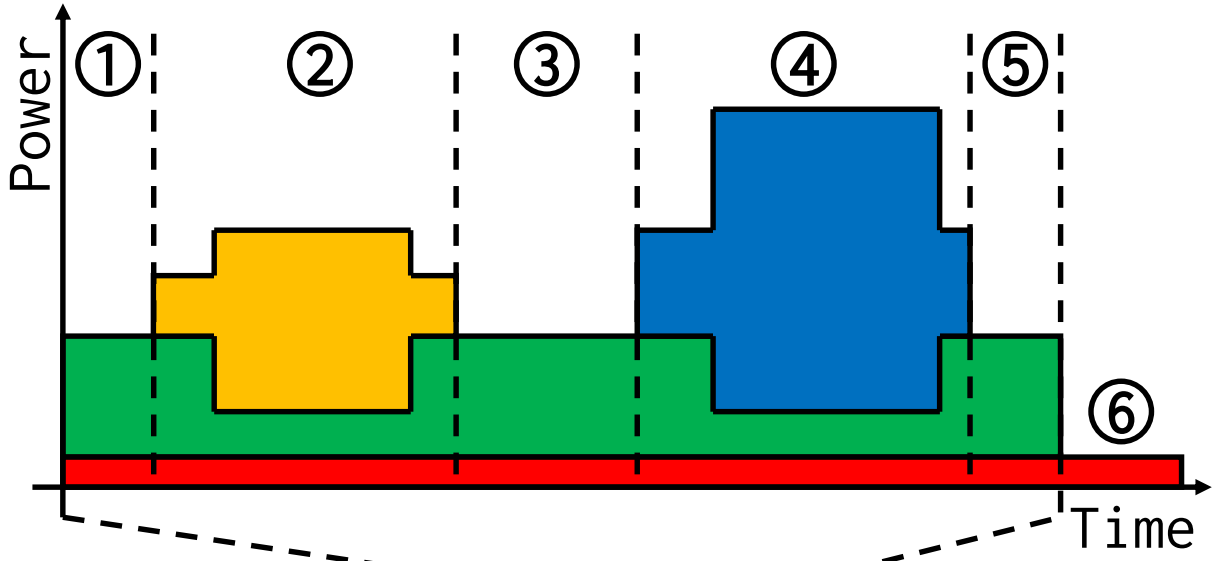
Internet of Things infrastructure



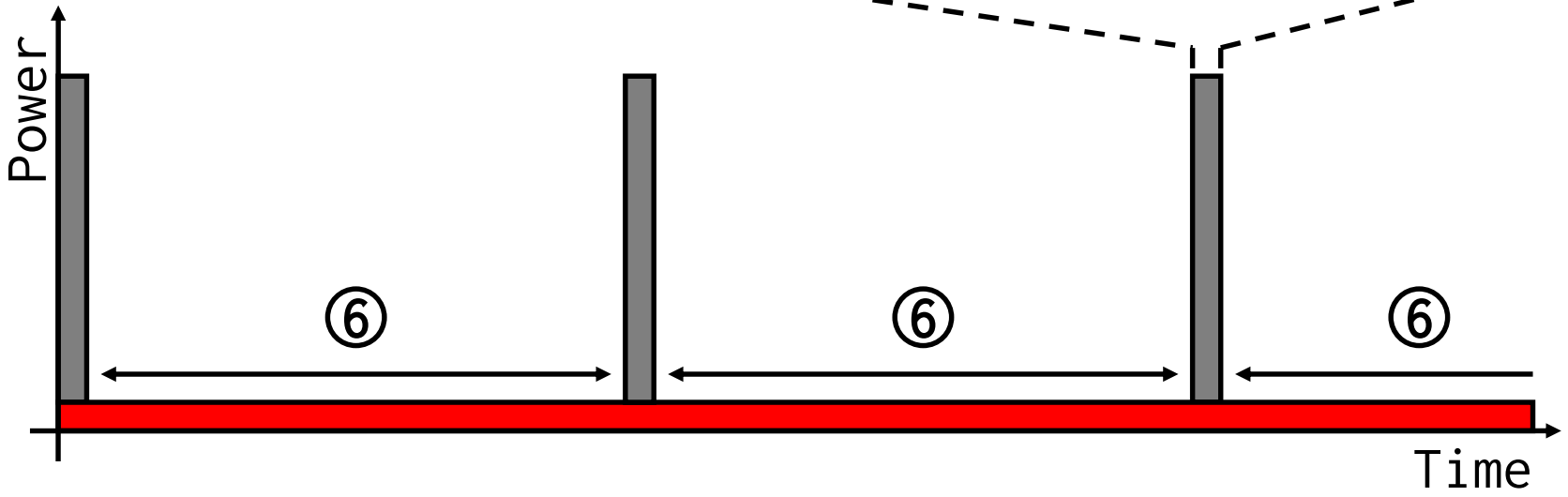
Sensor node


TYPICAL END NODE
COMMUNICATION (RADIO)
ENERGY HARVESTING, CONTROL AND STORAGE
SENSORS ACTUATORS
MICROCONTROLLER

Sensor node application power profile

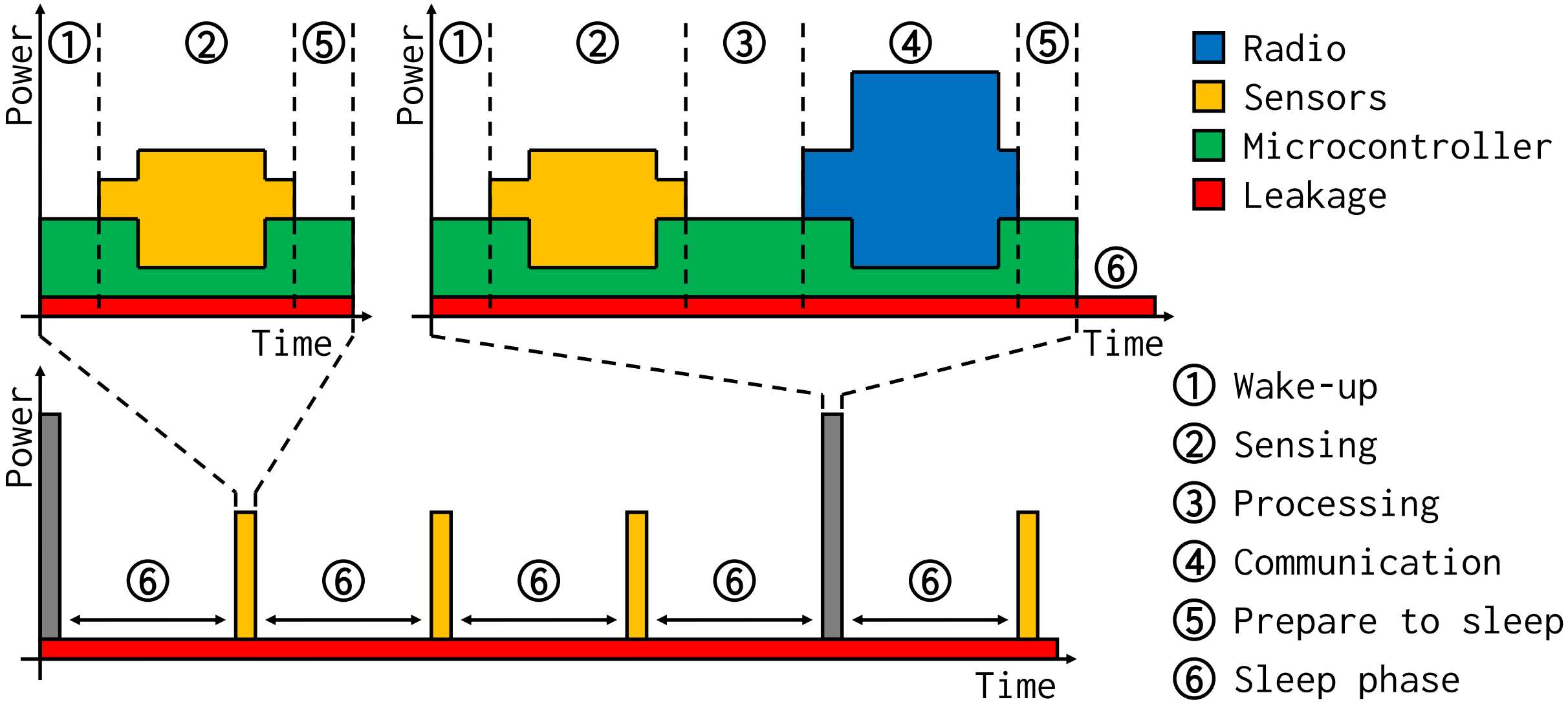


Radio
Sensors
Microcontroller
Leakage

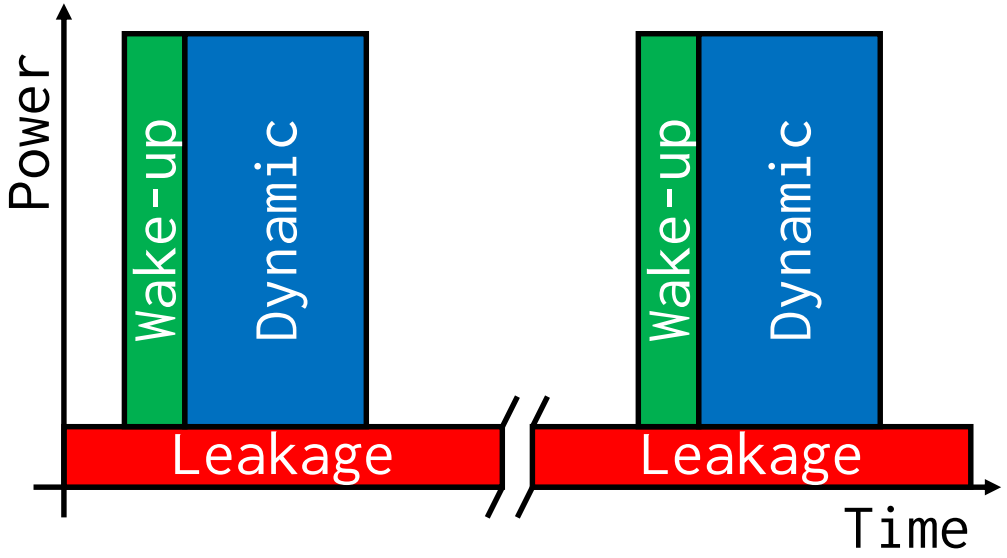


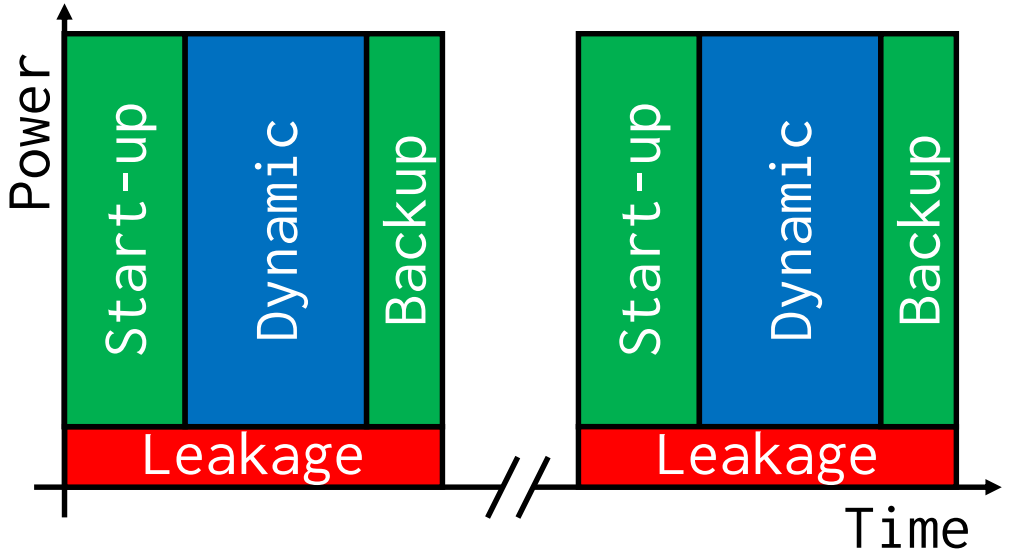
① Wake-up
② Sensing
③ Processing
④ Communication
⑤ Prepare to sleep
⑥ Sleep phase

Low-power strategies



Low-power strategies





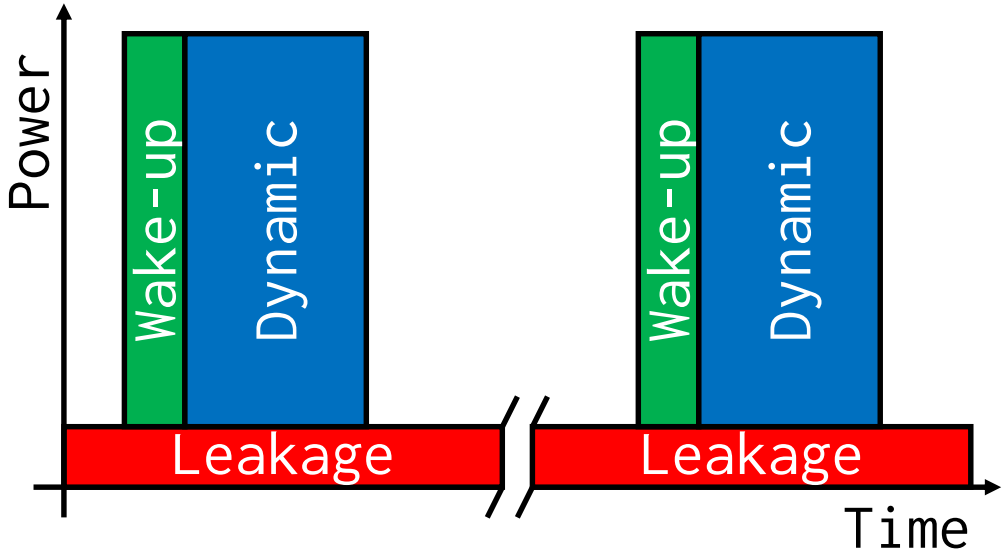
$$E_{loss} = E_{wakeup} + E_{leakage}$$
$$E_{loss} = E_{wakeup} + P_{leakage} \times t_{sleep}$$

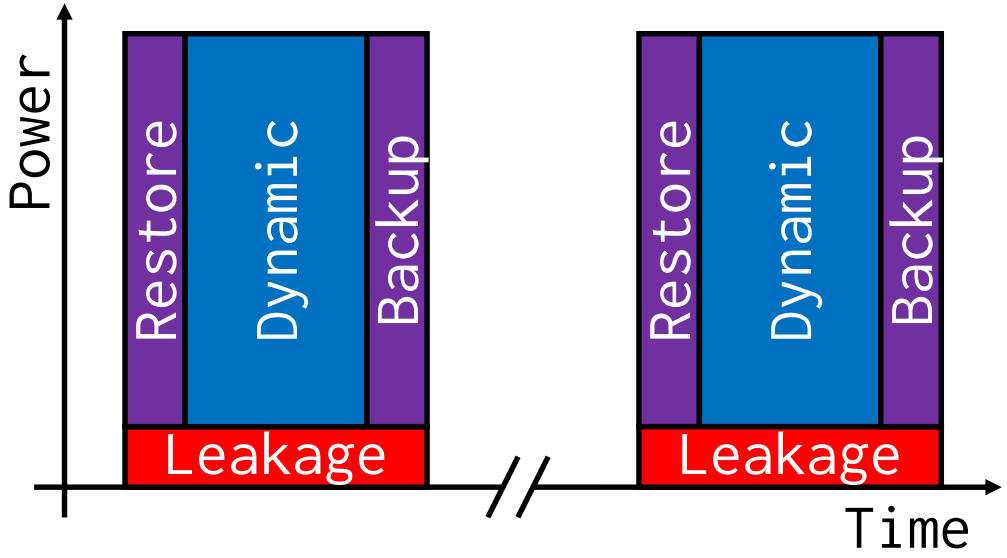
$$>$$

$$E_{loss} = E_{startup} + E_{backup}$$

Energy efficiency achieved when $t_{sleep} > \dfrac{E_{startup} + E_{backup} - E_{wakeup}}{P_{leakage}}$

Normally-off computing





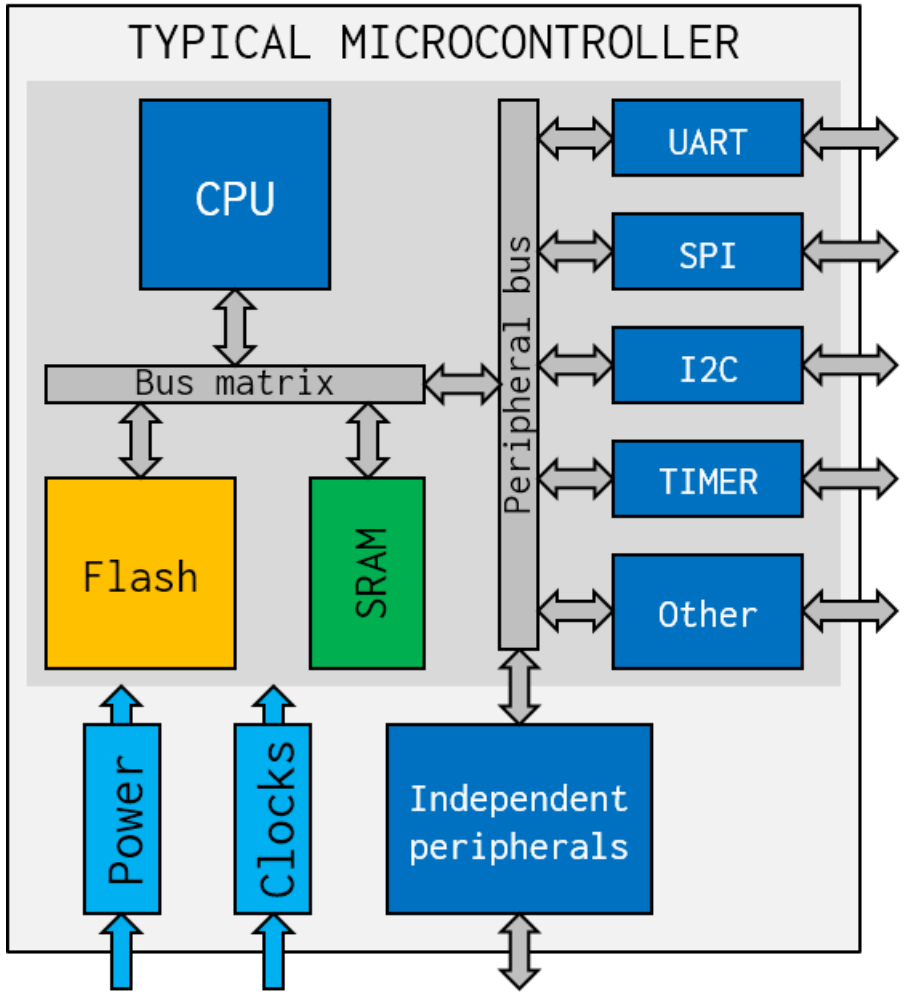
$$E_{loss} = E_{wakeup} + E_{leakage}$$
$$E_{loss} = E_{wakeup} + P_{leakage} \times t_{sleep}$$

$$>$$

$$E_{loss} = E_{restore} + E_{backup}$$

Energy efficiency achieved when $t_{sleep} > \dfrac{E_{restore} + E_{backup} - E_{wakeup}}{P_{leakage}}$

Traditional technologies

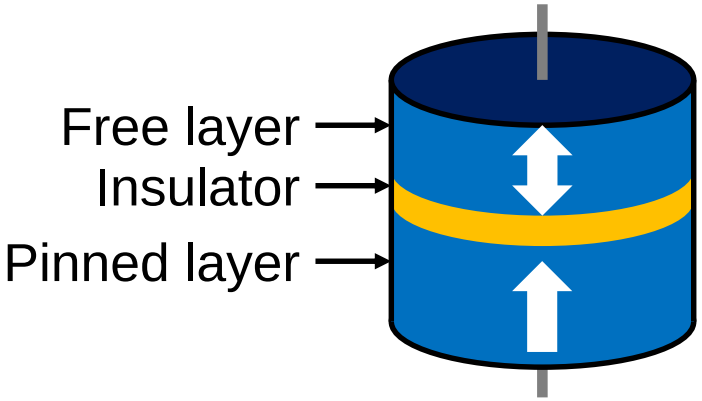


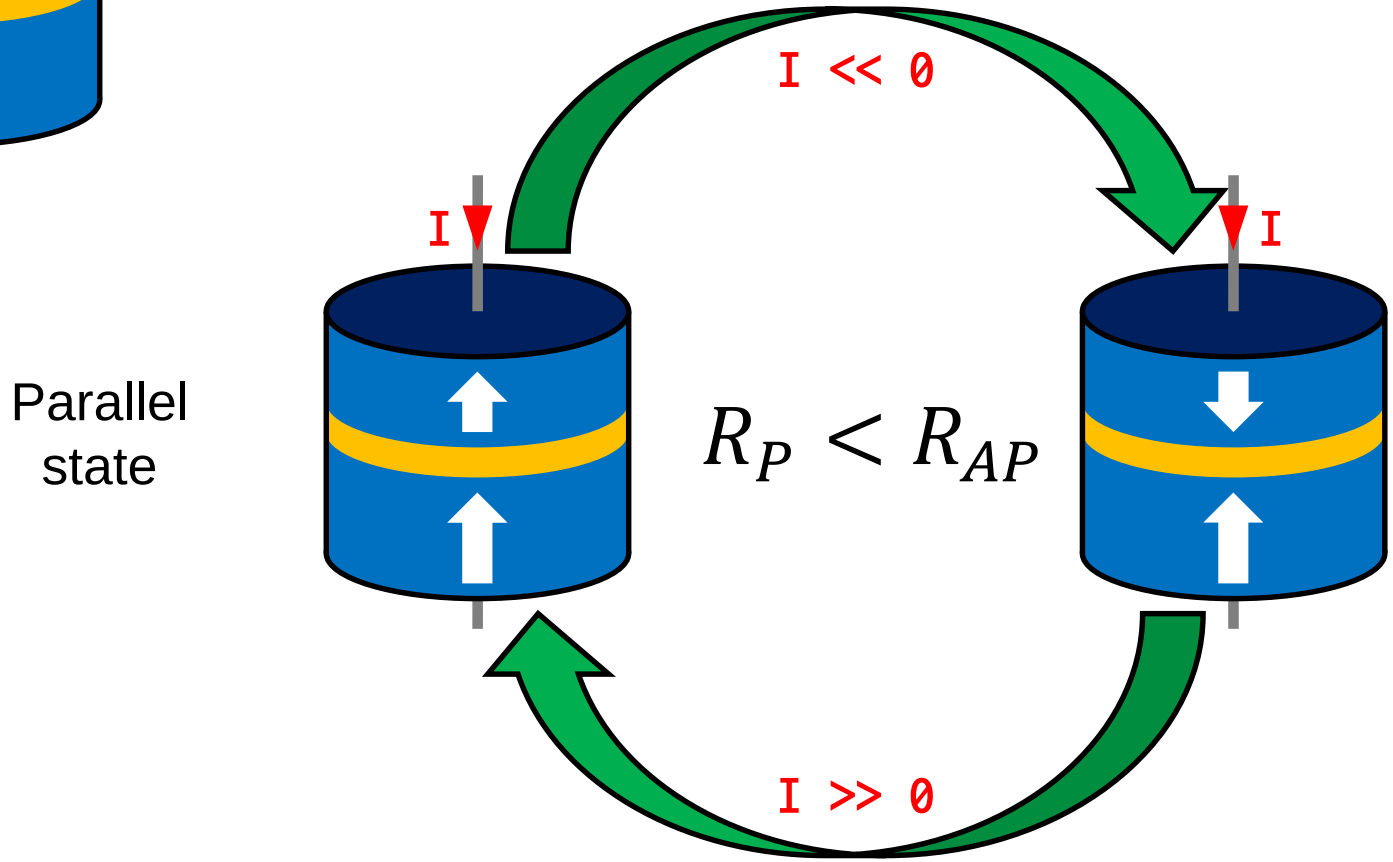
Typical microcontroller memory hierarchy:

- Volatile flip-flops for registers (processor, peripherals, bus...)
  - volatile (data lost when powered down)
- SRAM for application data
  - volatile (data lost when powered down)
- Flash for program and constant data (sometimes for long term data storage)
  - random access for read and programming, but not for erase operations
  - erase and programming operations are slow and use a lot of energy
  - slow, request wait states when clock is too high

How can we use emerging technologies to improve sensor nodes’ energy efficiency?

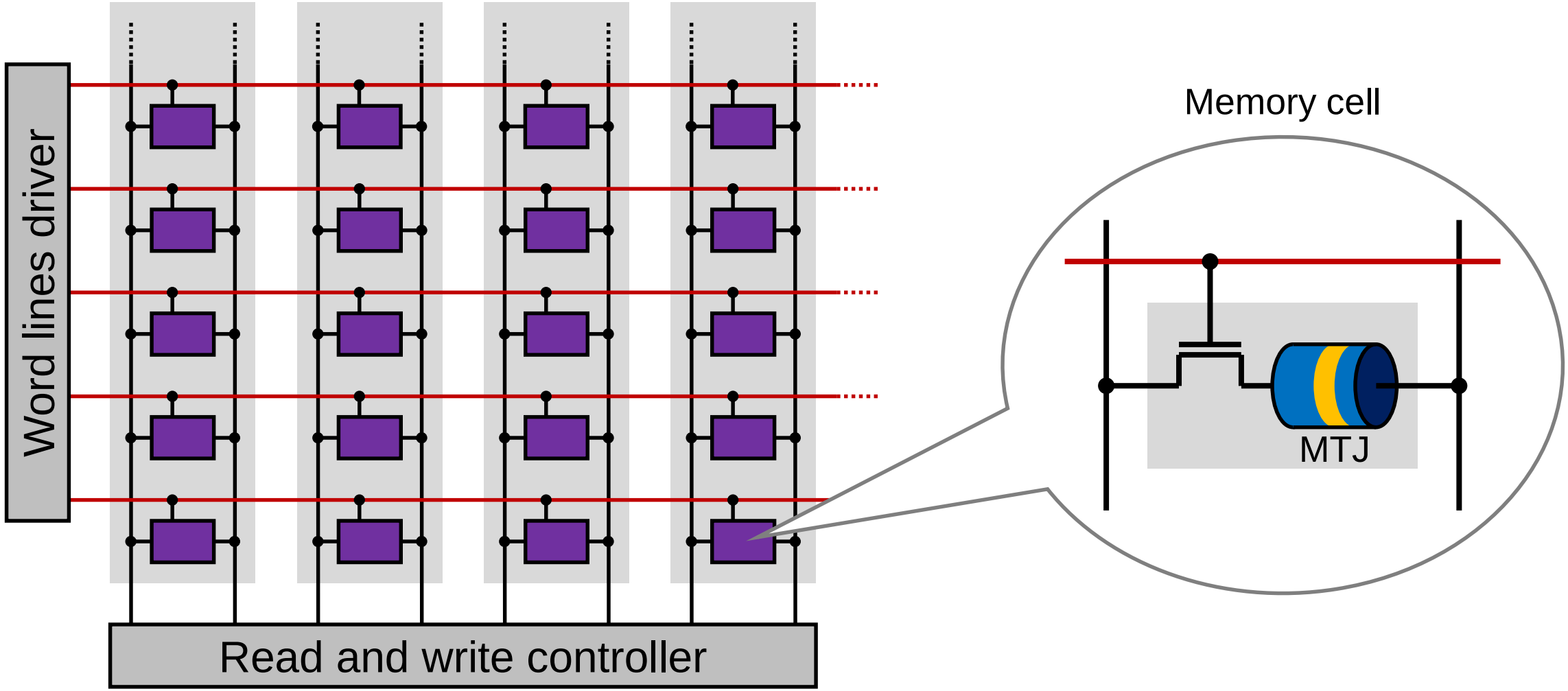
Magnetic tunnel junction





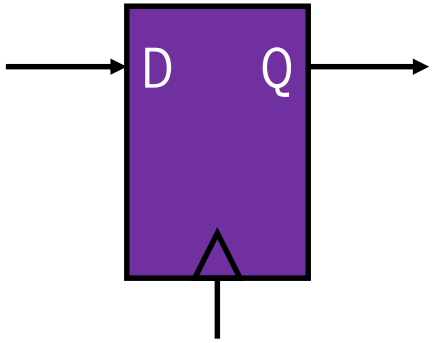
Magnetic memories

Magnetic Random Access Memory - MRAM

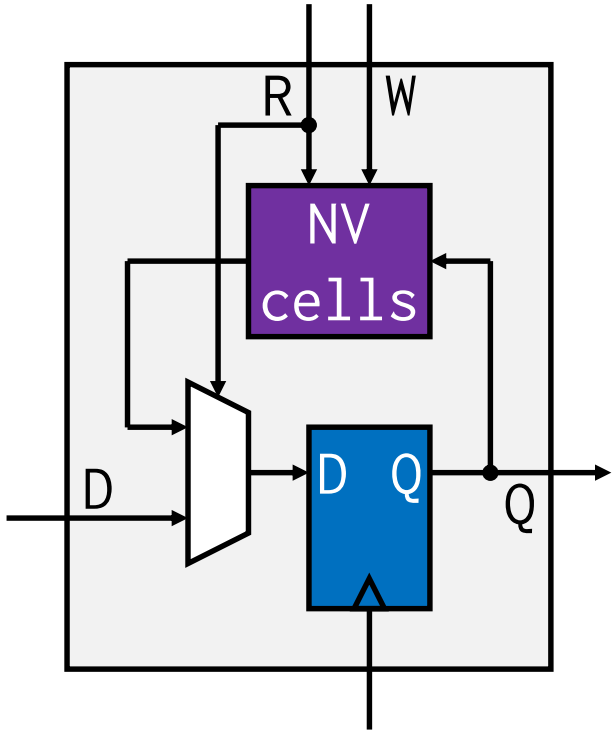


Magnetic memories

Non-volatile flip-flop [1]:
value stored at each cycle

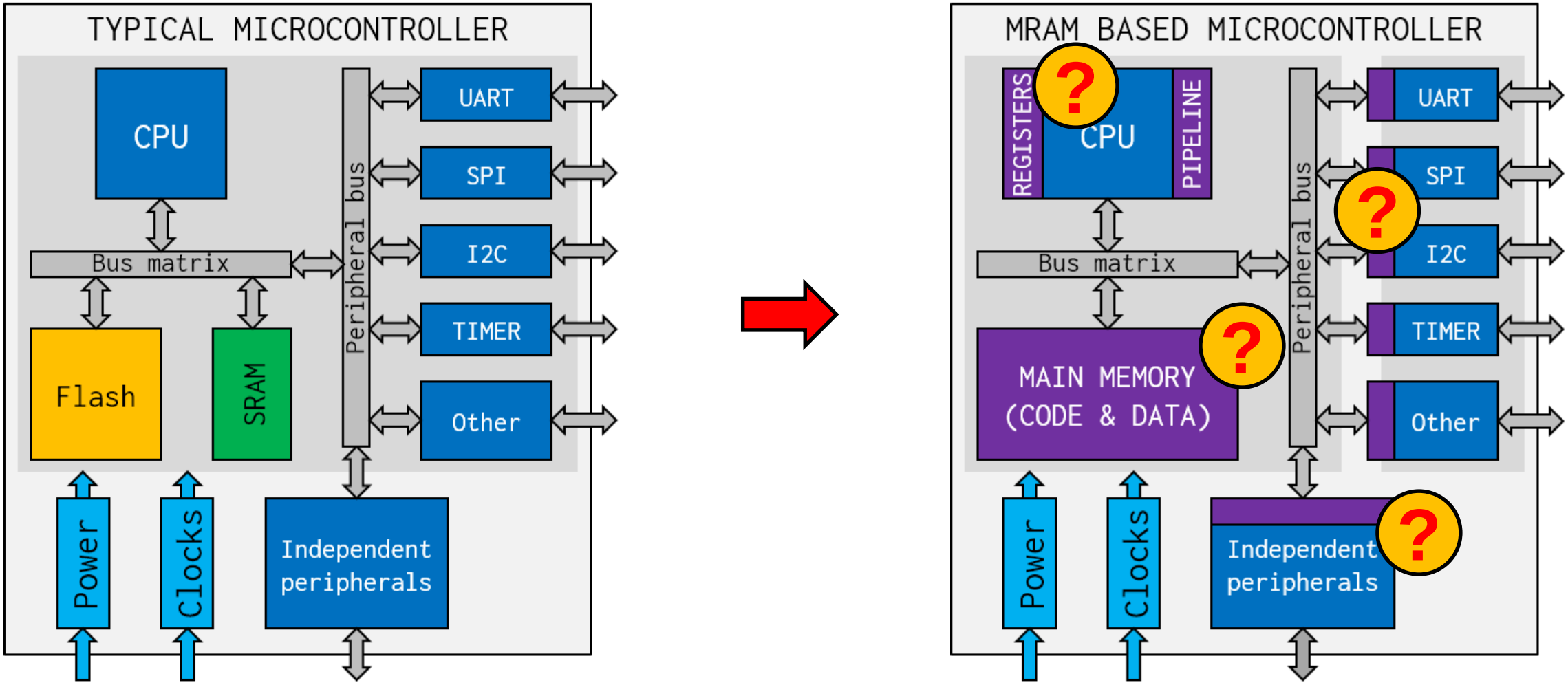


Hybrid flip-flop [2]:
value (re)stored on-demand

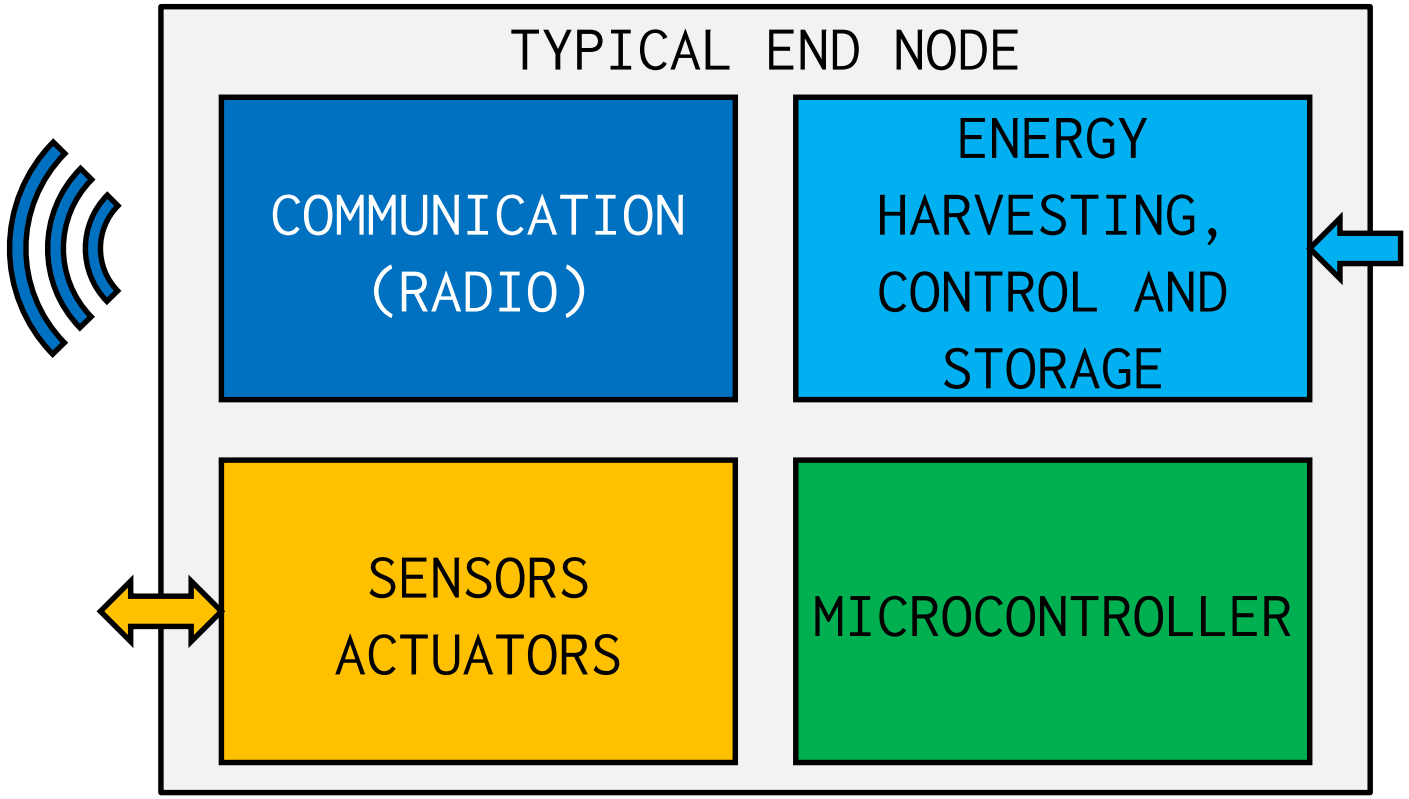


[1] W. Zhao *et al.*, “Spin-MTJ based Non-volatile Flip-Flop”, 2007
[2] S. Senni *et al.*,“From Spintronic Devices to Hybrid CMOS/Magnetic System On Chip”, 2018

Hybrid architecture

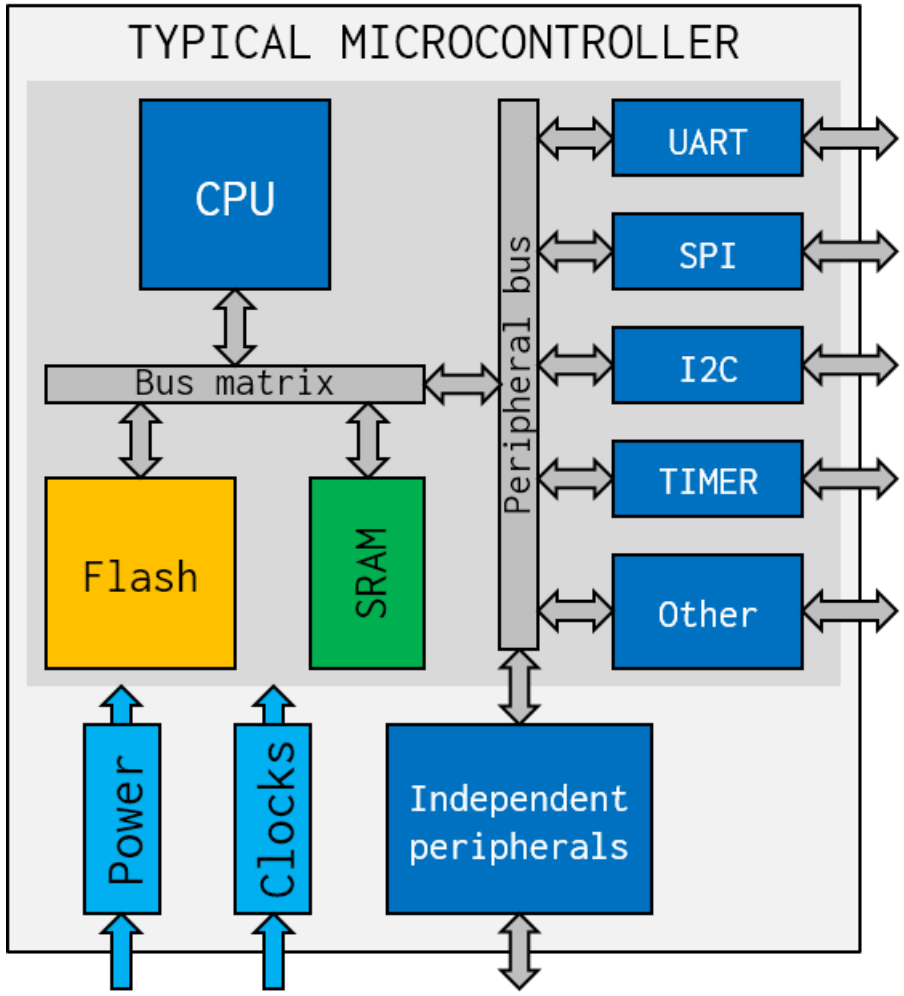


Sensor node evaluation



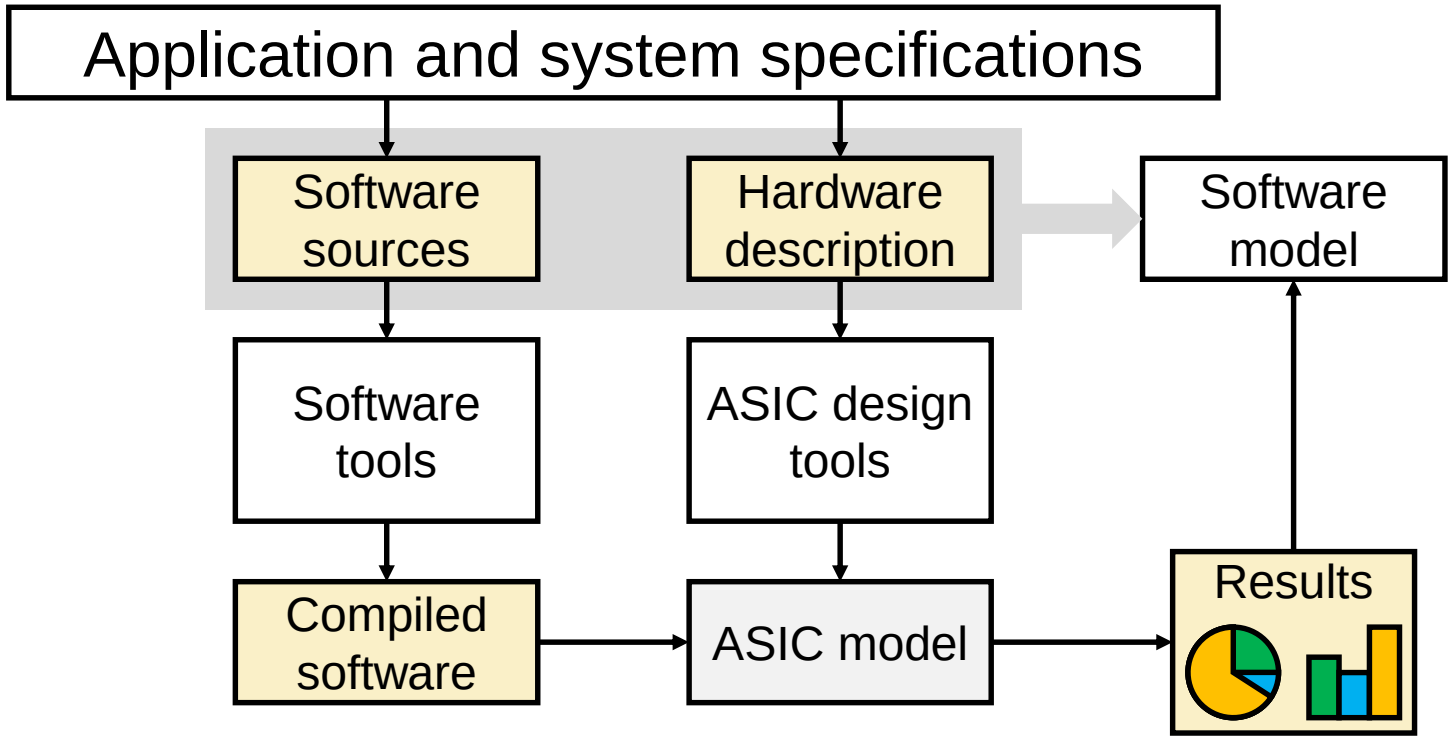
External peripherals (sensors, actuators, radio modules, energy storage units, power management units, harvesters...) power consumption can be obtained from measures or datasheets information

System-on-chip evaluation

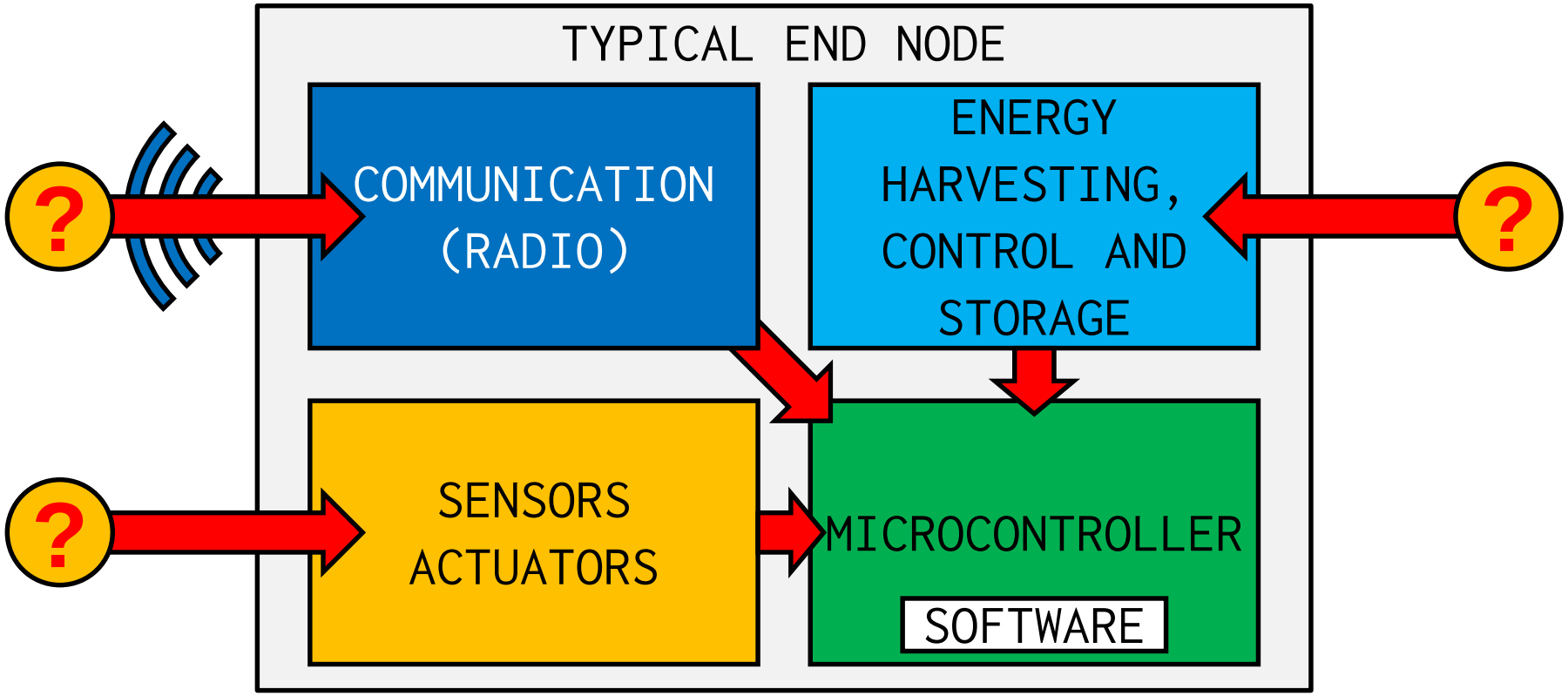


- Shared power supply between internal components
- Cannot discriminate each block's power consumption
- Black boxes with unknown but non-negligible power consumption
- No enough precisions in datasheet (privacy)

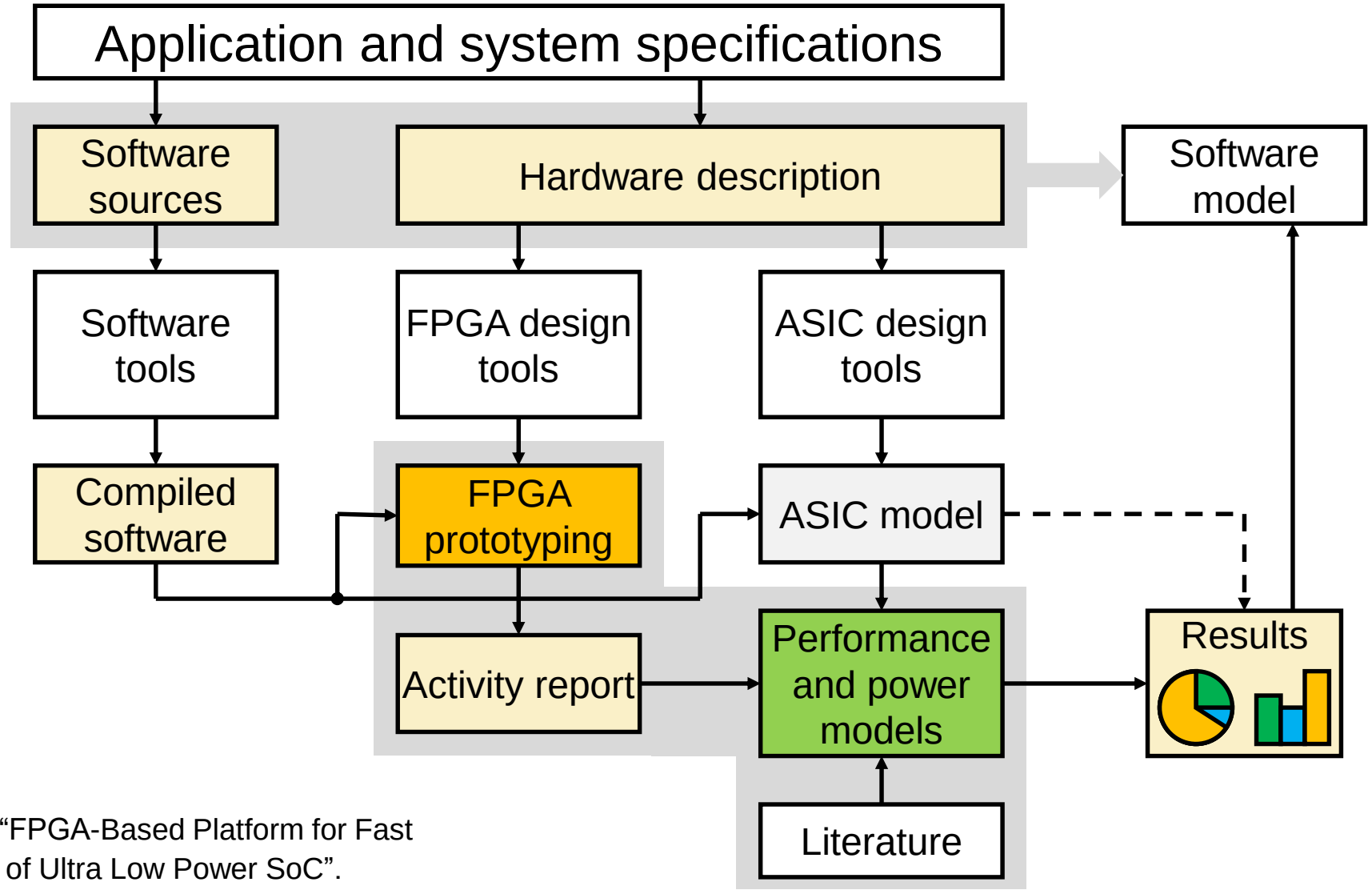
Exploration flow



External perturbations

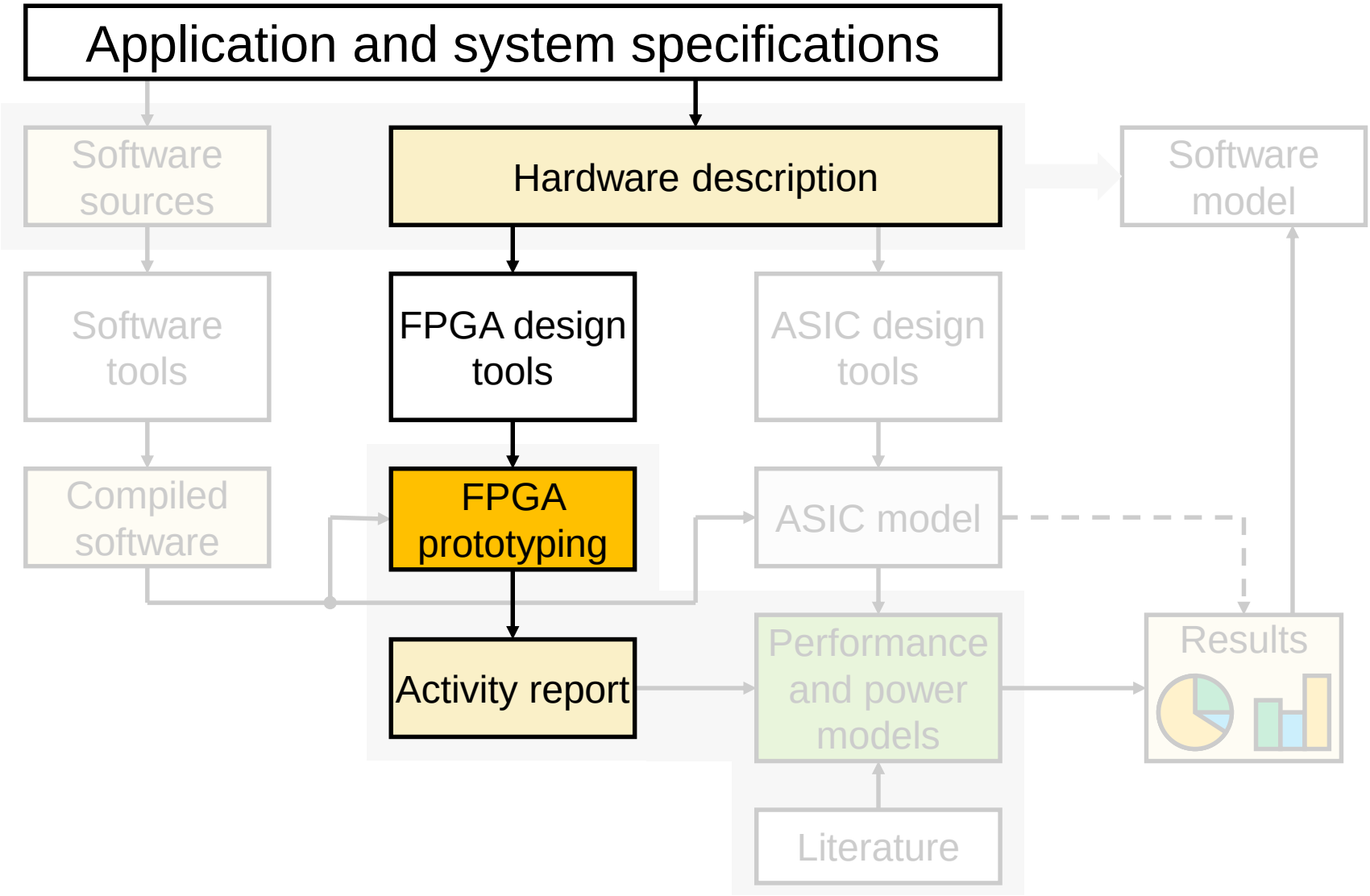


Exploration flow

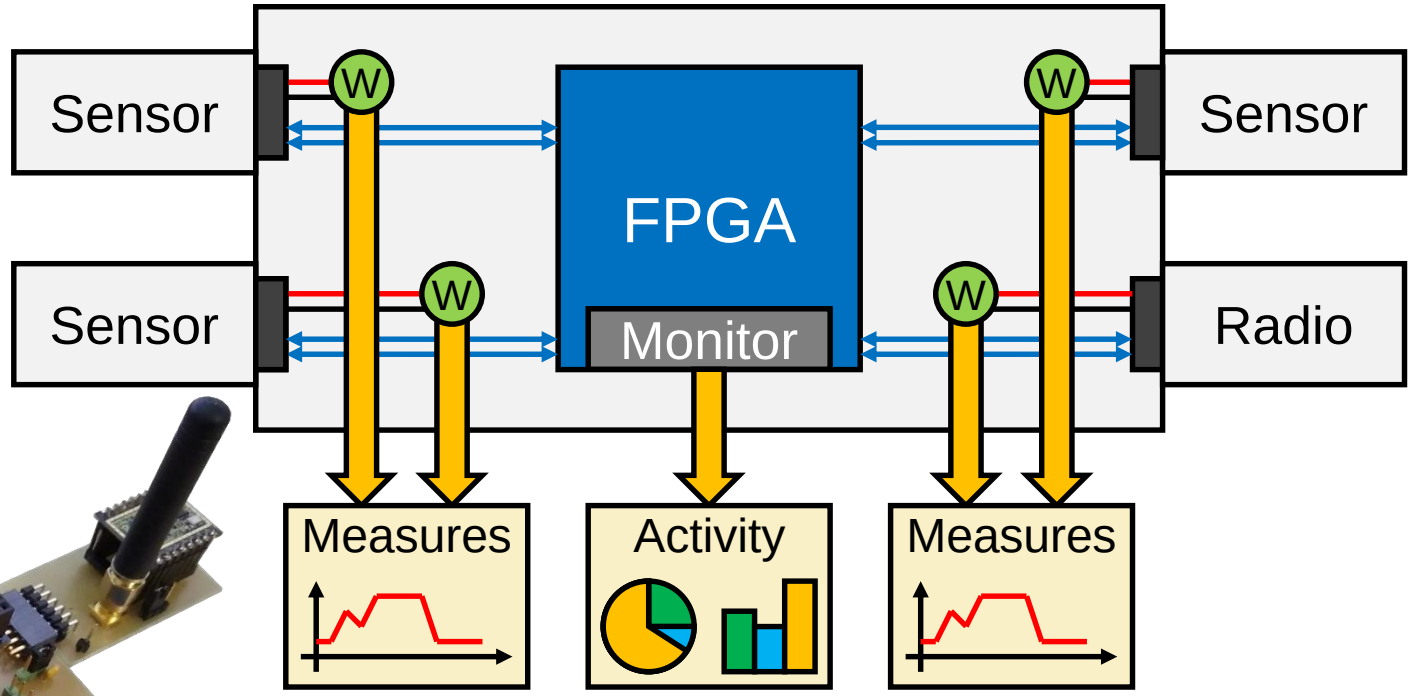


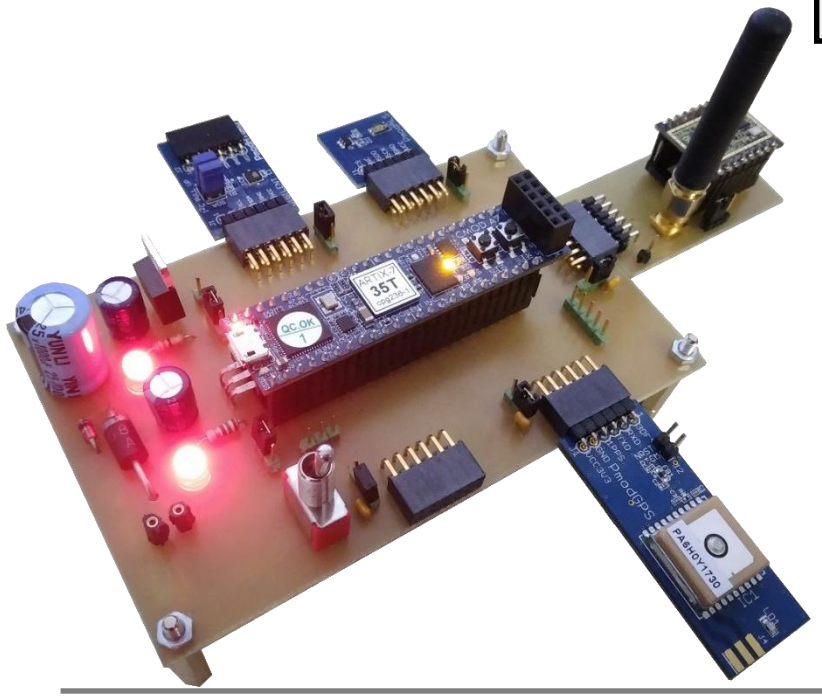
G. Patrigeon *et al.*, “FPGA-Based Platform for Fast Accurate Evaluation of Ultra Low Power SoC”.

Exploration flow



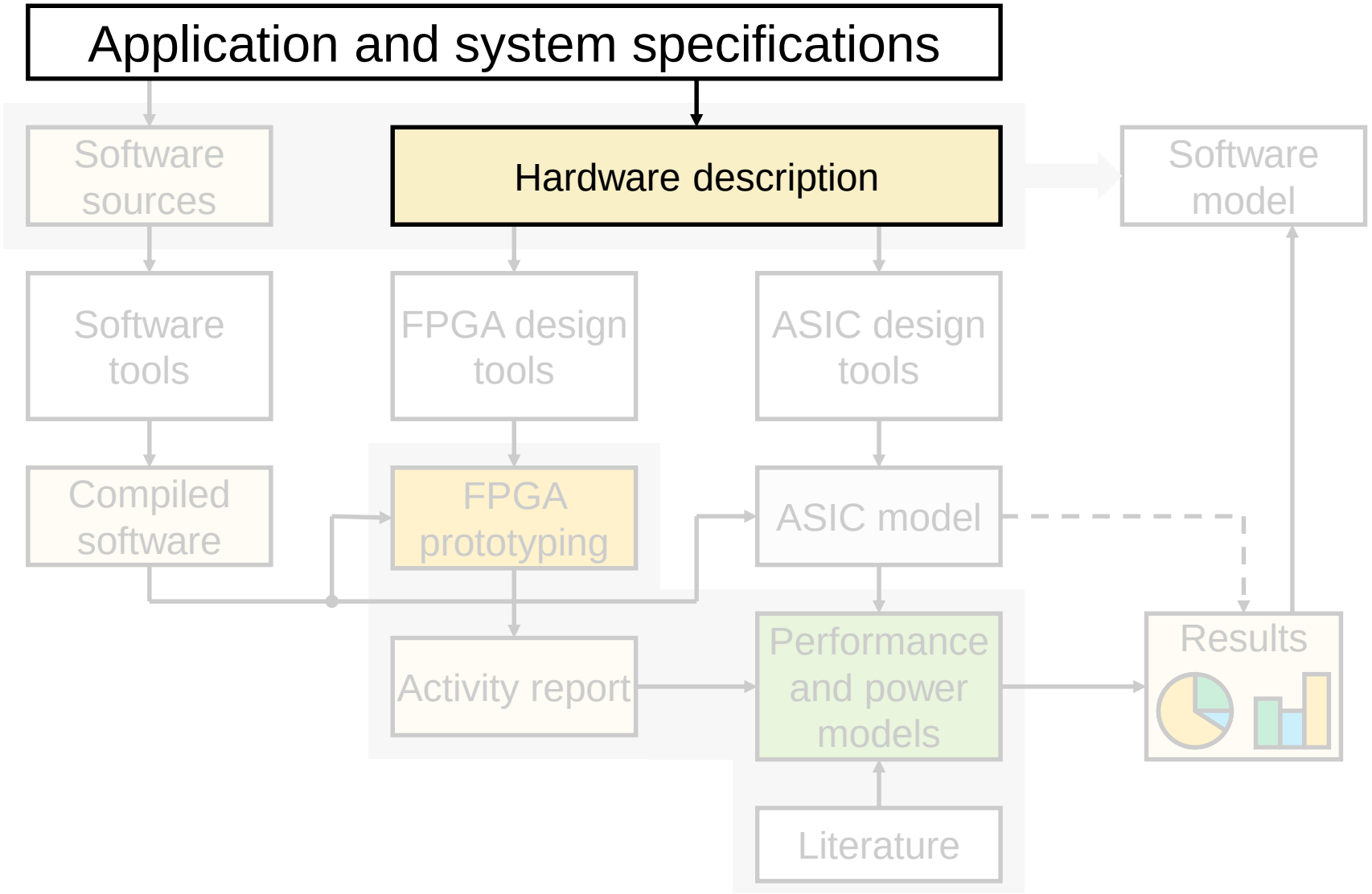
FlexNode





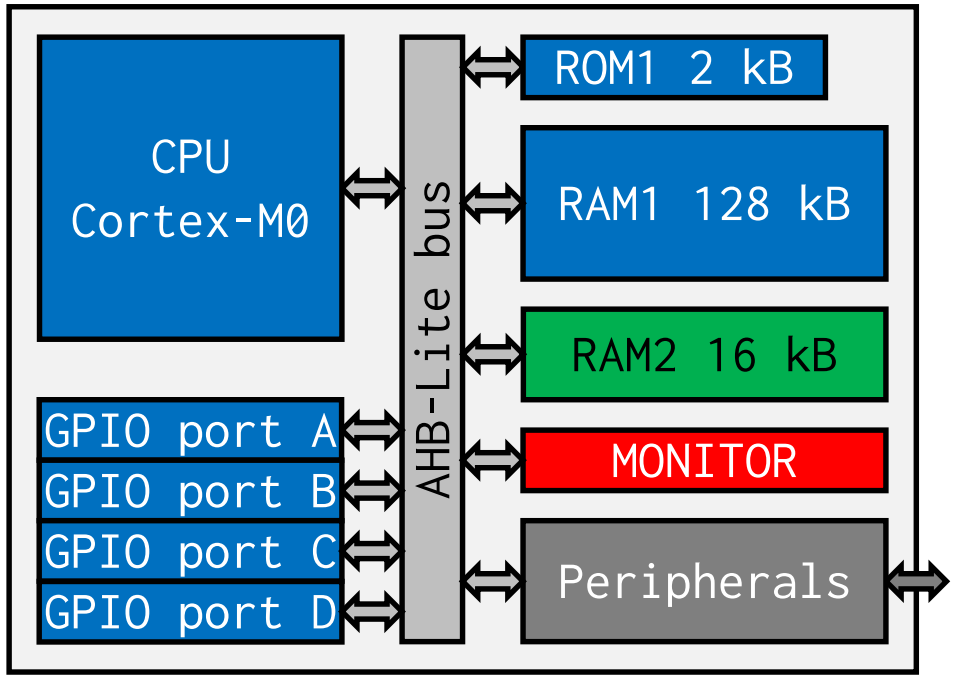
G. Patrigeon *et al.*, “FlexNode: a reconfigurable Internet of Things node for design evaluation”.

Exploration flow

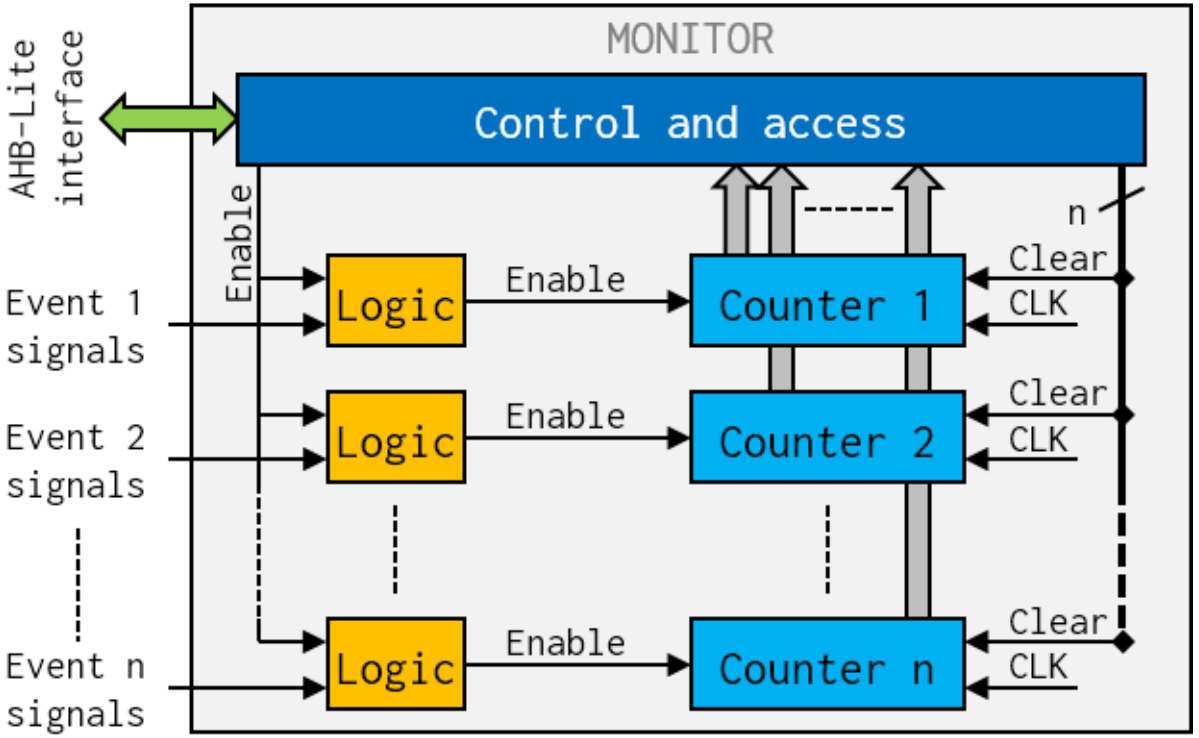


Microcontroller architecture

- Processor: ARM Cortex-M0 r1p0
- Internal bus: AHB-Lite
- Program memory: 128 kB RAM
- Data memory: 16 kB RAM
- Bootloader memory: 2 kB ROM
- Peripherals: GPIO, UART, I²C, SPI, Timers, PPS
- Activity monitor



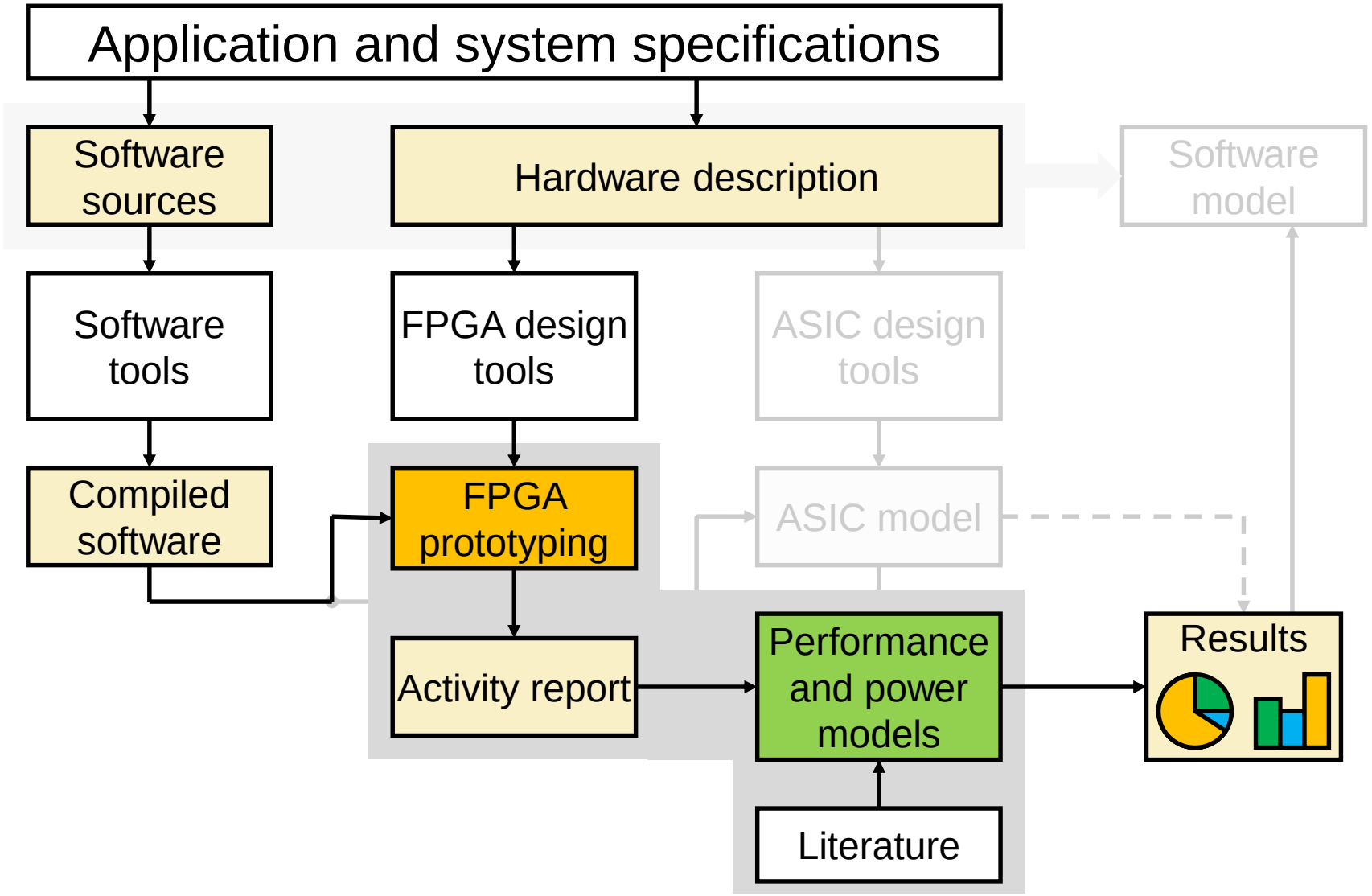
Activity Monitor



Captured events:

- Cycles
- Executed instructions
- Read operations
  - data reads
  - instruction fetches
- Writes operations (with data width)

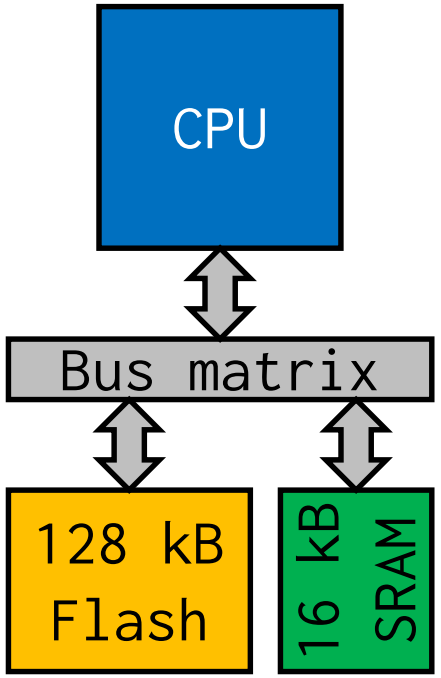
Exploration flow



Main memory exploration

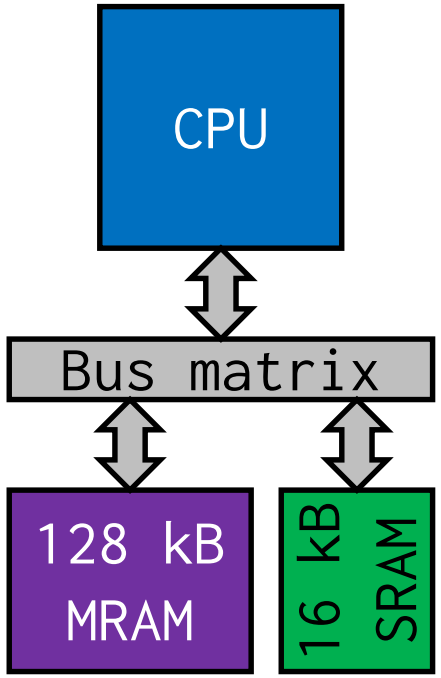
①

program in Flash
data in SRAM
(typical MCU)



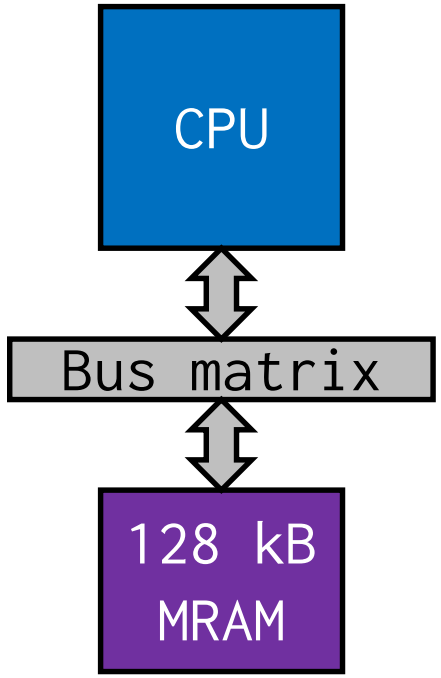
②

program in MRAM
data in SRAM



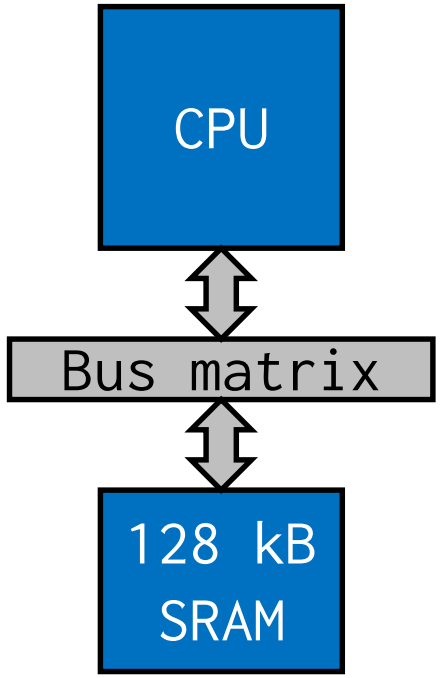
③

program and data
in MRAM



④

program and data
in SRAM



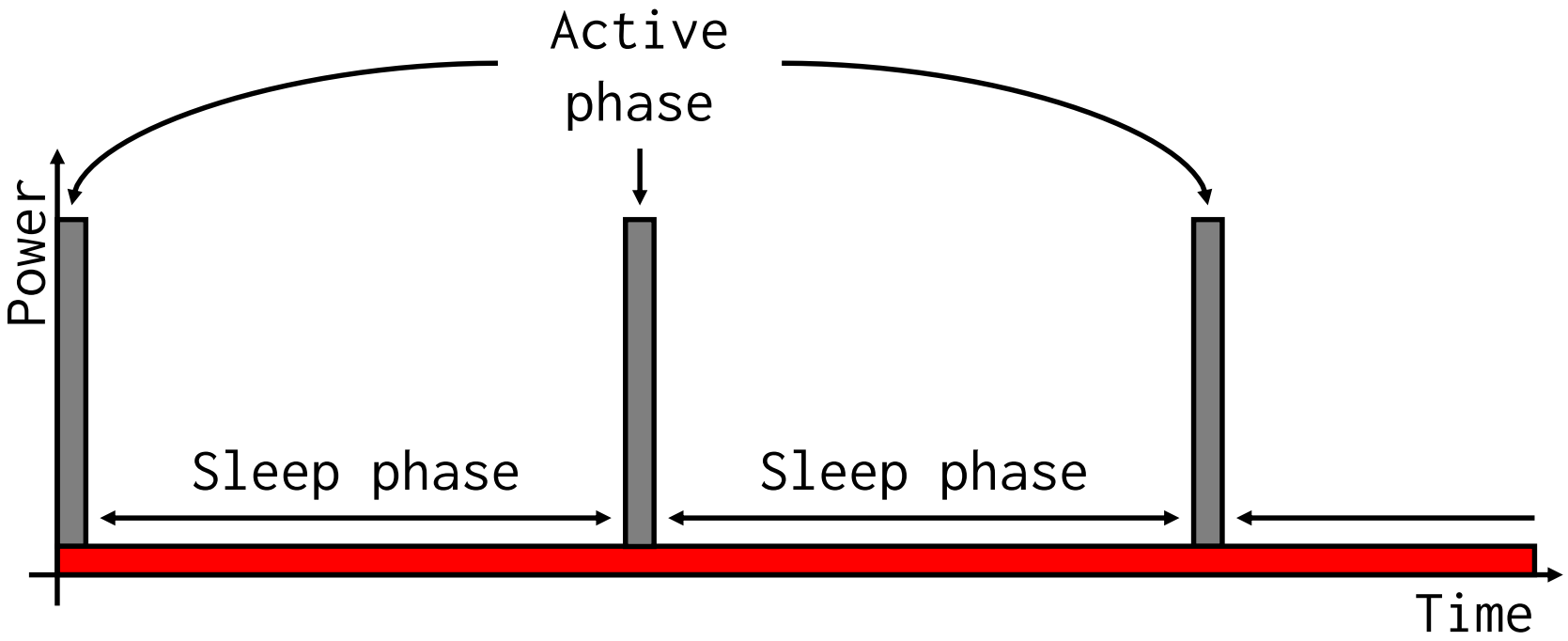
Main memory exploration

Dynamic energy consumption:

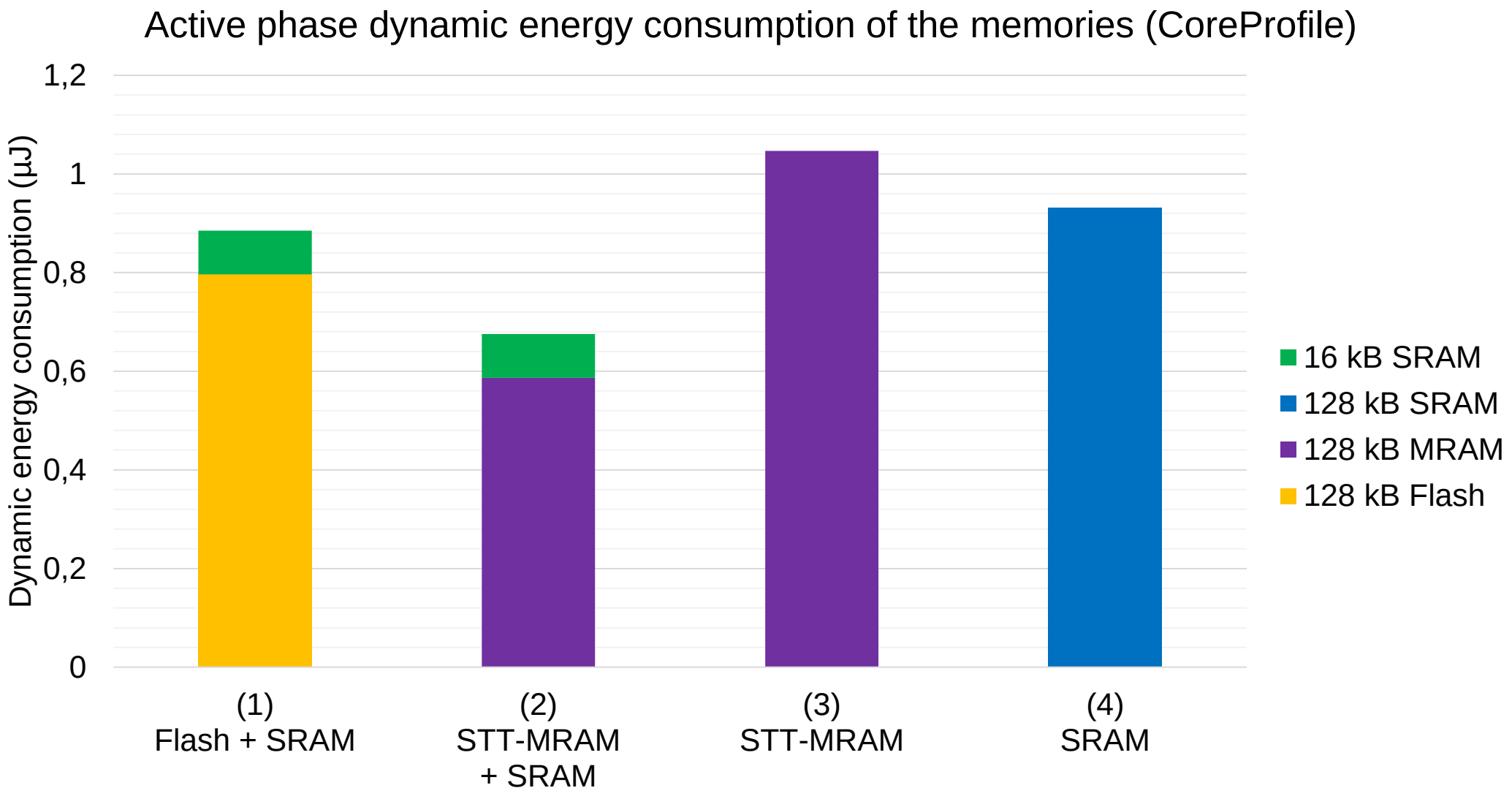
Operation	Flash 128 kB [1]	STT-MRAM 128 kB [2]	SRAM 128 kB [3]	SRAM 16 kB [3]
32-bit read	39.4 pJ	29 pJ	30.6 pJ	11.7 pJ
8-bit write	-	24 pJ	5.85 pJ	2.68 pJ
16-bit write	-	48 pJ	11.7 pJ	5.36 pJ
32-bit write	-	96 pJ	23.4 pJ	10.7 pJ

[1] Igor Kouznetsov, “Embedded 28-nm Charge-Trap NVM Technology”, 2017
[2] Kotb Jabeur and Guillaume Prenat, “Design of a full 1Mb STT-MRAM based on advanced FDSOI technology”, 2017
[3] STMicroelectronics 28 nm FD-SOI memories

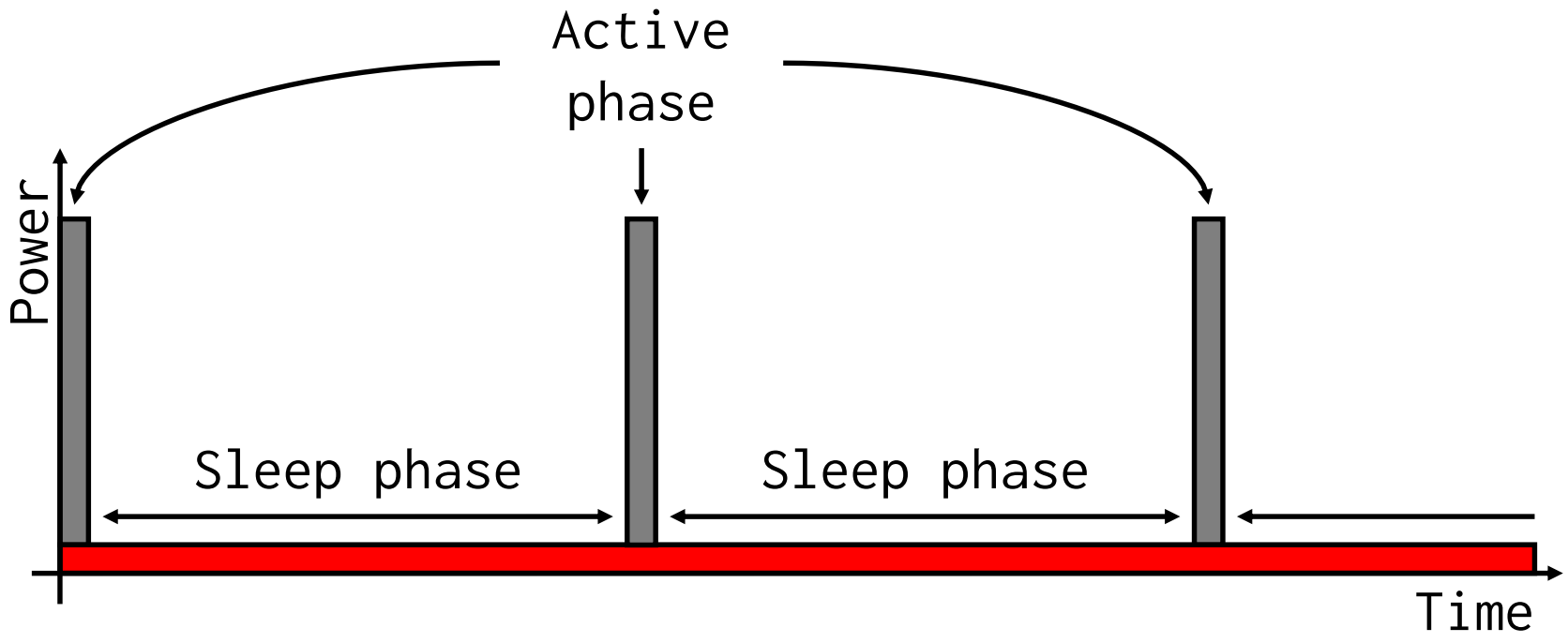
Main memory exploration (benchmark)



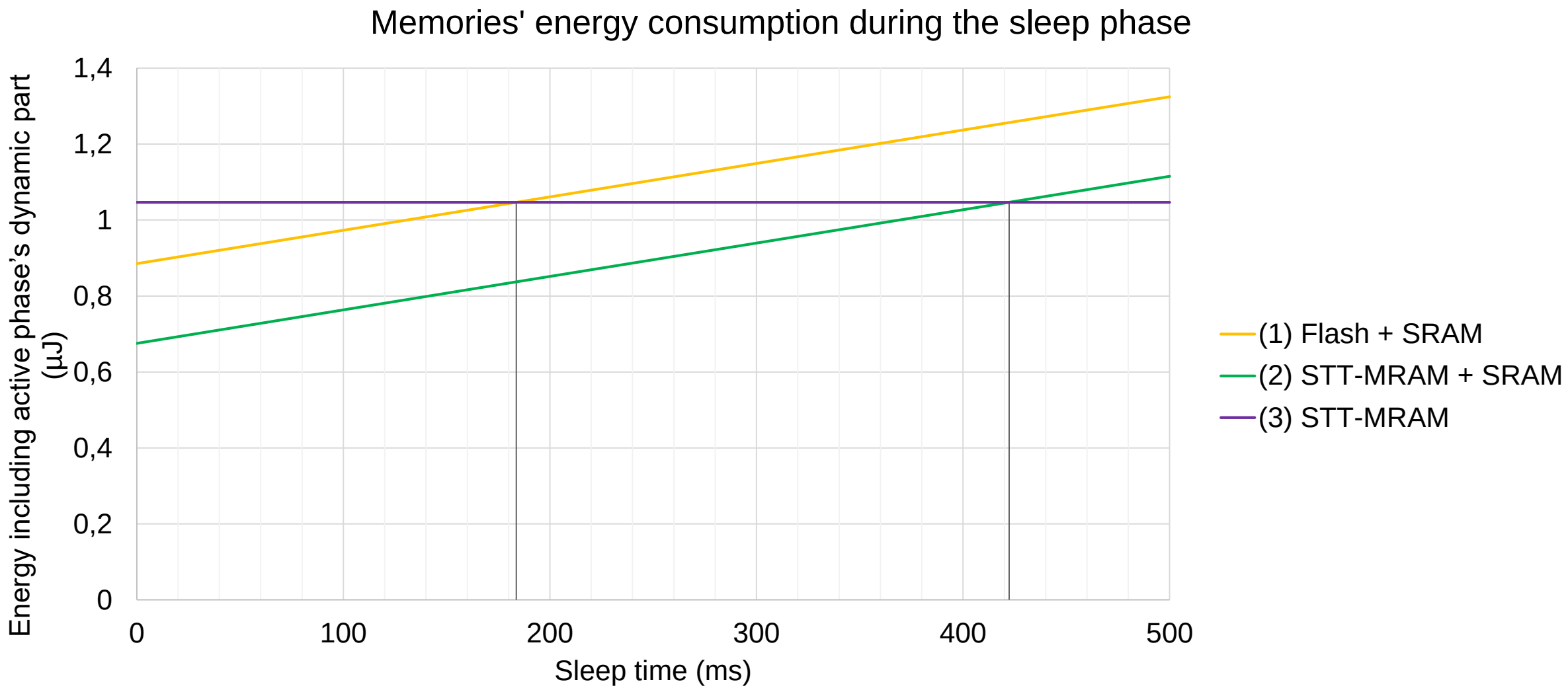
Main memory exploration (active phase)



Main memory extrapolation (periodic behaviour)

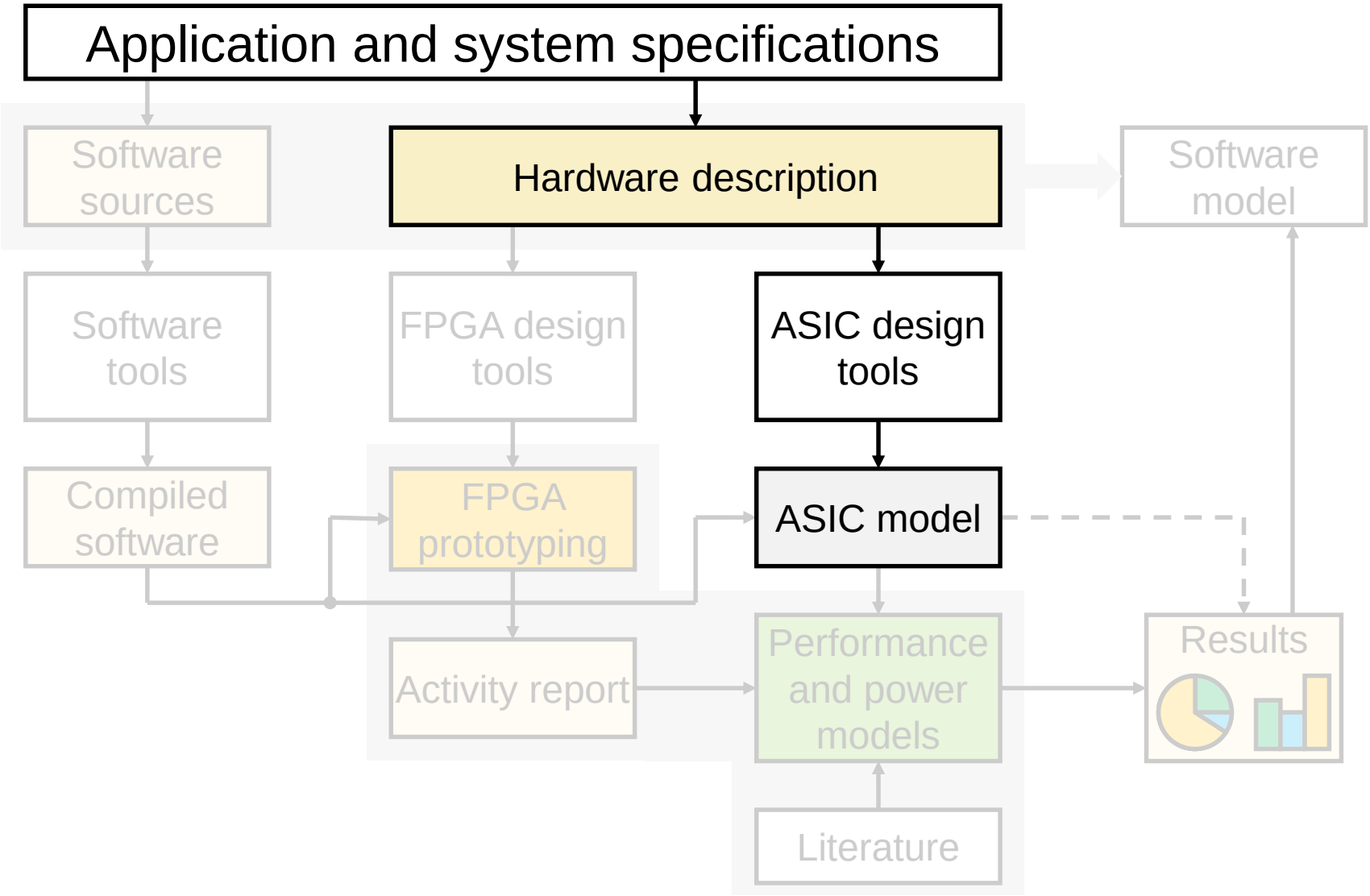


Main memory extrapolation (periodic behaviour)

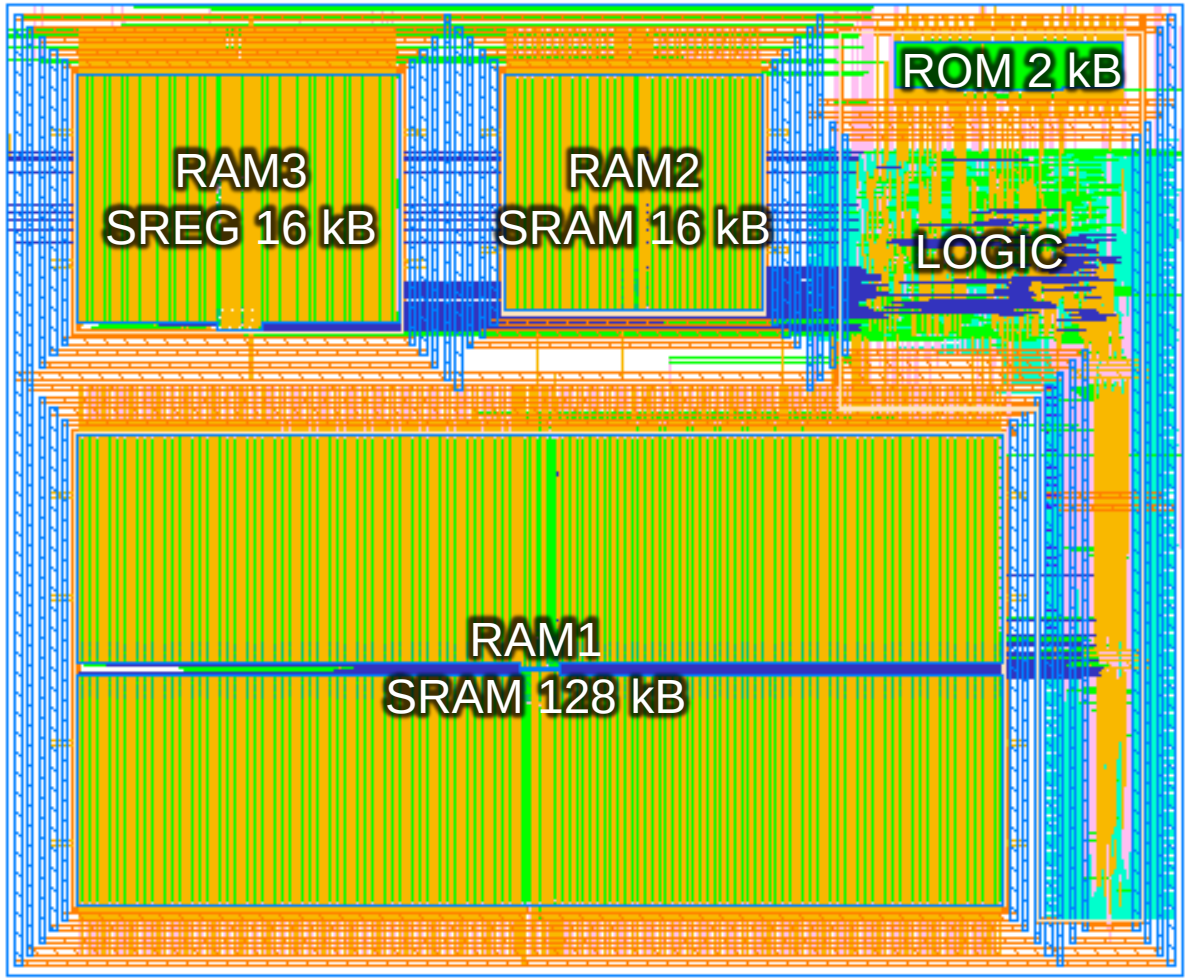


G. Patrigeon *et al.*, "Design and Evaluation of a 28-nm FD-SOI STT-MRAM for Ultra-Low Power Microcontrollers".

Exploration flow

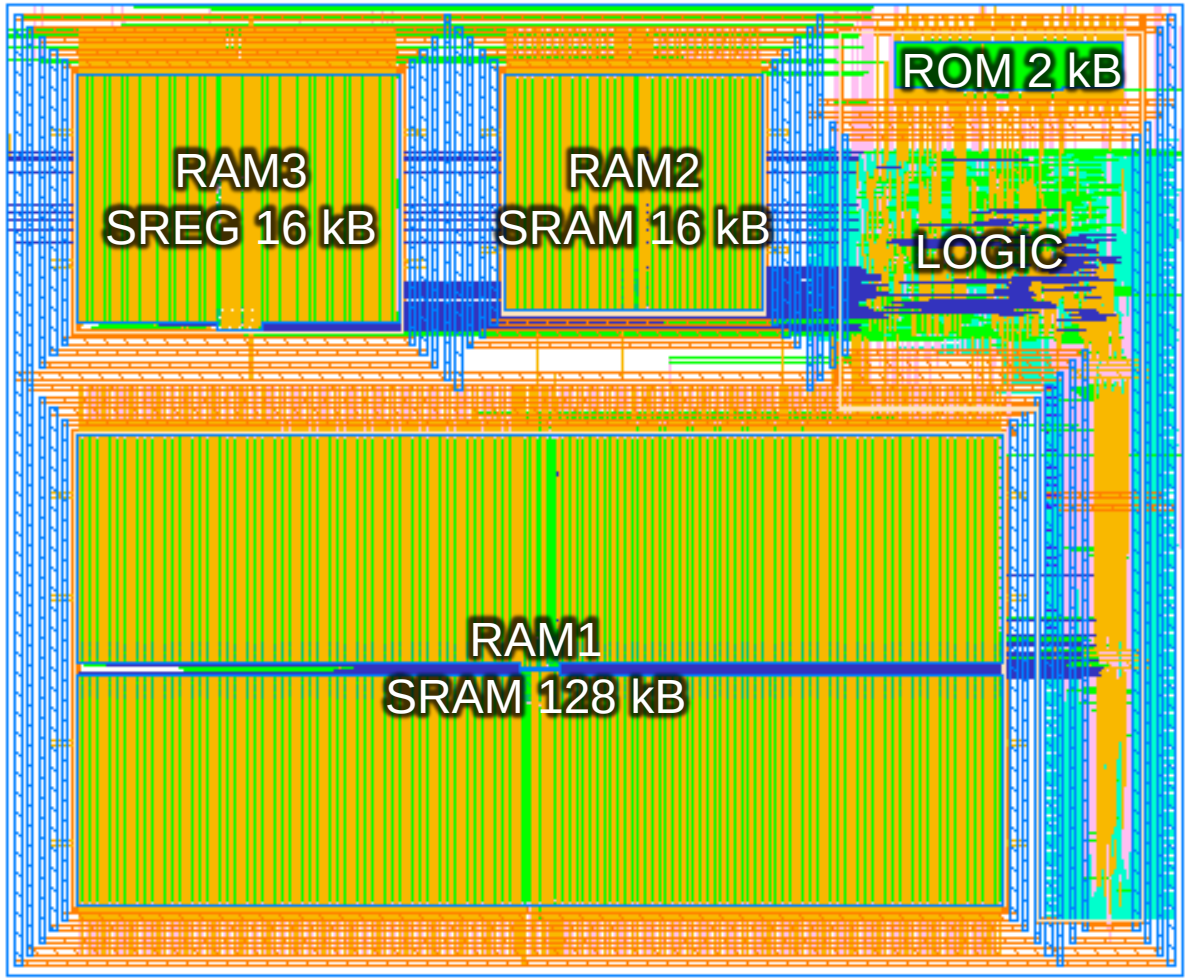


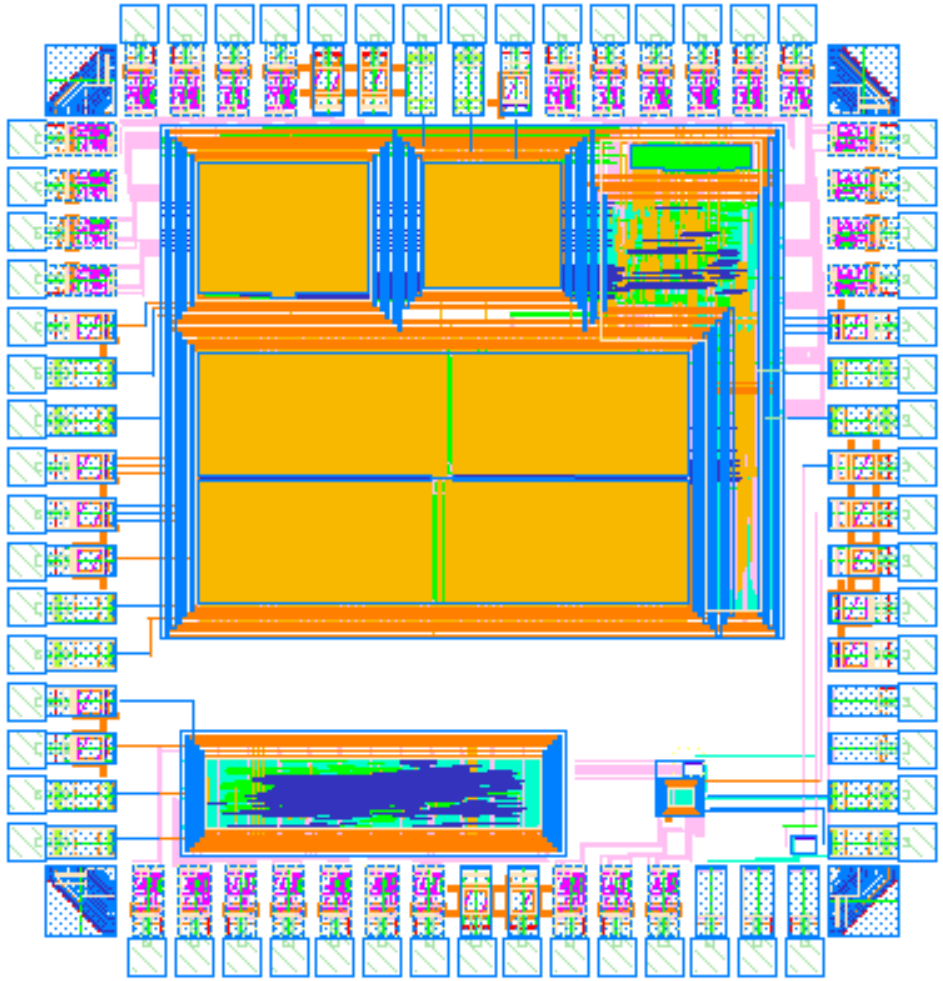
28 nm FD-SOI design



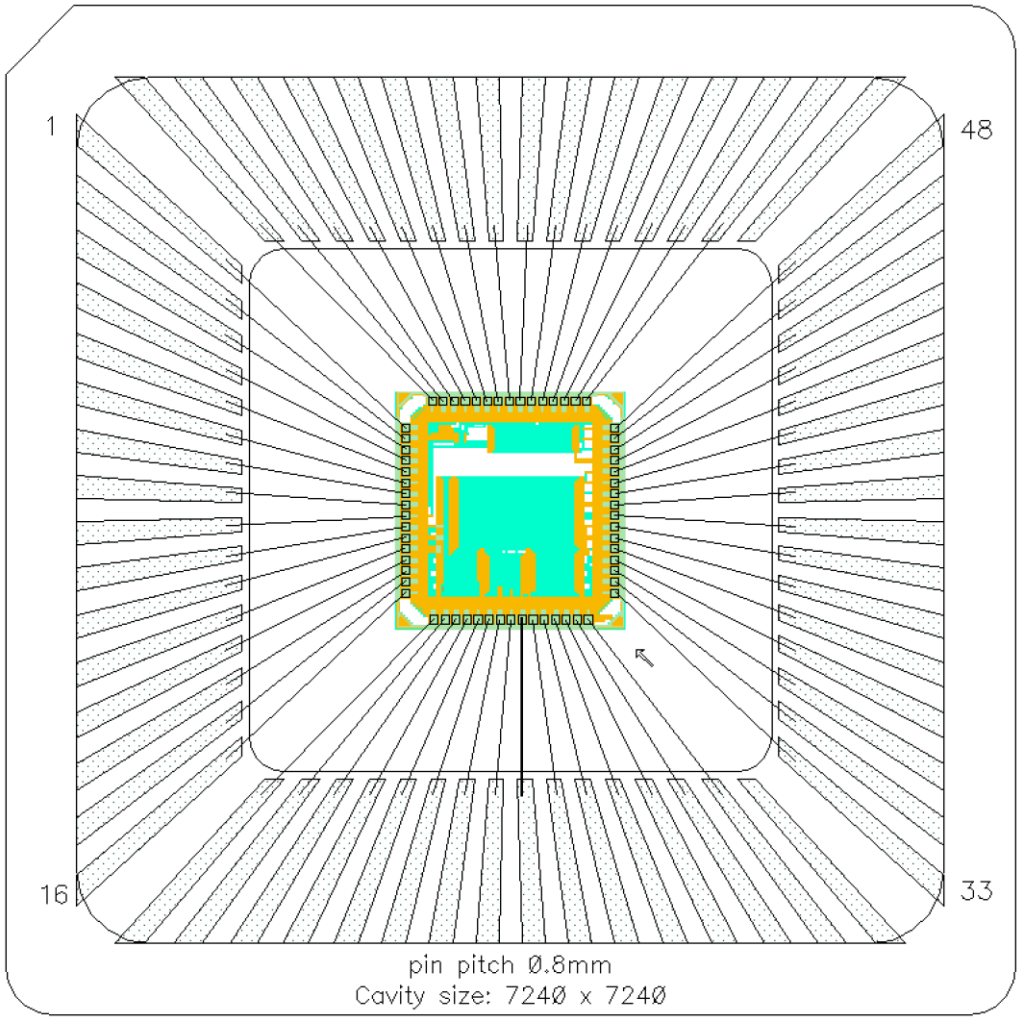
- STMicroelectronics 28 nm FD-SOI design kit
- Regular threshold voltage transistor (RVT)
- Clock frequency constraint set to 50 MHz
- Nominal voltage 0.9 V
- Individual power lines for memories
- RAM1 is made from two 64 kB SRAM banks

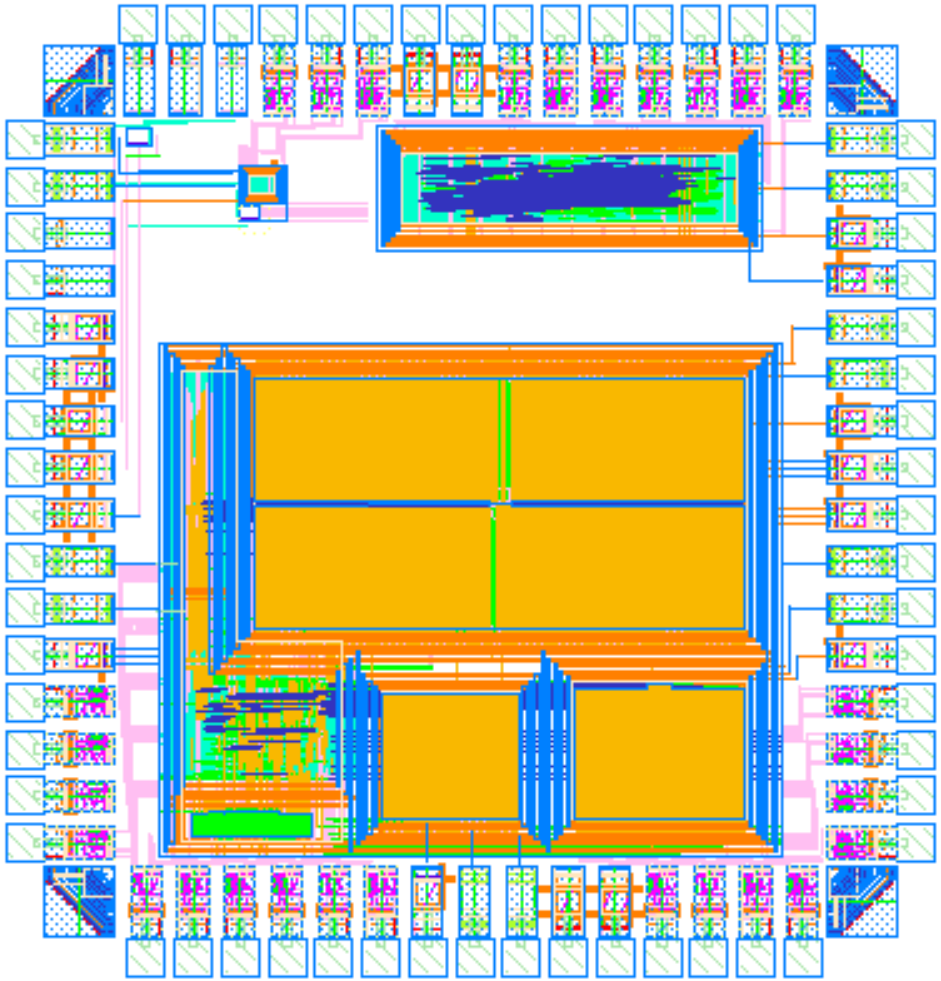
28 nm FD-SOI design





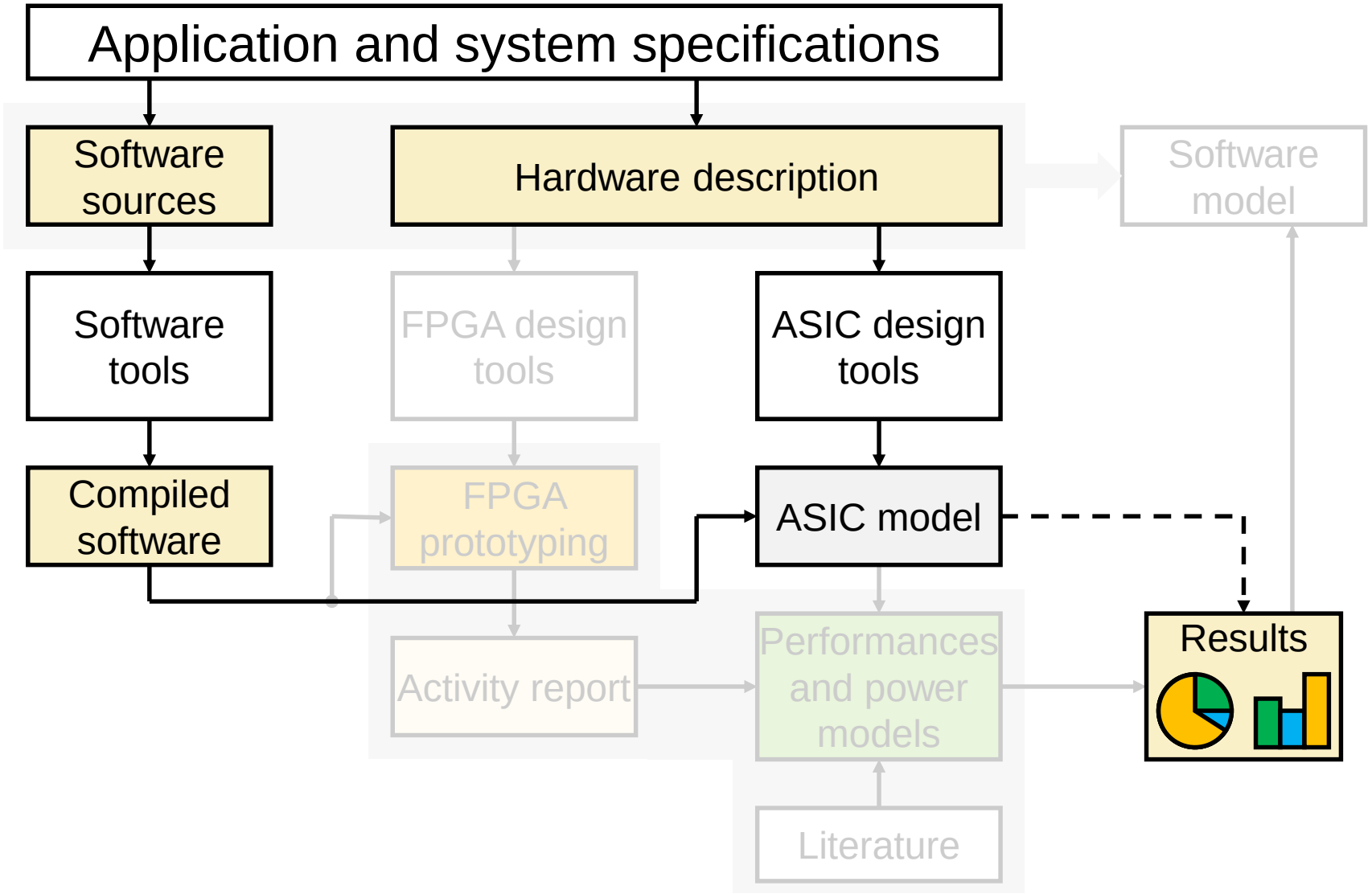
28 nm FD-SOI design



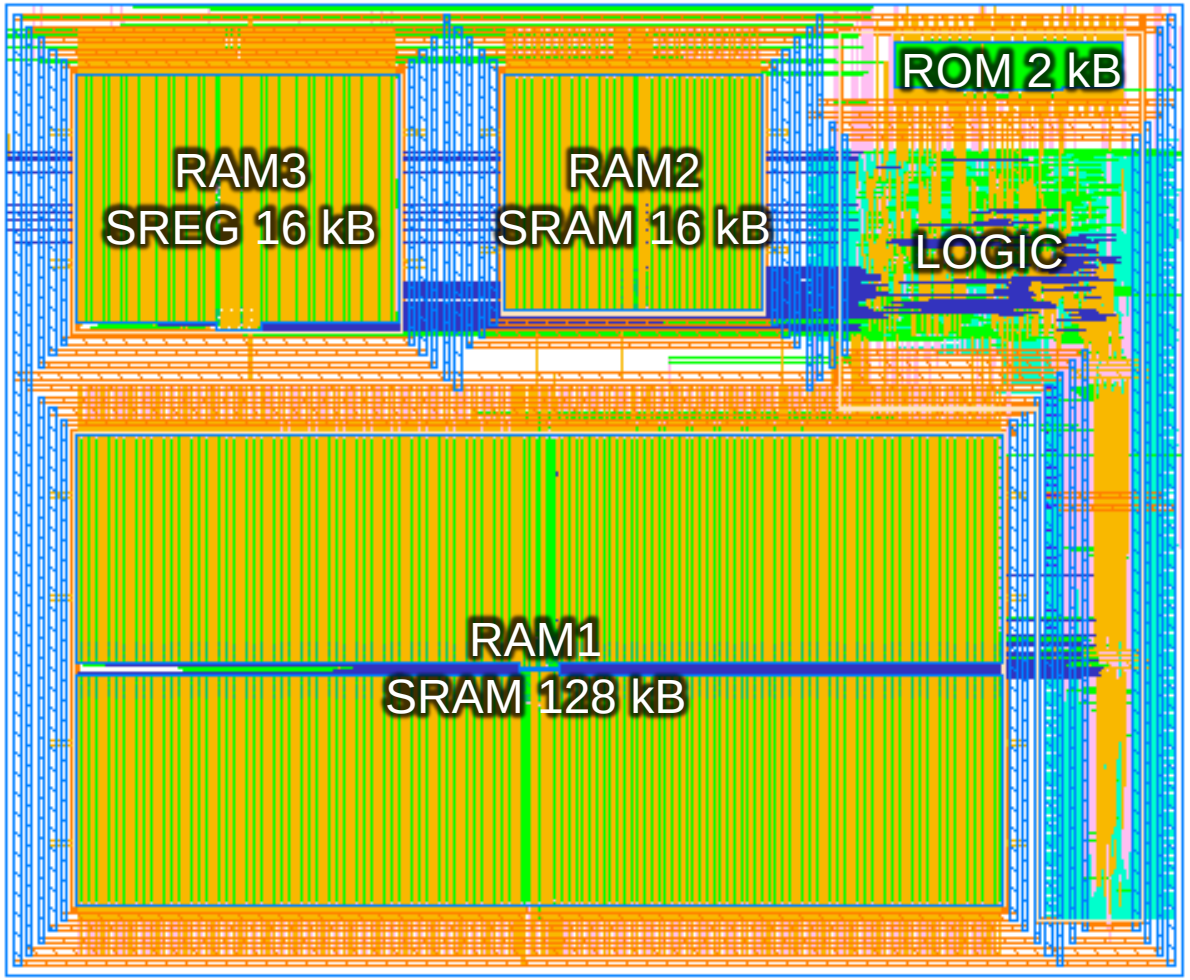


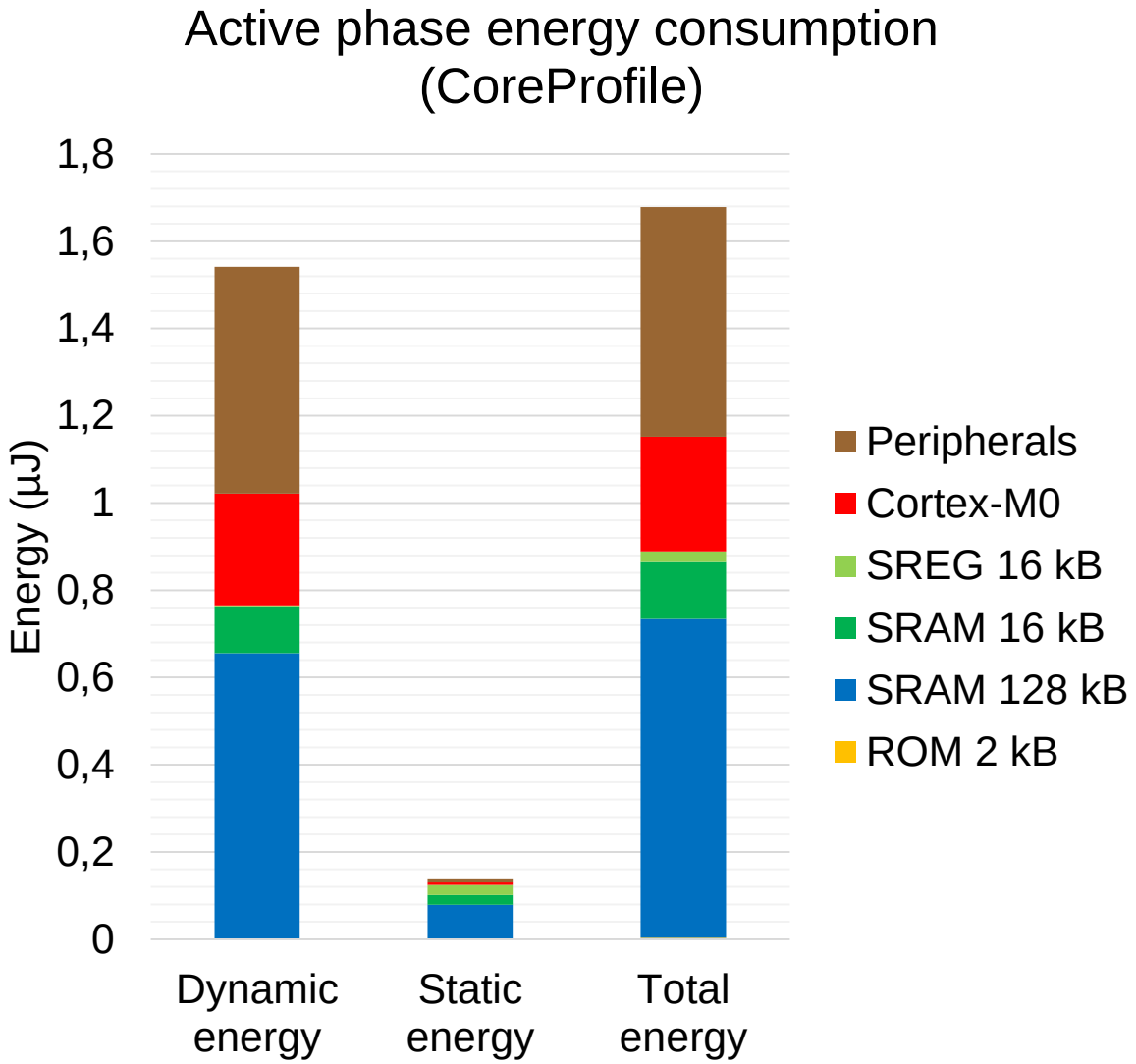
Delivery expected in September

Exploration flow

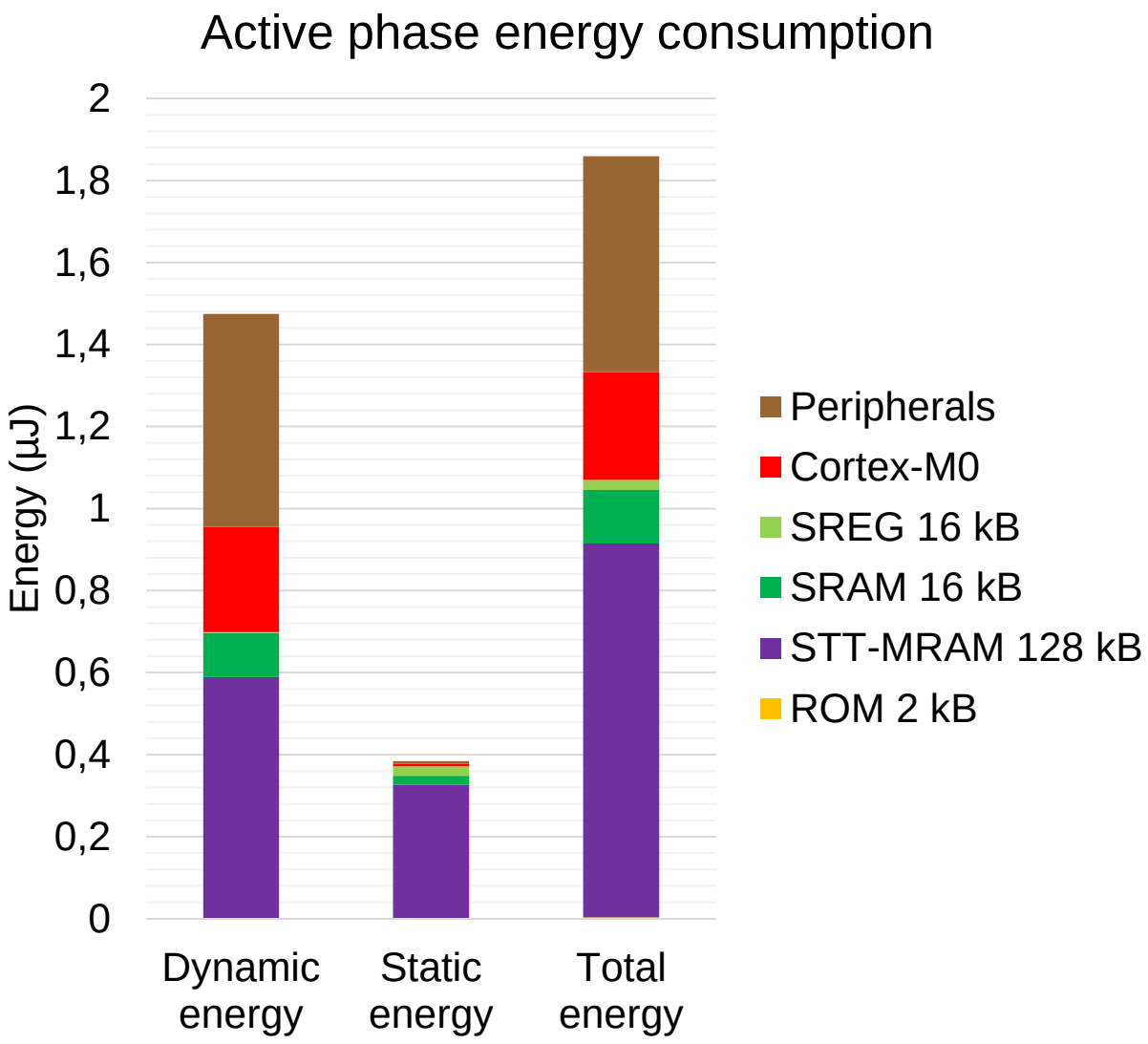


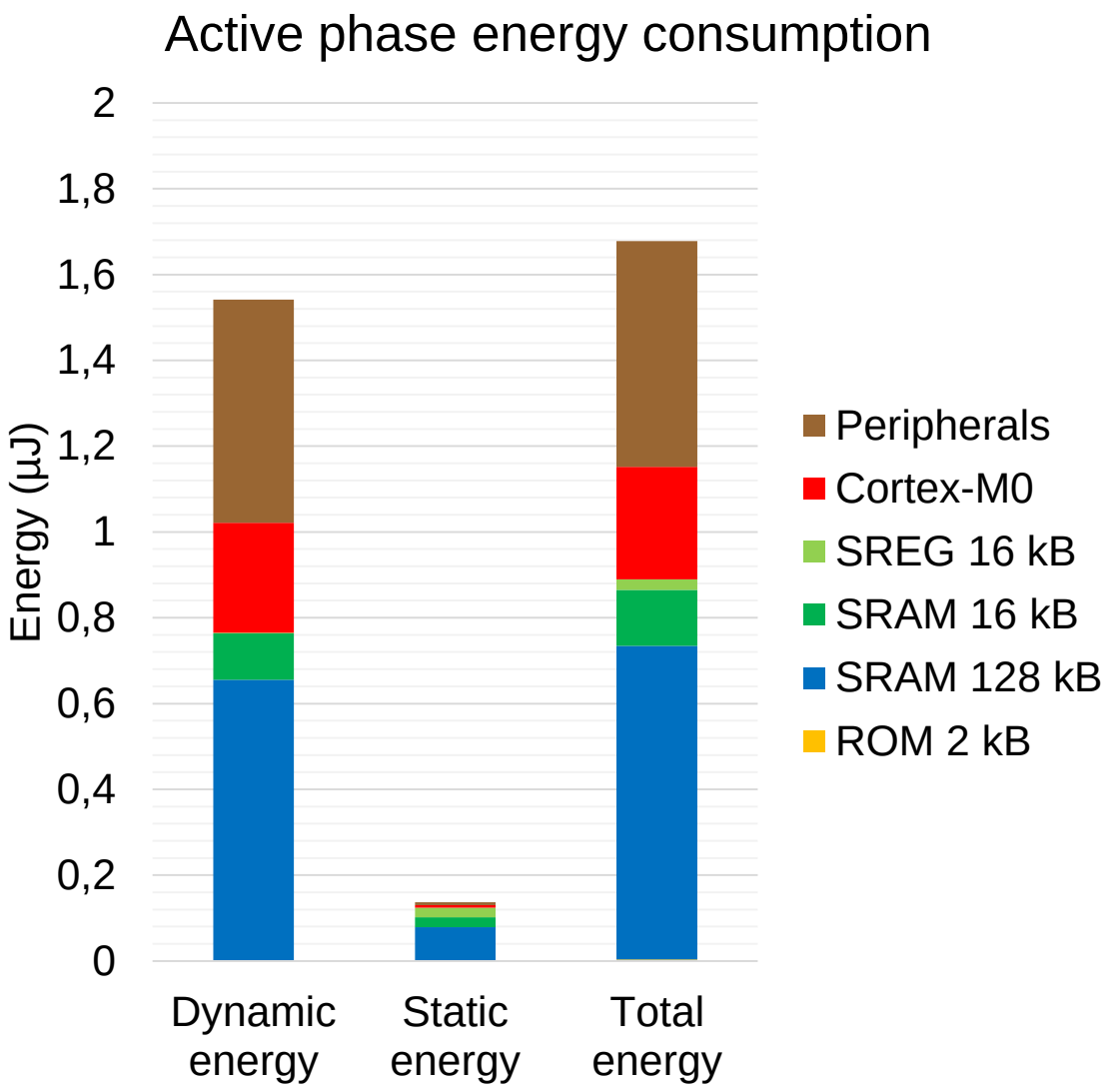
Simulation (active phase)



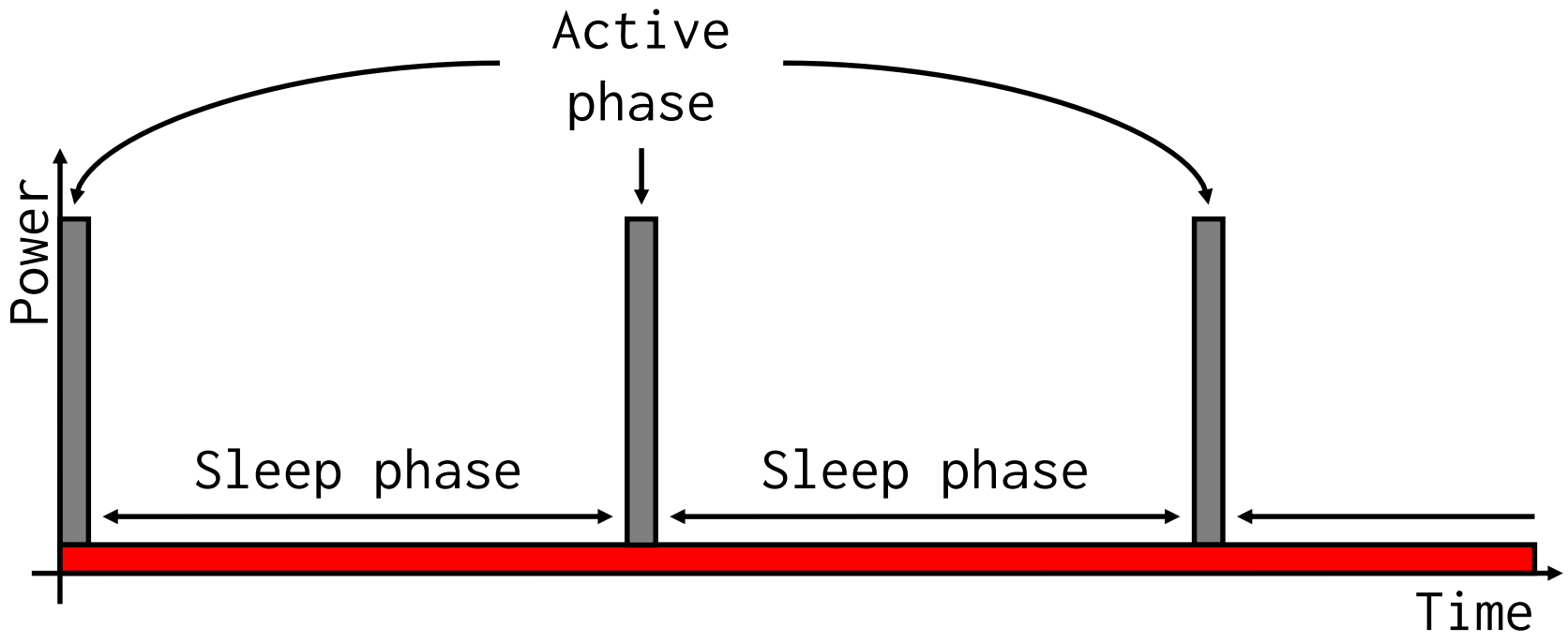


Extrapolation (active phase)





Extrapolation (periodic behaviour)



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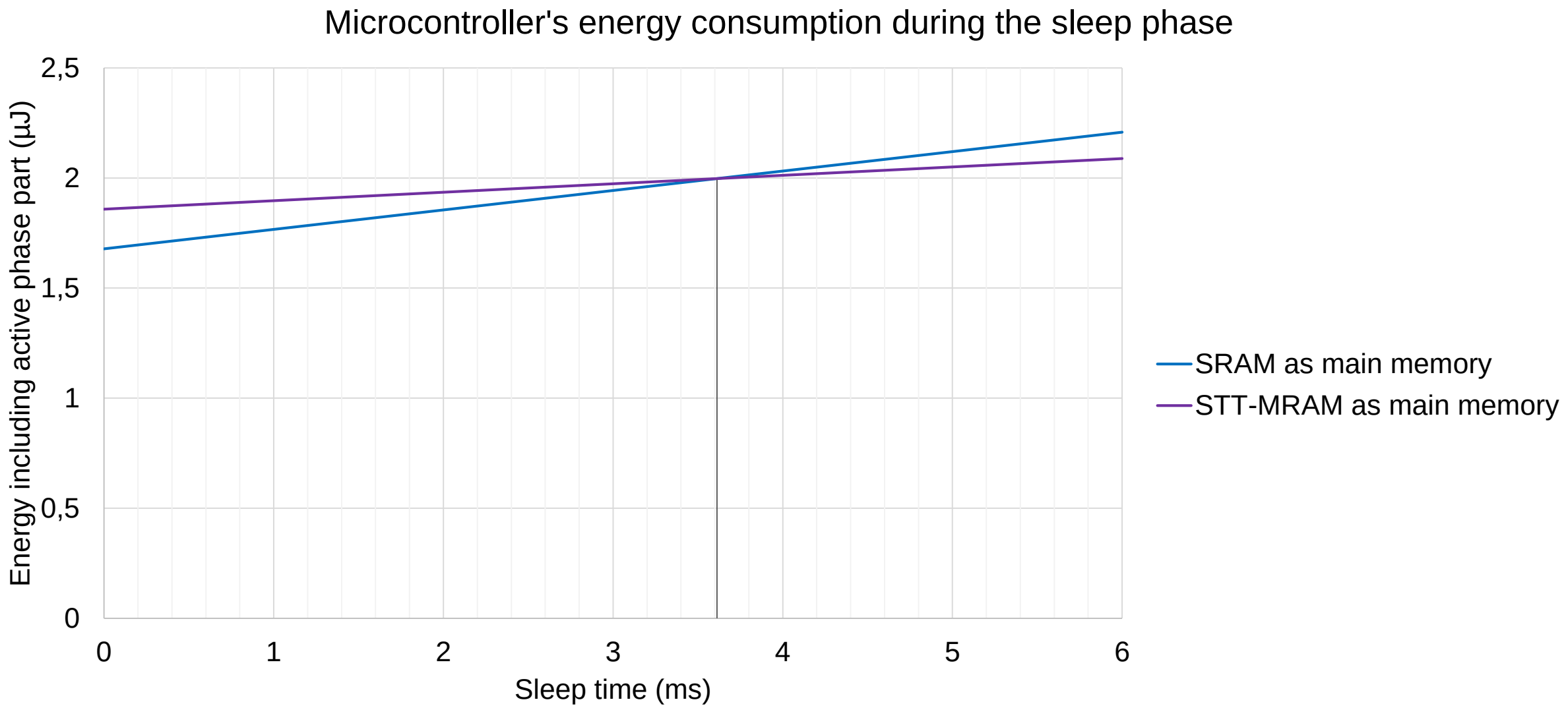

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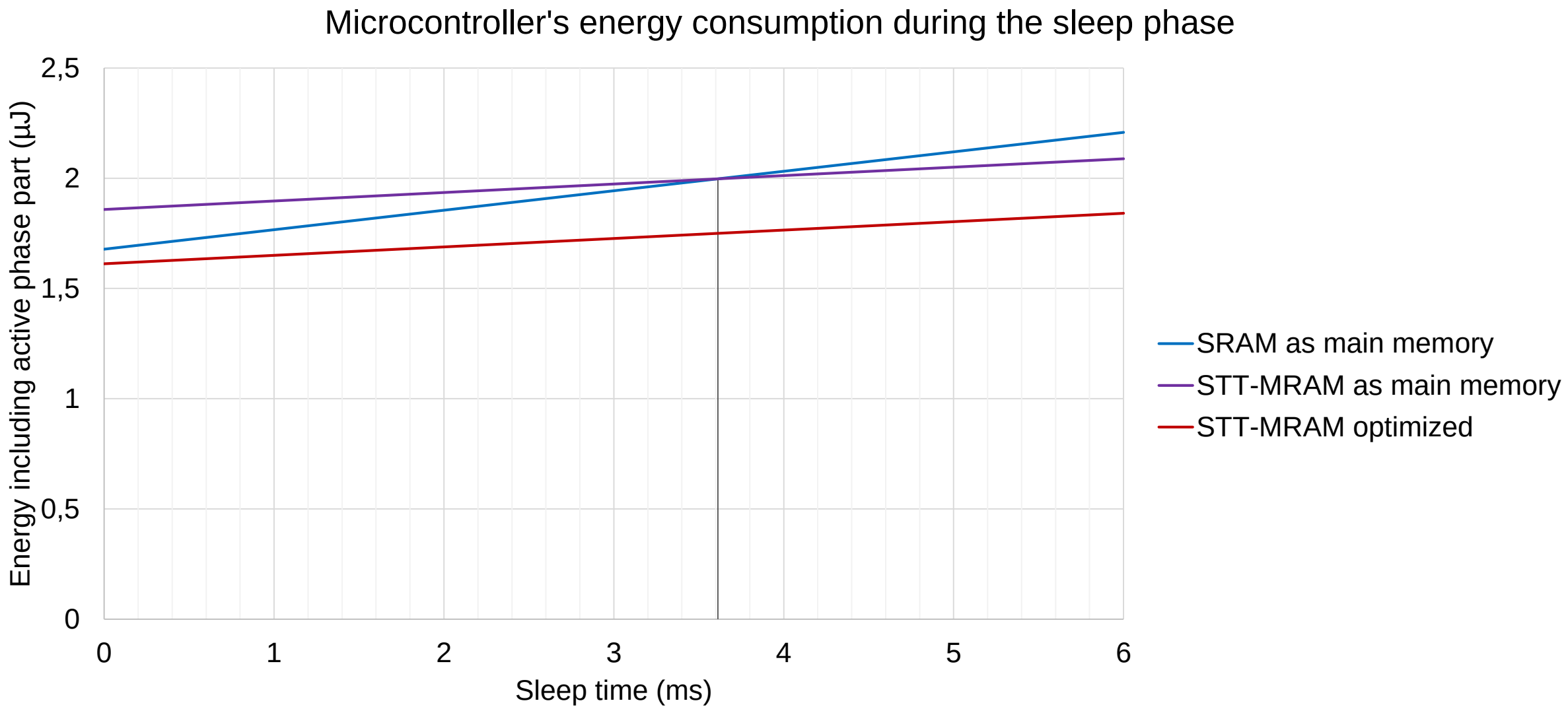
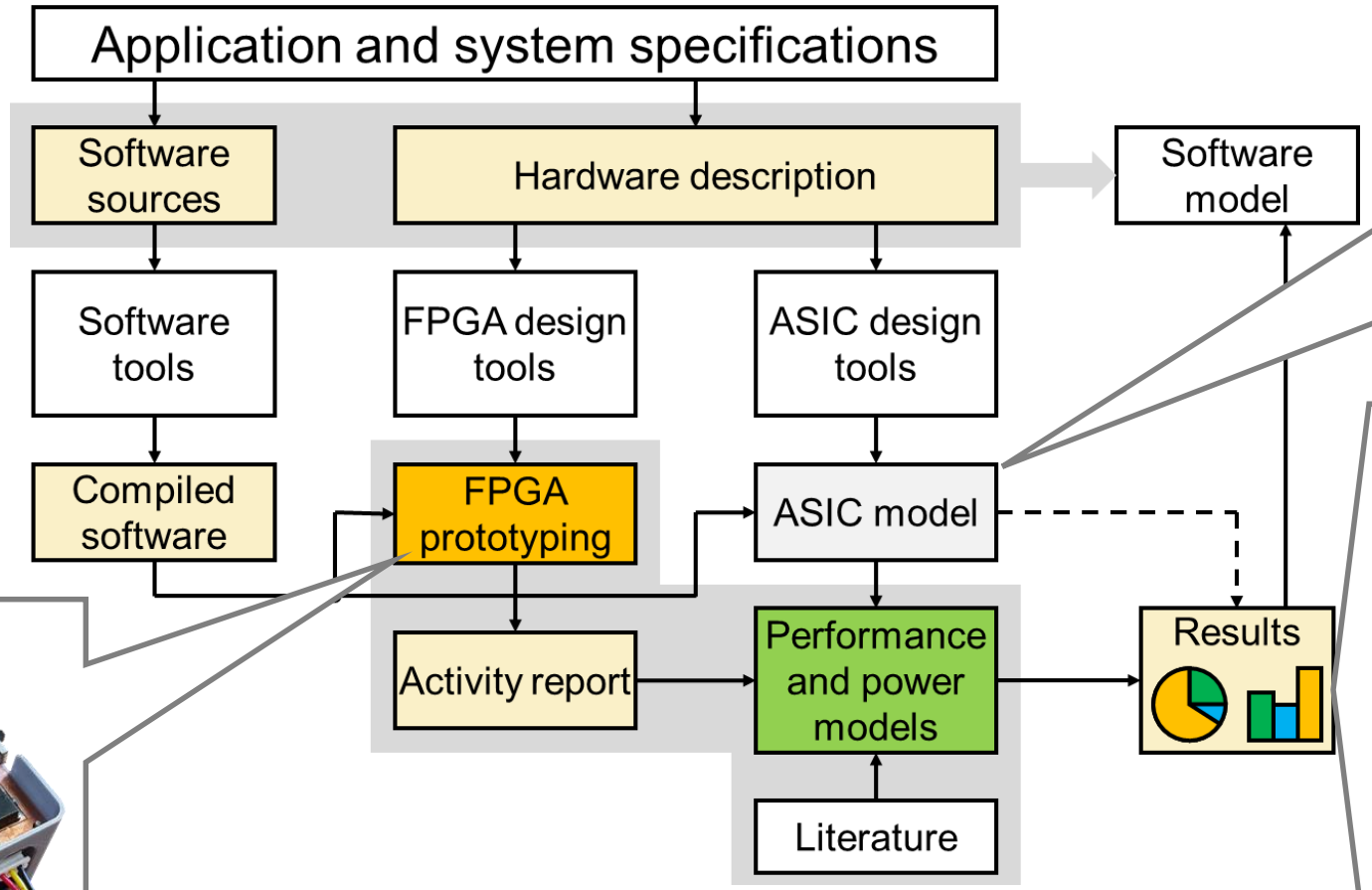
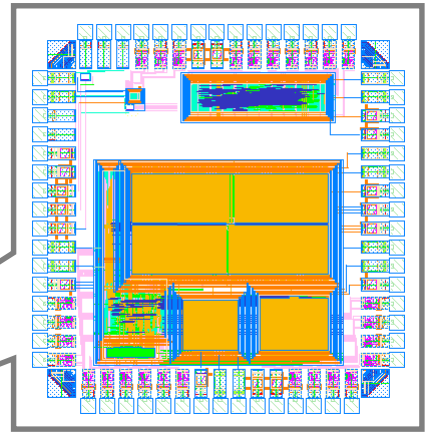
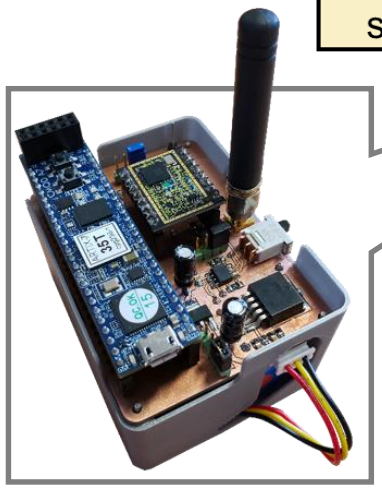


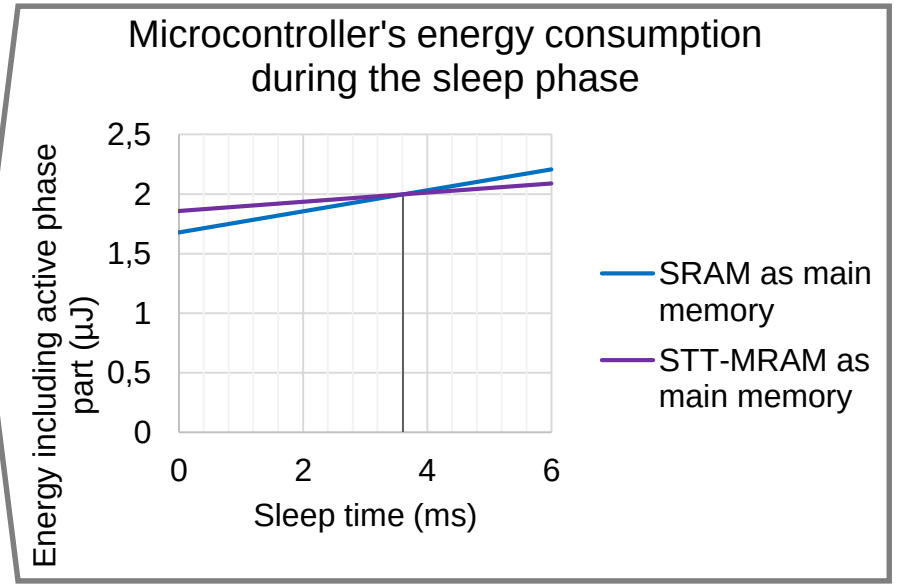
Conclusion

How can we use emerging technologies to improve sensor nodes' energy efficiency?







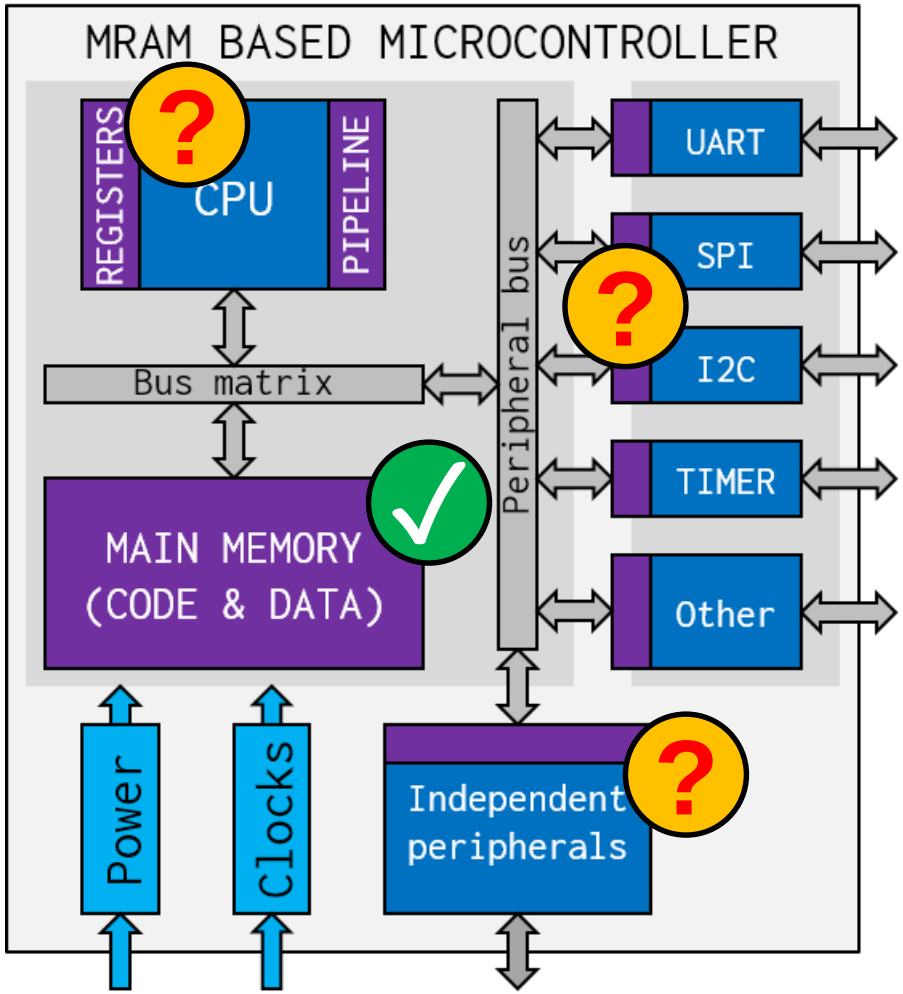


Publications

- **Guillaume Patrigeon**, Paul Leloup, Pascal Benoit and Lionel Torres, “FlexNode: a reconfigurable Internet of Things node for design evaluation”, in proceedings of *2019 IEEE Sensors Applications Symposium (SAS)*, 2019.
- **Guillaume Patrigeon**, Pascal Benoit, Lionel Torres, Sophiane Senni, Guillaume Prenat and Gregory Di Pendina, “Design and Evaluation of a 28-nm FD-SOI STT-MRAM for Ultra-Low Power Microcontrollers”, *IEEE Access*, 2019.
- **Guillaume Patrigeon**, Pascal Benoit and Lionel Torres, “FPGA-Based Platform for Fast Accurate Evaluation of Ultra Low Power SoC”, in proceedings of *2018 28th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2018.
- Mehdi Baradaran Tahoori, Sarath Mohanachandran Nair, Rajendra Bishnoi, Lionel Torres, Sophiane Senni, **Guillaume Patrigeon**, Pascal Benoit, Gregory Di Pendina and Guillaume Prenat, ‘A Universal Spintronic Technology based on Multifunctional Standardized Stack’, *2020 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2020.
- Pascal Benoit, Loic Dalmasso, **Guillaume Patrigeon**, Thierry Gil, Florent Bruguier and Lionel Torres, “Edge-Computing Perspectives with Reconfigurable Hardware”, in proceedings of *2019 14th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*, 2019.
- Sophiane Senni, Frederic Ouattara, Jad Modad, Kaan Sevin, **Guillaume Patrigeon**, Pascal Benoit, Pascal Nouet, Lionel Torres, François Duhem, Gregory Di Pendina and Guillaume Prenat, “From Spintronic Devices to Hybrid CMOS/Magnetic System On Chip”, in proceedings of *2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2018.
- Odilia Coi, **Guillaume Patrigeon**, Sophiane Senni, Lionel Torres and Pascal Benoit, “A novel SRAM — STT-MRAM hybrid cache implementation improving cache performance”, in proceedings of *2017 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2017.

Perspectives

- Consolidate models with ASIC characterization
- Create models for the processor and the peripherals
- Investigate hybrid processor and hybrid peripherals
- Investigate other technologies (SOT, FeRAM...)
- Evaluate different processors
- Integration of accelerators (DMA...)
- Toward edge computing?



Thank you!